

Features

- High speed
 - 25 ns
- CMOS for optimum speed/power
- Low active power
 - 880 mW
- Low standby power
 - 220 mW
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

The CY7C197N is a high-performance CMOS static RAM organized as 256 K words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}) and three-state drivers. The CY7C197N has an automatic power-down feature, reducing the power consumption by 75% when deselected.

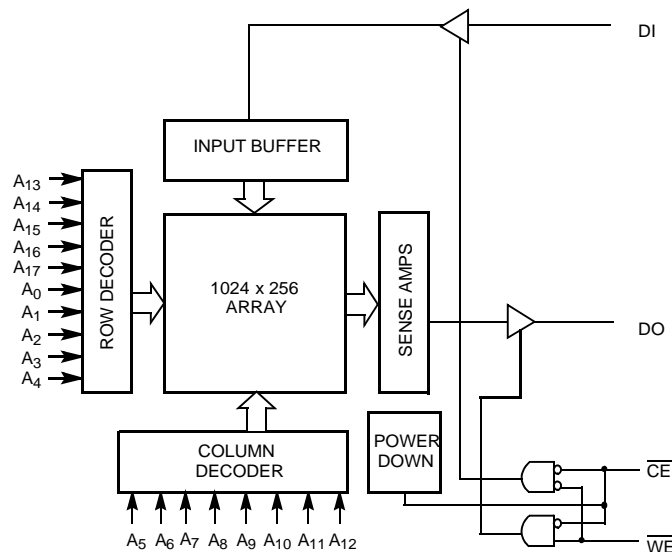
Writing to the device is accomplished when the Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable (\overline{CE}) LOW while Write Enable (\overline{WE}) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

The output pin stays in a high-impedance state when Chip Enable (\overline{CE}) is HIGH or Write Enable (\overline{WE}) is LOW.

The CY7C197N uses a die coat to insure alpha immunity.

Logic Block Diagram

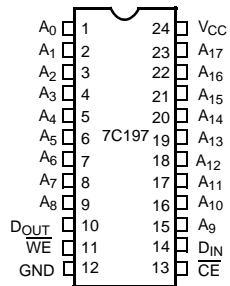


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Pin Configurations

Figure 1. 24-pin DIP (Top View)



Selection Guide

| Description | -25 |
|--------------------------------|-----|
| Maximum access time (ns) | 25 |
| Maximum operating current (mA) | 95 |
| Maximum standby current (mA) | 30 |

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage to ground potential (Pin 24 to Pin 12)..... -0.5 V to +7.0 V
 DC voltage applied to outputs in High Z state^[1] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage^[1] -0.5 V to $V_{CC} + 0.5$ V
 Output current into outputs (LOW) 20 mA
 Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)
 Latch up current..... > 200 mA

Operating Range

| Range | Ambient Temperature | V_{CC} |
|------------|---------------------|-----------|
| Commercial | 0 °C to +70 °C | 5 V ± 10% |

Electrical Characteristics

Over the Operating Range

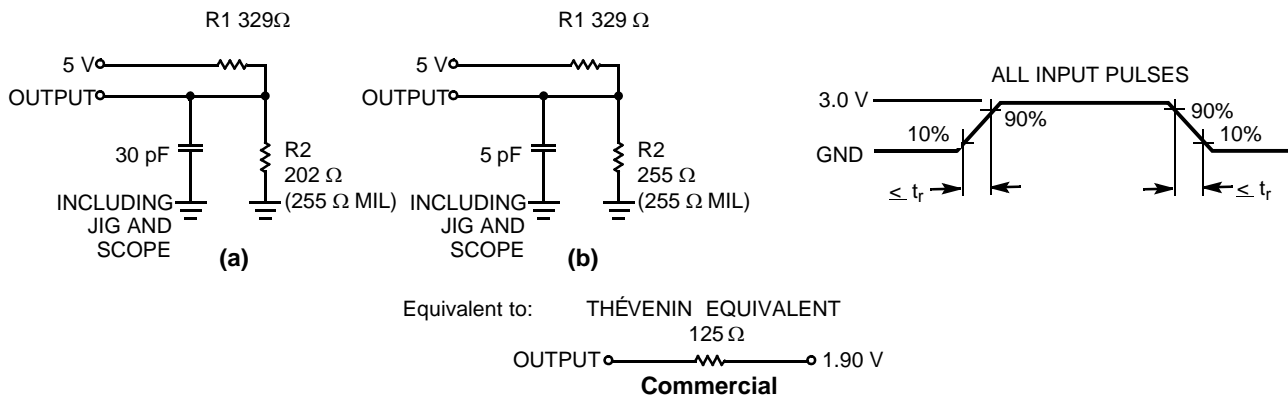
| Parameter | Description | Test Conditions | -25 | | Unit |
|-----------|---|---|------|------------------|------|
| | | | Min | Max | |
| V_{OH} | Output HIGH voltage | $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA | 2.4 | – | V |
| V_{OL} | Output LOW voltage | $V_{CC} = \text{Min}, I_{OL} = 12.0$ mA | – | 0.4 | V |
| V_{IH} | Input HIGH voltage | | 2.2 | $V_{CC} + 0.3$ V | V |
| V_{IL} | Input LOW voltage ^[1] | | -0.5 | 0.8 | V |
| I_{IX} | Input load current | $GND \leq V_I \leq V_{CC}$ | -5 | +5 | µA |
| I_{OZ} | Output leakage current | $GND \leq V_O \leq V_{CC}$, Output Disabled | -5 | +5 | µA |
| I_{OS} | Output short circuit current ^[2] | $V_{CC} = \text{Max}, V_{OUT} = GND$ | – | -300 | mA |
| I_{CC} | V_{CC} operating supply current | $V_{CC} = \text{Max}, I_{OUT} = 0$ mA, $f = f_{MAX} = 1/t_{RC}$ | – | 95 | mA |
| I_{SB1} | Automatic \overline{CE} power-down current—TTL inputs ^[3] | Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | – | 30 | mA |
| I_{SB2} | Automatic \overline{CE} power-down current—CMOS inputs ^[3] | Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} < 0.3$ V | – | 15 | mA |

Capacitance^[4]

| Parameter | Description | Test Conditions | Max | Unit |
|-----------|--------------------|--|-----|------|
| C_{IN} | Input capacitance | $T_A = 25$ °C, $f = 1$ MHz, $V_{CC} = 5.0$ V | 8 | pF |
| C_{OUT} | Output capacitance | | 10 | pF |

Notes

- $V_{(min.)} = -2.0$ V for pulse durations of less than 20 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V_{CC} on the \overline{CE} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
- Tested initially and after any design or process changes that may affect these parameters.

Figure 2. AC Test Loads and Waveforms^[5]


Switching Characteristics

 Over the Operating Range^[6]

| Parameter | Description | -25 | | Unit |
|----------------------------------|---|-----|-----|------|
| | | Min | Max | |
| READ CYCLE | | | | |
| t_{RC} | Read cycle time | 25 | – | ns |
| t_{AA} | Address to data valid | – | 25 | ns |
| t_{OHA} | Output hold from address change | 3 | – | ns |
| t_{ACE} | \overline{CE} LOW to data valid | – | 25 | ns |
| t_{LZCE} | \overline{CE} LOW to low $Z^{[7]}$ | 3 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to high $Z^{[7, 8]}$ | 0 | 11 | ns |
| t_{PU} | \overline{CE} LOW to power-up | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to power-down | – | 20 | ns |
| WRITE CYCLE^[9] | | | | |
| t_{WC} | Write cycle time | 25 | – | ns |
| t_{SCE} | \overline{CE} LOW to write end | 20 | – | ns |
| t_{AW} | Address setup to write end | 20 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 20 | – | ns |
| t_{SD} | Data setup to write end | 15 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | ns |
| t_{LZWE} | \overline{WE} HIGH to low $Z^{[7]}$ | 3 | – | ns |
| t_{HZWE} | \overline{WE} LOW to high $Z^{[7, 8]}$ | 0 | 11 | ns |

Notes

- $t_r = \leq 5$ ns for the -25 and slower speeds.
- Test conditions assume signal transition time of 5 ns or less for -25 and slower speeds, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

Figure 3. Read Cycle No. 1^[10, 11]

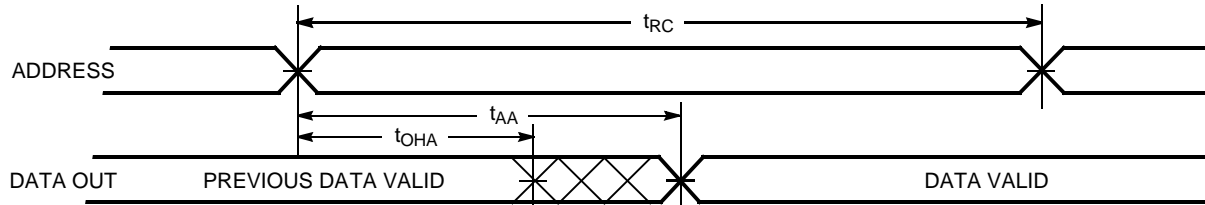


Figure 4. Read Cycle No. 2^[10]

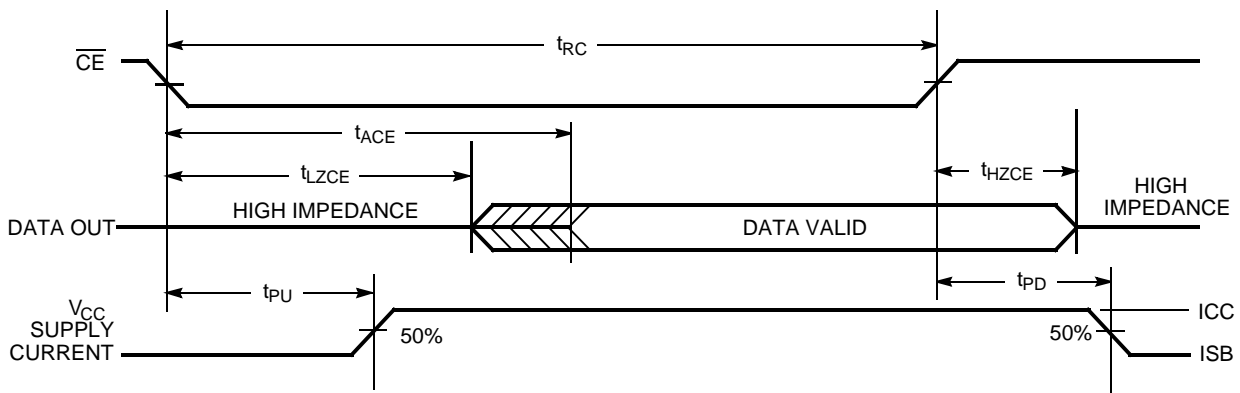
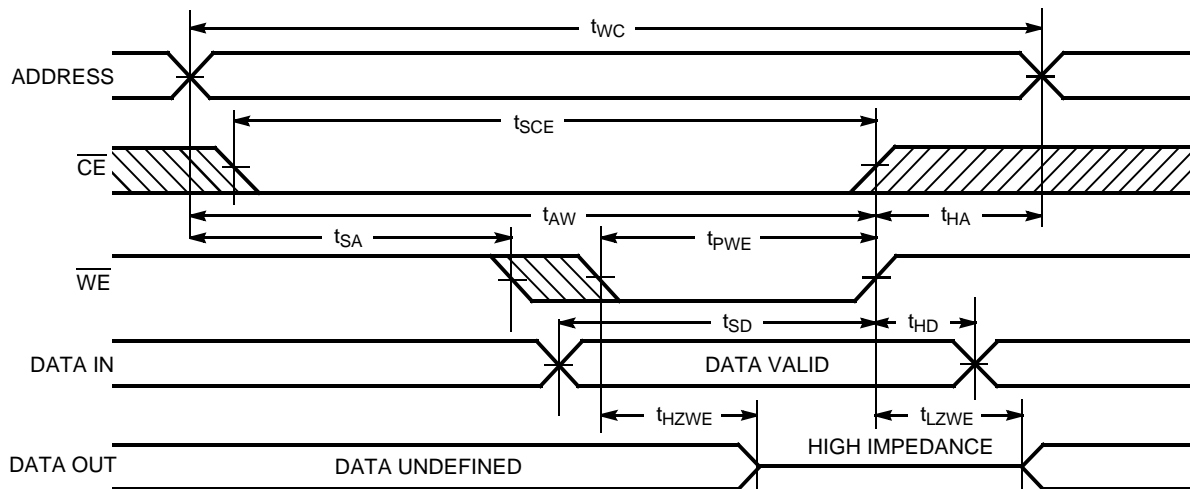


Figure 5. Write Cycle No. 1 (\overline{WE} Controlled)^[12]



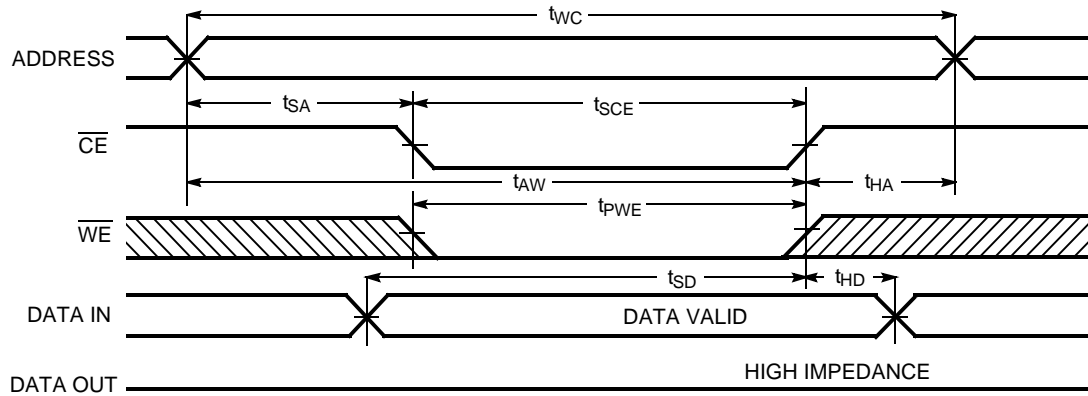
C197-8

Notes

- 10. \overline{WE} is HIGH for read cycle.
- 11. Device is continuously selected, $\overline{CE} = V_{IH}$.
- 12. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

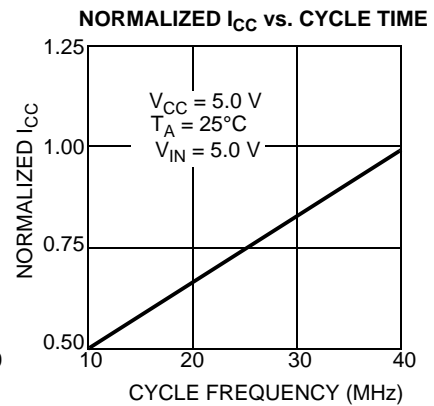
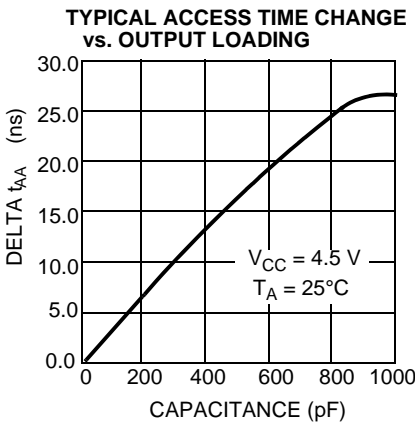
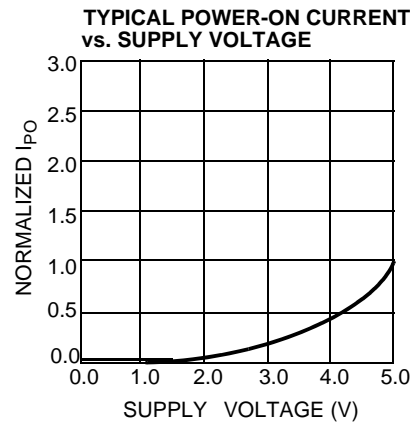
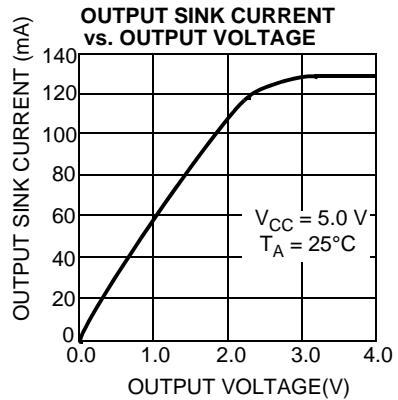
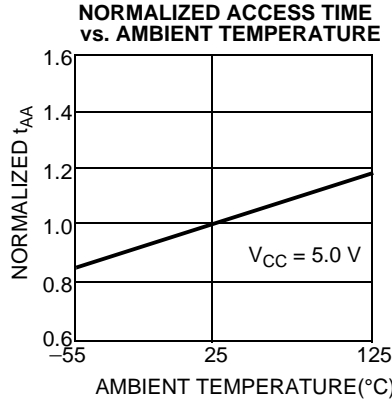
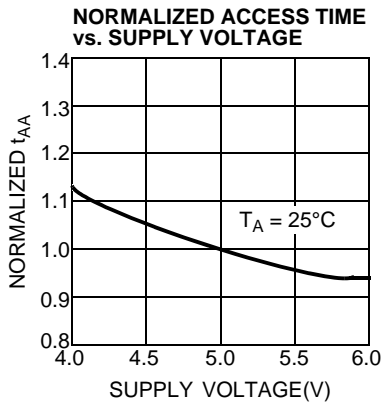
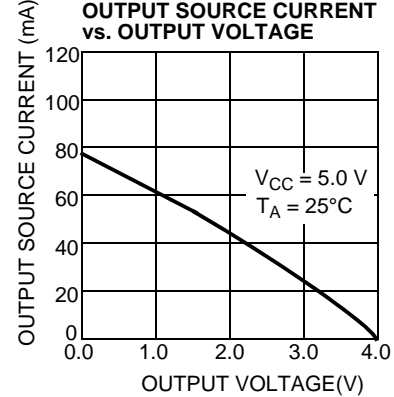
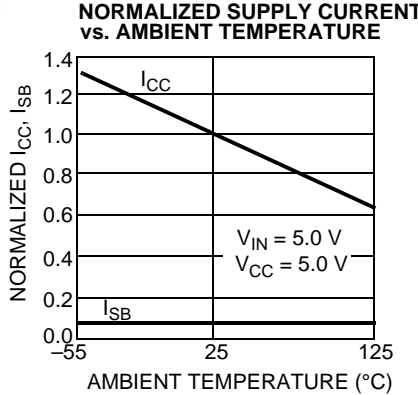
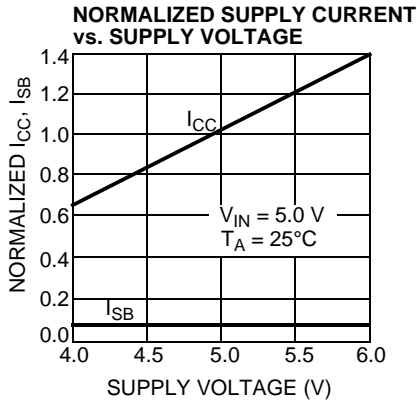
Figure 6. Write Cycle No. 2 (\overline{CE} Controlled)^[13, 14]



Notes

- 13. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- 14. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



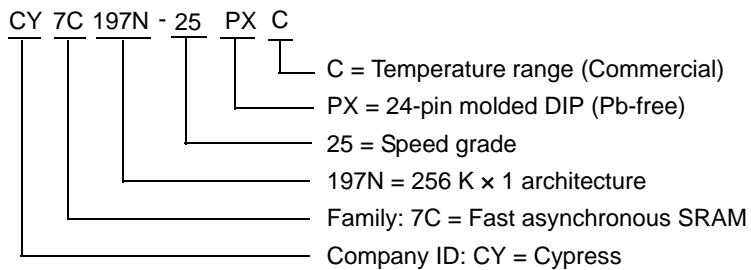
CY7C197N Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | Input/Output | Mode |
|------------------------|------------------------|--------------|---------------------|
| H | X | High Z | Deselect/Power-Down |
| L | H | Data Out | Read |
| L | L | Data In | Write |

Ordering Information

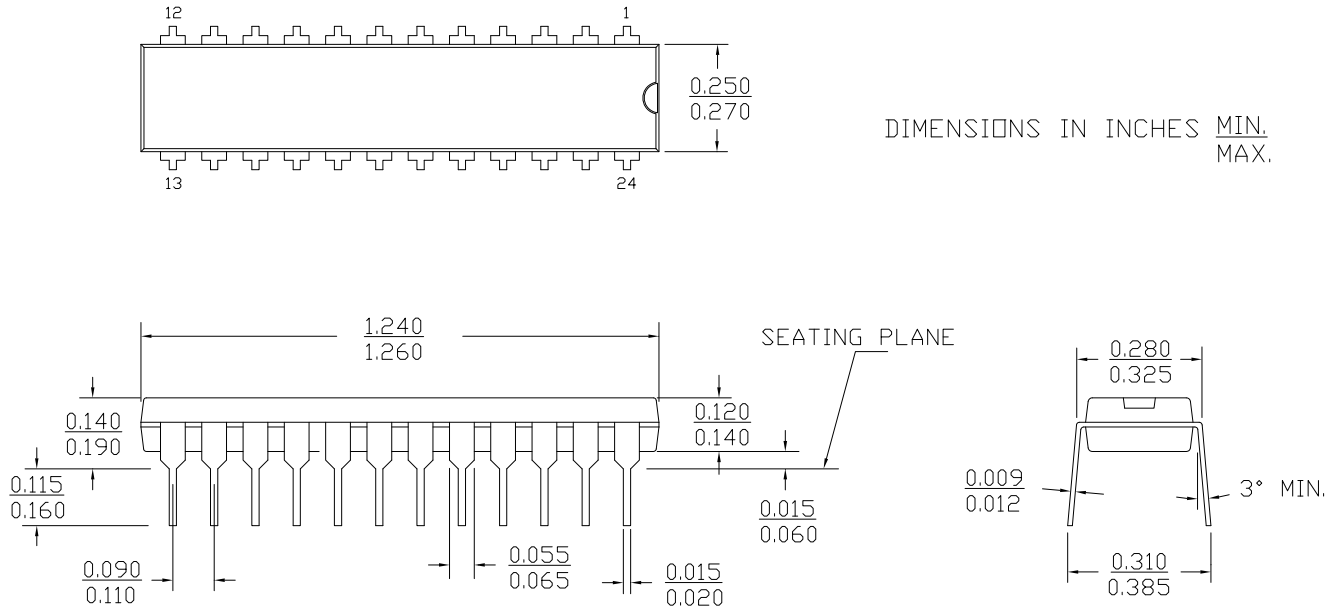
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|----------------|-----------------|---------------------------------------|-----------------|
| 25 | CY7C197N-25PXC | 51-85013 | 24-pin (300-Mil) Molded DIP (Pb-free) | Commercial |

Contact your local sales representative regarding availability of these parts.

Ordering Code Definitions


Package Diagram

Figure 7. 24-pin (300-Mil) PDIP (51-85013)



51-85013 *C

Acronyms

| Acronym | Description |
|---------|---|
| CE | chip enable |
| CMOS | complementary metal oxide semiconductor |
| DIP | dual inline package |
| I/O | input/output |
| PDIP | plastic dual inline package |
| SRAM | static random access memory |
| TTL | transistor-transistor logic |
| WE | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| % | percent |
| °C | degree Celsius |
| mA | milliamperes |
| MHz | megahertz |
| mV | millivolts |
| mW | milliwatts |
| ns | nanoseconds |
| pF | picofarads |
| V | volts |
| Ω | ohms |
| W | watts |
| μA | microamperes |

Document History Page

| Document Title: CY7C197N, 256 K x 1 Static RAM Document Number: 001-06495 | | | | |
|--|---------|-----------------|-----------------|--|
| REV. | ECN NO. | Submission Date | Orig. of Change | Description of Change |
| ** | 424111 | See ECN | NXR | New Data Sheet |
| *A | 2958594 | 06/22/10 | AJU | The EOL Prune part number CY7C197N-45PXC removed & Updated package diagram. |
| *B | 3095450 | 11/25/2010 | AJU | Updated template. Added Acronyms , Document Conventions , and Ordering Code Definitions Removed -45 information. Changed posting to external web. |
| *C | 3246053 | 05/02/2011 | PRAS | Updated in new template. |
| *D | 3270287 | 07/01/2011 | AJU | Fixed units in Electrical Characteristics table. |

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