

# Si53108 EVALUATION BOARD USER'S GUIDE

#### Description

The Si53108-EVB can be used to evaluate the Si53108-A01AGM, an 8-output PCIe Gen1/2/3 buffer that can operate in either fanout or zero delay mode.

#### Features

- 10-inch traces to evaluate signal integrity
- The signal traces of the input and outputs have a single-ended impedance of 50 ohms, and differential impedance of 100 ohms.
- The series resistance on the outputs are set to match to this impedance design.
- DC pin controls per data sheet specification.
- Ability to measure input to output propagation delay.
- Ability to measure PCIe clock jitter.
- Ability to program features of Si53108-A01AGM via l<sup>2</sup>C interface.



### 1. Schematics





Figure 1. Schematic 1







Figure 2. Schematic 2





Figure 3. Schematic 3



## 2. Input and Power Supply Sequencing

The Si53108-A01AGM should be powered up with supply at both the VDD and VDD\_IO nodes (at the jumpers available on the EVB). A 100MHz or 133MHz HCSL input clock should be applied to pins 8 and 9. There is no internal or on-board resistive termination, therefore HCSL termination needs to be provided at the input if needed by the driver. The input clock should be applied only after the supplies are stable.

### 3. Quick Start Guide:

- 1. Enable supply on the VDD pin.
- 2. Enable supply on the VDDIO pin.
- 3. Apply input clock on the SMA connectors CLK\_IN/CLK\_IN# and measure the return path clock on CLK\_IN\_RET, CLK\_IN#\_RET.



Figure 4. Clock Return Path

- a. The input clock measured at J32, J33 needs a 50-ohm termination on the scope.
- b. The attenuation will be 1:10 after the above termination. Appropriate scaling (10x) needs to be set at the scope to adjust for the scaling.
- 4. The output clocks are now set up and can be measured on an oscilloscope or frequency domain measurement instrument.

#### 4. Usage of the EVB

- 1. Once the EVB has been set up, the following can be evaluated:
- 2. Signal integrity of the device when driving 10-inch, 100-ohm differential traces.
- 3. Effect of capacitance load on output signal integrity.
- 4. Output-to-output skew over 10-inch traces.
- 5. Input-to-output prorogation delay in BYPASS, HBW, and LBW modes using the input clock return path.
- 6. Measuring the power consumption of the device.
- 7. Modification of the device settings via the  $I^2C$  interface.



# 5. Bill of Materials

Item Quar	ntty Reference	Part	PLUE LOUGHT	LOUI MAILINE	to the second seco	IS IN YOUR IN IS INTERED. IN IS INTERED. IS INTE	CONTRACTOR
*	20 DIFF1#, DIFF1, DIFF2#,	SMA_THT	SMA_THT	LTI-SASF54GT	Vertical PCB Thru Hole SMA Jack	LIGHTHORSE	Component Reference-305-PD-13-1158
	DIFF2.DIFF3#.DIFF3.						
	DIFF4# DIFF4 DIFF5#						
	DIFF5.OIFF6#.DIFF6.						
	DIFF7# DIFF7, DIFF0#						
	DIFFO, CLK IN RET.						
	CLK PW RET.CLK INM.						
	CLK M						
2	3 05,07,08	0.1uf	CC0402	C1005X5R1A104K	CAP CER 0.1UF 10V 10% X5R 0402	TDK Corporation	
m.	3 C20,C21,C22	Int	CC0402	C1005X5R1A105K	CAP CER 1UF 10V 10% X5R 0402	TDK Corporation	
4	2 C24 C25	10uf	C3216.A	T494A106M020AT	CAP TANT 10UF 20V 20% 1205	Kemet	Component Reference-305-PD-13-1158
10	32 C30, C31, C32, C33, C34, C35,	2pF	CC0402	C1005C0G1H020C	CAP CER 2PF 50V NP0 0402	TDK Corporation	
+	C36, C37, C38, C39, C40, C41,						
	C42, C43, C44, C45, C46, C47,						
+	C48, C49, C50, C51, C52, C53,						
+	U24, U25, U26, U37, U28, U50,						
+	051,C62		· · · · · · · · · · · · · · · · · · ·	100 100 100	· · · · · · · · · · · · · · · · · · ·		And the second of the second
0	1 HBW BYPASS LBW	HEADER 4 1	BERGER	P/COUSSABIN	COMN READER 100 SINGL STR 4POS	Sullins Connector Solutions	Component Reference 305-PD-13-1156
	2 JJ34, J35	1714955	1714955	1/14955	CONN TERM BLOCK 2POS 6.35MM PCB	Phoenix Contact	
	4 L1,L2,L3,L4	BLM1580221SN1D	10402	BUM16BDZ21SN1D	FERRITE CHIP 220 CHM 300MA 0402	Murata Electronics North America	A 410 AU 410 AU
d)	11 SCLK SDATA1.0E 1#.0E 2#.	HEADER 3	BERGJP	PZC03SABN	CONN HEADER . 100 SINGL STR 3POS	Sullins	Component Reference-305-PD-13-1158
+	OE 3#, OE 4#, OE 5#, OE 6#,						
+	OE 7#,100-133M#.						
	PWRG PWRDN# OE 0#						
10	2 PAD1 PAD2	DAD	DAD				NOT A PART
	15 R1, R2, R3, R4, R5, R6, R7, R8,	10K	RC0402	RC0402JR-0710KL	RES 10K OHM 1/16W 5% 0402 SMD	Yageo	
+	R9,R10,R11,R12,R13,R26,						
	KU	1000	2.04.140		PRES 110 DITE TRUE TO DITE		
21	Z K14,K15	H42H	HCU4UZ	FORCEORDZF1442K	HES 442 OHM 1/16W 1% 0402	Stackpole Electronics Inc	
13	32 H15 H17 H18 H24 H25 H26	33K	RC0402	EKU-ZKKF33R0X	HES 33.0 OHM 1/10W 1% 0402 SMD	Panasone - ECG	
+	R30,R31,R33,R34,R36,R37,						
+	R39, R40, R42, R43, R45, R45,						
+	R48,R49,R51,R52,R54,R55,						
	R57,R58,R50,R61,R67,R68,						
-	R71,R72		0.000.000	PLANA IN A PART	DEC & A SUM AND AND AND		
14	13 K13, KZ2, KZ3, KZ3, K32, K35, K35,	2	HCC040Z	KCU4UZUK-UTUHQ.	HES U.U. OHM T/16W 04UZ SMU	7 ageo	
-	DAG DAS DAS DAS DAS DAS DAS DAS						
	R74						
15	2 R20.R21	5040	RC0402	RC0402FR-0749K9L	RES 49.9K OHM 1/16W 1% 0402 SMD	Yaoeo	
16	5 TP1 TP2 TP3 TP4 TP5	T POINT B	TP	5001	TEST POINT PC MINI 040'D BLACK	Keystone Electronics	Component Reference 305-PD-13-1158
17	16 TP6, TP7, TP8, TP9, TP10.	T POINT B	TESTPOINT				NOT A PART
	TP11.TP12.TP13.TP14.TP15.						
	TP16.TP17.TP18.TP19.TP20,						
	TP21						
18	101	SI53108-AD1AGM	480FN				CUSTOMER PART
10	16 VIA1#, VIA1, VIA2#, VIA2	DI GND VIA	DI GND VIA				NOT A PART
+	VIA3#, VIA3, VIA4#, VIA4						
	MAS#, VIAS, VIA6#, VIA6,						
	VIA7#, VIA7, VIA0#, VIA0				The second residence and the second se		





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