LB11852FV

ON Semiconductor®

www.onsemi.com

Monolithic Digital IC

For Fan Motor

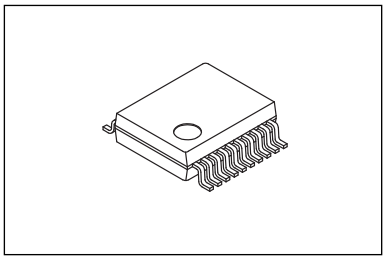
Single-phase Full-wave Pre-driver with Speed Control Function

Overview

The LB11852FV is a single-phase bipolar driving motor pre-driver with a speed control function based on speed feedback. With a small number of external parts, a highly efficient and very quiet variable-speed drive fan motor with low power consumption and high rotational accuracy can be implemented. The LB11852FV, integrated in a miniature package, is best suited for driving small fan motors requiring speed control.

Features

- Single-phase full-wave driving pre-driver
  ⇒ With a PMOS-NMOS device used as the external power transistor, low saturation output and a single-phase full-wave drive enable a high-efficiency drive with low power consumption.
- Speed control circuit incorporated
  ⇒ Compared with open-loop control, a closed-loop control function that uses speed feedback to control the speed makes it possible to improve the rotational speed accuracy and reduce the variations in the rotational speed caused by fluctuations in the supply voltage or load. The separately excited upper direct PWM method is featured as the variable speed system.
- Variable speed control is possible with external PWM input or analog voltage input
  ⇒ The speed control input signal is compatible with PWM duty ratio and analog voltages.
- Soft start circuit incorporated
- Minimum speed setting pin
  ⇒ The minimum speed can be set using an external resistor.
- Current limiting circuit incorporated
  ⇒ Chopper type current limit at startup or lock.
- Reactive current cut circuit incorporated
  ⇒ Reactive current before phase changeover is cut, ensuring highly silent and low power-consumption drive.
- Automatic resetting type constraint circuit incorporated
- FG (rotational speed detection) output



SSOP20J (225 mil)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} pin maximum supply voltage	V_{CC} max		18	V
OUTN pin maximum output current	IOUTN max		20	mA
OUTP pin maximum Sink current	IOUTP max		20	mA
OUT pin output withstand voltage	VOUT max		18	V
CTL, C pin withstand voltage	CTL, C max		7	V
LIM pin withstand voltage	LIM max		7	V
FG output pin output withstand voltage	FG max		19	V
FG output current	FG max		10	mA
5VREG pin maximum output current	I5VREG max		10	mA
Allowable power dissipation	Pd max	Mounted on a specified board *1	0.8	W
Operating temperature	Topr		-30 to 95	°C
Storage temperature	Tstg		-55 to 150	°C

*1 Mounted on a specified board : 114.3mm×76.1mm×1.6mm, glass epoxy

*2 Tj max = 150°C. Use the device in a condition that the chip temperature does not exceed Tj = 150°C during operation.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{CC} supply voltage 1	$V_{CC}1$	V_{CC} pin	5.5 to 16	V
V_{CC} supply voltage 2	$V_{CC}2$	V_{CC} -5VREG	4.5 to 5.5	V
CTL input voltage range	VCTL		0 to 5VREG	V
LIM input voltage range	VLIM		0 to 5VREG	V
Hall input common phase input voltage range	VICM		0.2 to 3	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V, unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	$I_{CC}1$	During drive		12	15	mA
	$I_{CC}2$	During lock protection		12	15	mA
5VREG voltage	5VREG	I5VREG = 5mA	4.8	5.0	5.2	V
Current limiting voltage	VLIM		190	210	230	mV
CPWM pin H level voltage	$V_{CR}H$		2.8	3.0	3.2	V
CPWM pin L level voltage	$V_{CR}L$		0.9	1.1	1.3	V
CPWM pin charge current	$I_{CPWM}1$	V_{CPWM} = 0.5V	24	30	36	μA
CPWM pin discharge current	$I_{CPWM}2$	V_{CPWM} = 3.5V	21	27	33	μA
CPWM oscillation frequency	F_{PWM}	C = 220pF		30		kHz
CT pin H level voltage	$V_{CT}H$		2.8	3.0	3.2	V
CT pin L level voltage	$V_{CT}L$		0.9	1.1	1.3	V
CT pin charge current	$I_{CT}1$	V_{CT} = 2V	1.6	2.0	2.5	μA
CT pin discharge current	$I_{CT}2$	V_{CT} = 2V	0.16	0.20	0.25	μA
CT pin charge/discharge current ratio	R_{CT}	$I_{CT}1/I_{CT}2$	8	10	12	times
OUTN pin output H voltage	V_ONH	I_O = 10mA		V_{CC}-0.85	V_{CC}-1.0	V
OUTN pin output L voltage	V_ONL	I_O = 10mA		0.9	1.0	V
OUTP pin output L voltage	V_OPL	I_O = 10mA		0.5	0.65	V
Hall input sensitivity	VHN	IN^+, IN^- differential voltage (including offset and hysteresis)		±15	±25	mV

Continued on next page.

Continued from preceding page.

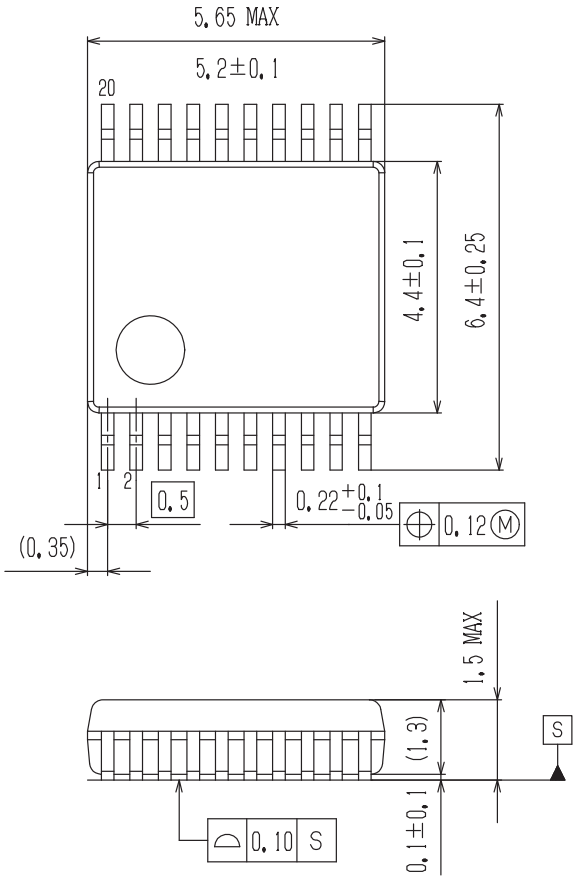
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FG output L voltage	$V_{FG}L$	I_{FG} = 5mA		0.15	0.30	V
FG pin leak current	$I_{FG}L$	V_{FG} = 19V			30	μA
EO pin output H voltage	$V_{EO}H$	$I_{EO}1$ = -0.2mA	VREG-1.2	VREG-0.8		V
EO pin output L voltage	$V_{EO}L$	$I_{EO}1$ = 0.2mA		0.8	1.1	V
RC pin output H voltage	$V_{RC}H$		3.2	3.45	3.7	V
RC pin output L voltage	$V_{RC}L$		0.7	0.8	1.05	V
RC pin clamp voltage	$V_{RC}CLP$		1.3	1.5	1.7	V
CTL pin input H voltage	$V_{CTL}H$		2.0		VREG	V
CTL pin input L voltage	$V_{CTL}L$		0		1.0	V
CTL pin input open voltage	$V_{CTL}O$		VREG-0.5		VREG	V
CTL pin H input H current	$I_{CTL}H$	V_{FG}IN = 5VREG	-10	0	10	μA
CTL pin L input L current	$I_{CTL}L$	V_{FG}IN = 0V	-120	-90		μA
C pin output H voltage	$V_C H$		VREG-0.3	VREG-0.1		V
C pin output L voltage	$V_C L$		1.8	2.0	2.2	V
LIM pin input bias current	I_BLIM		-1		1	μA
LIM pin common phase input voltage range	V_ILIM		2.0		VREG	V
SOFT pin charge current	I_CSOFT		1.0	1.3	1.6	μA
SOFT pin operating voltage range	V_ISOFT		2.0		VREG	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

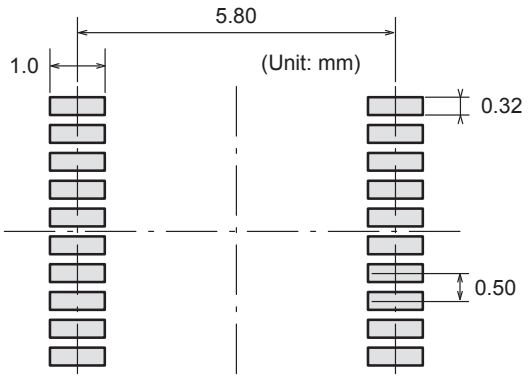
Package Dimensions

unit : mm

SSOP20J (225mil)
CASE 565AP
ISSUE A



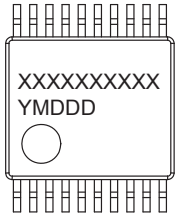
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

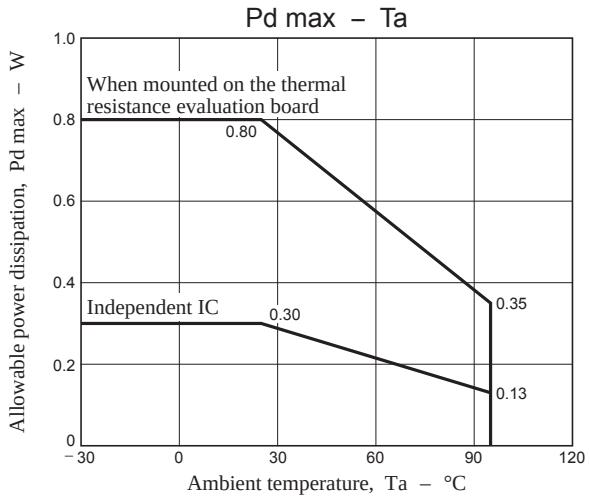
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.



Truth table

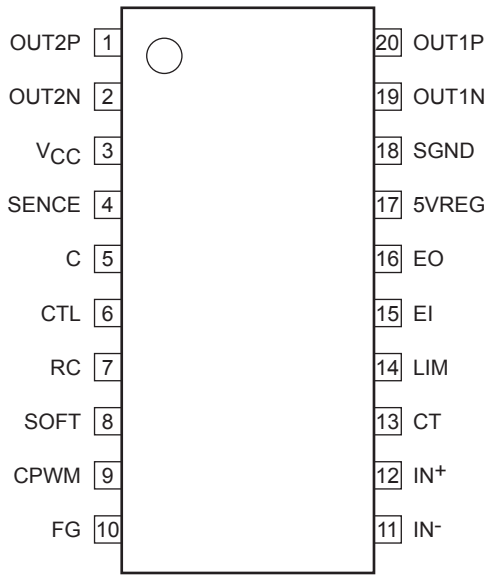
Lock protection CPWM = H

IN-	IN+	CT	OUT1P	OUT1N	OUT2P	OUT2N	FG	Mode
H	L	L	L	L	OFF	H	L	OUT1 → 2 drive
L	H		OFF	H	L	L	OFF	OUT2 → 1 drive
H	L	H	OFF	L	OFF	H	L	Lock protection
L	H		OFF	H	OFF	L	OFF	

Speed control CT = L

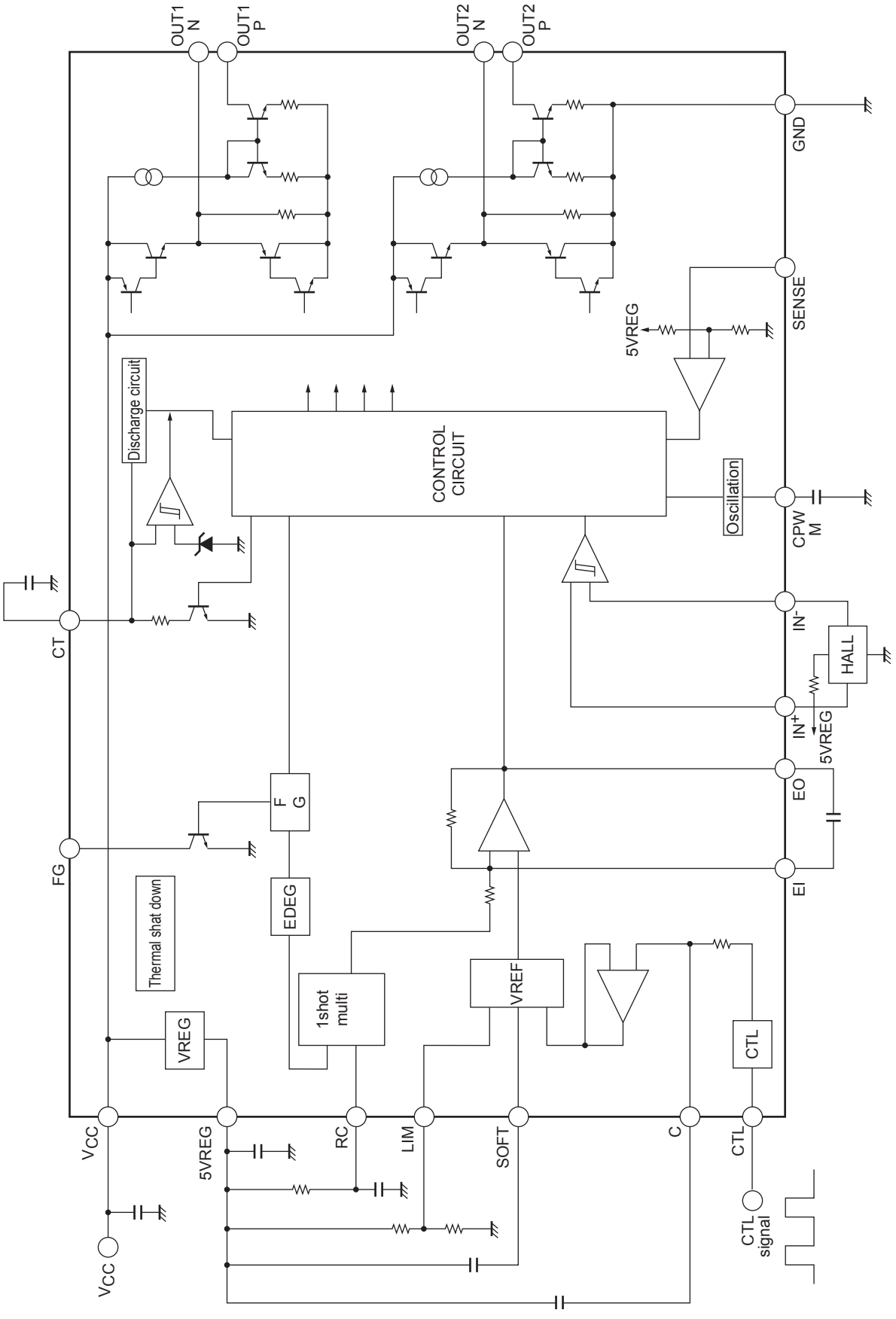
EO	CPWM	IN-	IN+	OUT1P	OUT1N	OUT2P	OUT2N	Mode
L	H	H	L	L	L	OFF	H	OUT1 → 2 drive
		L	H	OFF	H	L	L	OUT2 → 1 drive
H	L	H	L	OFF	L	OFF	H	Regeneration mode
		L	H	OFF	H	OFF	L	

Pin Assignment

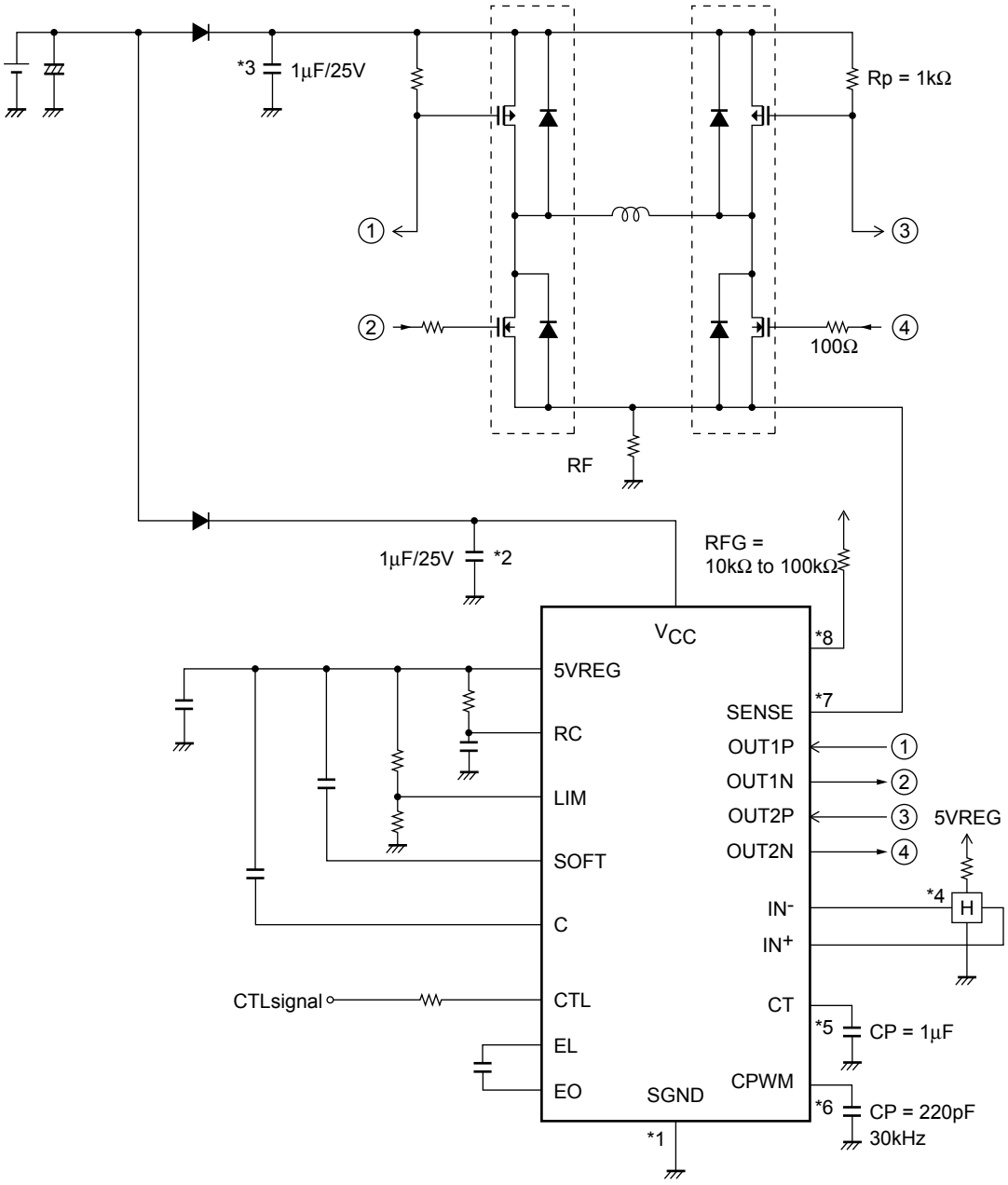


Top view

Block Diagram



Sample Application Circuit



Description of Pre-driver Bock

*1 : Power-GND wiring

The SGND is connected to the control circuit power supply system.

*2 : Power stabilization capacitor

For the power stabilization capacitor on the signal side, use a capacitor of 0.1μF or more. Connect the capacitor between V_{CC} and GND with a thick and along the shortest possible route.

*3 : Power-side power stabilization capacitor

For the power-side power stabilization capacitor, use a capacitor of 1μF or more. Connect the capacitor between the power-side power supply and GND with a thick and along the shortest possible route.

*4 : IN^+, IN^- pins

Hall signal input pins
Wiring should be short to prevent noise from being carried.
If noise is carried, insert a capacitor between the IN^+ and IN^- pins.
The Hall input circuit functions as a comparator with hysteresis (15mV).
It also has a soft switch zone with ±30mV (input signal difference voltage).
It is also recommended that the Hall input level should be a minimum of 100mV (p-p).

*5 : CPWM pin

Pin to connect the capacitor used to generate the PWM basic frequency
Use of CP = 200pF causes oscillation at f = 30kHz, which is the basic frequency of PWM.
As this is also used for the current limiter reset signal, a capacitor must be connected even if the speed is not going to be controlled.

*6 : CT pin

Pin to connect the capacitor used for lock detection
The constant-current charging and constant-current discharging circuits incorporated cause locking when the pin voltage reaches 3.0V, and releasing the lock protection when it drops to 1.0V.
Connect this pin to the GND when it is not to be used (locking not necessary).

*7 : SENSE pin

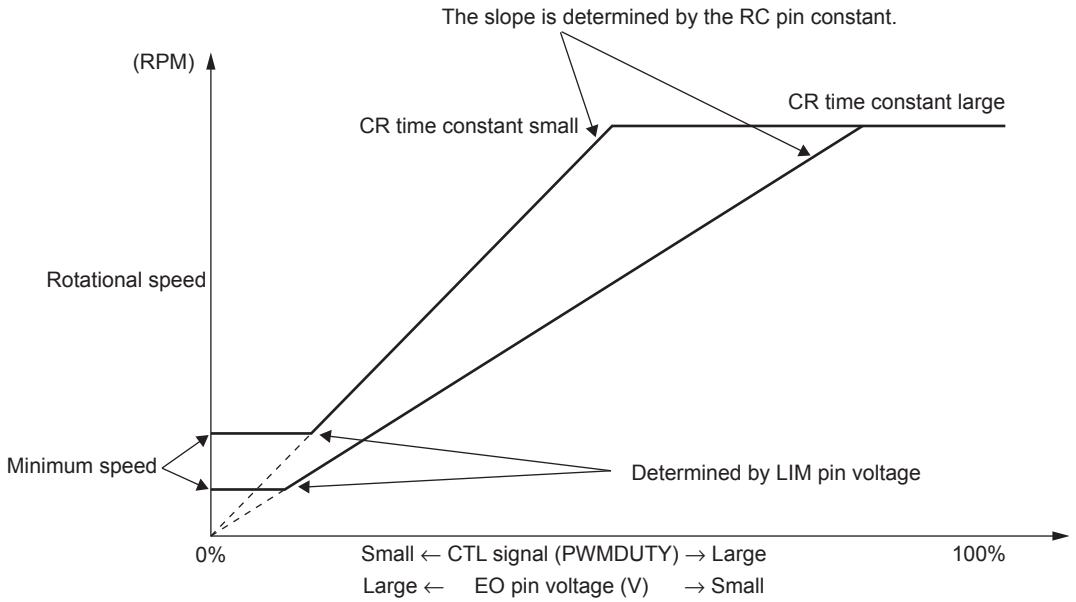
Current limiter detection pin
When the pin voltage exceeds 0.21V, the current limiter is activated, and operation enters lower regeneration mode.
Connect this pin to the GND when it is not to be used.

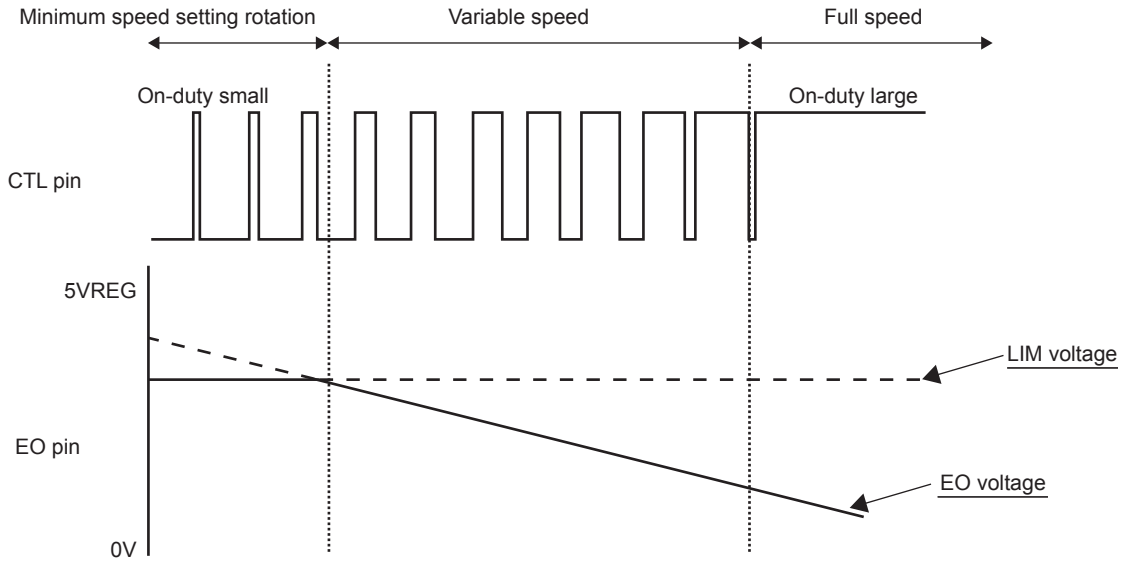
*8 : FG pin

Rotational speed detection pin
This is an open collector output that can detect the rotational speed using the FG output corresponding to the phase changeover.
Keep this pin open when it is not to be used.

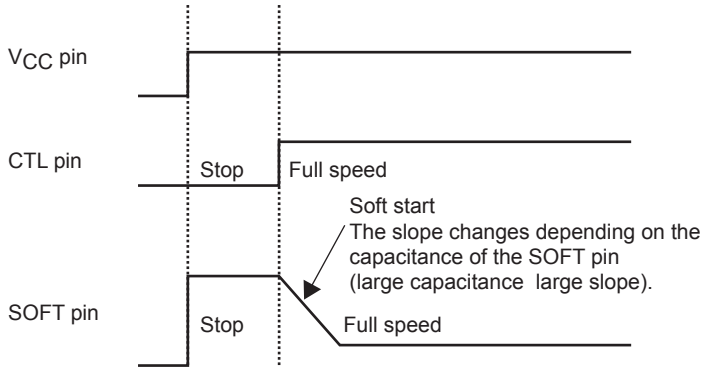
Description of Speed Control Block

1. Speed control diagram



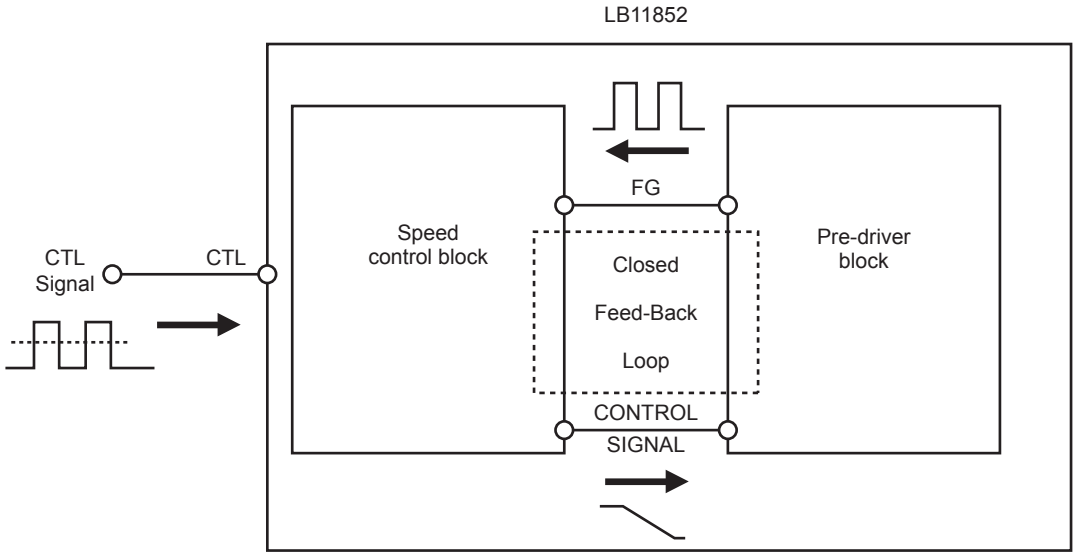


2. Timing at startup (soft start)

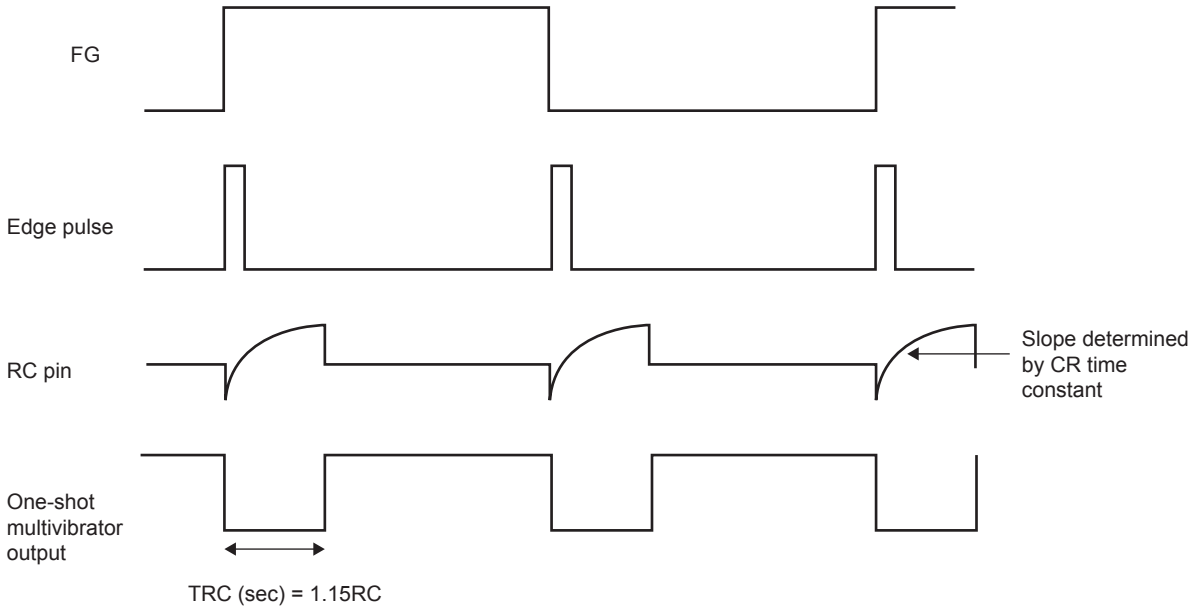


2. Supplementary description of operations

By inputting the duty pulses, a feedback loop is formed inside the LB11852 IC to establish the FG period (rotational speed of the motor) that corresponds to the control voltage of the pulses.



The operation inside the IC is as flows. pulse signals are created from the edges of the FG signals as shown in the figure below, and using these signals as a reference, waveforms with a pulse width determined by the CR time constant are generated using a one-shot multivibrator. These pulse waveforms are then integrated to control the duty ratio of the pre-driver output as the control voltage.



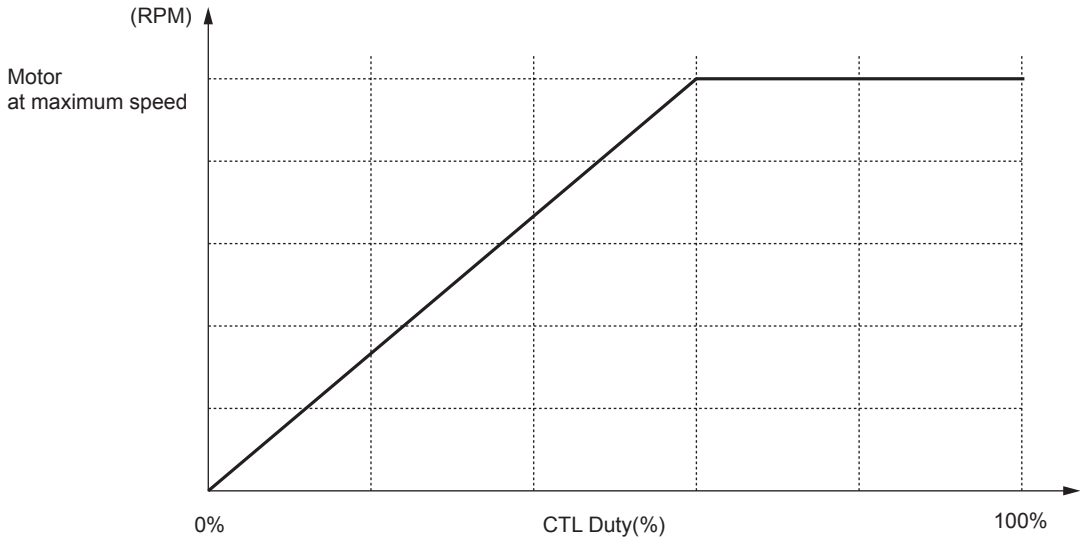
By changing the pulse width as determined by the CR time constant, the VCTL versus rotational speed slope can be adjusted as shown in the speed control diagram in the previous section.

However, since pulses that are determined by the CR time constant are used, the CR variations are output as-is as the speed control error.

4. Procedure for calculating the constant

〈RC pin〉

The slope shown in the speed control diagram is determined by the constant of the RC pin.



1) Obtain the FG signal frequency fFG (Hz) at the maximum rotational speed of the motor (with two FG pulses per rotation).

$fFG\ (Hz) = 2\ rpm/60 \cdots (1)$

2) Obtain the time constant of the components connected to the RC pin (use the duty ratio (example : 100% = 1.0 or 60% = 0.6) as the CTL duty ratio for achieving the maximum rotational speed).

$R \times C = Duty\ ratio/ (3.3 \times 1.1 \times fFG) \cdots (2)$

3) Obtain the resistance and the capacitance of the capacitor.

Based on the discharge capability of the RC pin, the capacitance of the capacitor which can be used is in the range of 0.01μF to 0.015μF.

Therefore, obtain the appropriate resistance from the result of (2) above using the formula in (3) or (4) below.

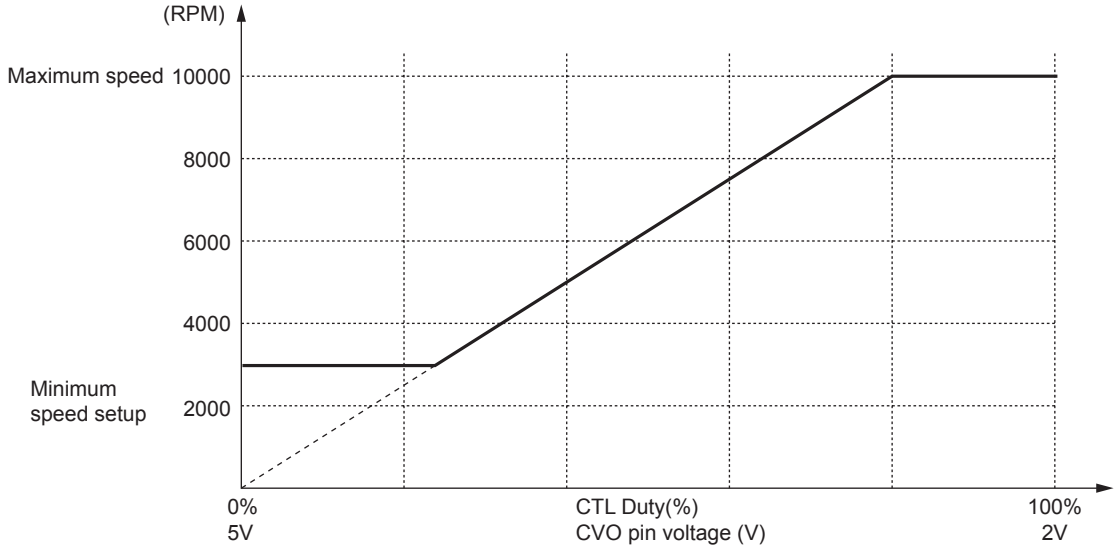
$R = (R \times C)/0.01\mu F \cdots (3)$

$R = (R \times C)/0.015\mu F \cdots (4)$

The temperature characteristics of the curve are determined by the temperature characteristics of the capacitor of the RC pin. To minimize the variations in the rotational speed caused by temperature, a capacitor with excellent temperature characteristics must be used.

〈LIM pin〉

The minimum speed is determined by the voltage of the LIM pin.

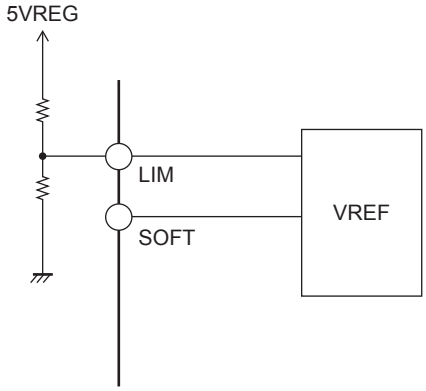


1) Obtain the ratio of the minimum speed required to the maximum speed.
   Ra = Minimum/maximum speed ⋯ (1)
   In the example shown in the figure above : Ra = minimum/maximum speed = 3000/10000 = 0.3

2) Obtain the product of the duty ratio at which the maximum speed is achieved and the value in formula (1).
   Ca = Maximum speed duty ratio × Ra ⋯ (2)
   In the example given : Ca = maximum speed duty ratio × Ra = 0.8 × 0.3 = 0.24

3) Obtain the required LIM pin voltage.
   LIM = 5 - (3 × Ca) ⋯ (3)
   In the example given : LIM = 5 - (3 × Ca) = 5 - (3 × 0.24) ≈ 4.3V

4) Divide the resistance of 5VREG to generate the LIM voltage.
   In the example given, the voltage is 4.3V so the resistance ratio is 1 : 6.
   The resistance is 10kΩ between 5VREG and LIM and 62kΩ between LIM and GND.

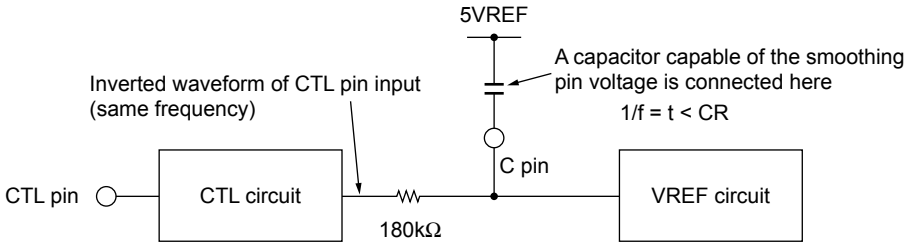


〈C pin〉

In order to connect a capacitor capable of smoothing the pin voltage to the C pin, the correlation given in the following equation must be satisfied when f (Hz) serves as the input frequency of the CTL pin. (R is incorporated inside the IC, and it is 180kΩ (typ.).)

$1/f = t < CR$

The higher the capacitance of the capacitor, the slower the response to changes in the input signals.



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LB11852FV-TLM-H	SSOP20J (225mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel
LB11852FV-TLM-E	SSOP20J (225mil) (Pb-Free)	2000 / Tape & Reel
LB11852FV-W-AH	SSOP20J (225mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF