High Speed, 10 GHz Window Comparator

Data Sheet

HMC974LC3C

FEATURES

Propagation delay: 88 ps
Propagation delay at 50 mV overdrive: 20 ps
Minimum detectable pulse width: 60 ps
Differential latch control
Power dissipation: 240 mW
16-terminal 2.9 mm × 2.9 mm LCC package

APPLICATIONS

Automatic test equipment (ATE)
High speed instrumentation
Clock and data restoration
Semiconductor test systems
Threshold detection in electronic warfare systems

FUNCTIONAL BLOCK DIAGRAM

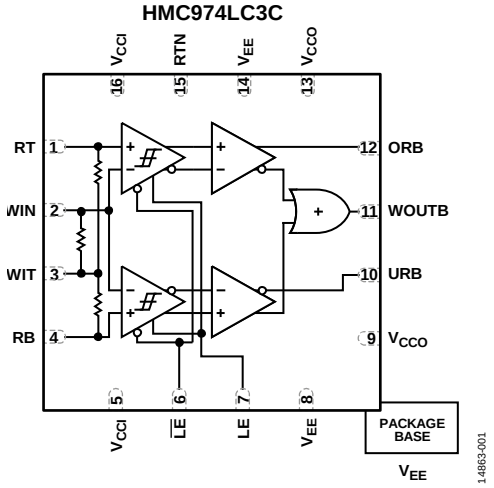


Figure 1.

GENERAL DESCRIPTION

The HMC974LC3C is a silicon germanium (SiGe) monolithic, ultra fast window comparator that features reduced swing positive emitter-coupled logic (RSPECL) output drivers that are level latched. Three output ports detect whether an analog input signal is above, below, or between two reference levels supplied at the input (see Figure 2).

The outputs are single-ended negative logic. Incorporating two proven comparators at the input provides good dc and dynamic matching and reduces the input capacitance. The reduced swing output stages are designed to directly drive 400 mV into 50 Ω terminated to a voltage ($V_{TERM} = V_{CCO} - 2$ V).

HMC974LC3C features high speed latches that can either be enabled to latch the output data or left in the track mode to implement a tracking window comparator.

Rev. C **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **Technical Support**

www.analog.com

HMC974* PRODUCT PAGE QUICK LINKS

Last Content Update: 03/25/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC974LC3C Evaluation Board

DOCUMENTATION

Data Sheet

- HMC974: High Speed, 10 GHz Window Comparator Data Sheet

REFERENCE MATERIALS

Quality Documentation

- Package/Assembly Qualification Test Report: LC3, LC3B, LC3C (QTR: 2014-00376 REV: 01)
- Semiconductor Qualification Test Report: BiCMOS-C (QTR: 2013-00241)

DESIGN RESOURCES

- HMC974 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC974 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

3/2017—v04.0616 to Rev. C

Updated Format ..... Universal
Changes to General Description 1
Changes to Table 1 3
Added Negative Supply (V_{EE} to GND) Parameter, Table 2 5
Changes to Table 3 5
Added Theory of Operation Section, Power Sequencing Section, and Table 4 9
Added Applications Information Section
Changes to Evaluation Board Section and Table 5 10
Updated Outline Dimensions 12
Changes to Ordering Guide 12

SPECIFICATIONS

T_A = +25 °C, V_{EE} = −3 V, V_{CCI} = +3.3 V, V_{CCO} = +2 V, V_{TERM} = 0 V, V_{CM} = 0 V, V_{OD}[1] = 50 mV.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC INPUT CHARACTERISTICS					
Offset Voltage	−10	±4	+10	mV	
Bias Current	−30	+20	+30	µA	WIT pin termination open
Differential Voltage	−2		+2	V	Measured between the WIN pin voltage and the RT pin voltage or RB pin voltage
Input Impedance					
WIN pin to WIT pin		50		Ω	
RT pin to WIT pin		50		Ω	
RB pin to WIT pin		50		Ω	
Common Mode Input Voltage Range	−1.5		+1.5	V	WIT to GND
Input Capacitance			1	pF	
LATCH ENABLE CHARACTERISTICS					
LE and $\overline{LE}$					
Input Low Voltage (V_{IL})			1.6	V	
Input High Voltage (V_{IH})	2.2			V	
LE and $\overline{LE}$ Impedance		7.8		kΩ	If not driven, the device is unlatched
DC OUTPUT CHARACTERISTICS					
Output Voltage					
High Level, V_{OH} (50 Ω to 0 V)		1.06		V	
Low Level, V_{OL} (50 Ω to 0 V		0.73		V	
Output Voltage Swing	320	365	410	mV	
AC PERFORMANCE					
Propagation Delay Dispersion vs. V_{OD}		20		ps	For V_{OD} > 50 mV
Rise Time (ORB, WOUTB, URB), t_R		25.3		ps	20% to 80%
Fall Time (ORB, WOUTB, URB), t_F		21.9		ps	80% to 20%
Minimum Detectable Pulse Width		60		ps	V_{CM} = 0 V; ±100 mV overdrive voltage
Equivalent Input Bandwidth[2]		11		GHz	
Input to Output Delay, t_{PD}		88		ps	
Latch to Output Delay, t_{PD}		83		ps	
Maximum Input Slew Rate		5		V/ns	
Noise (Referred to Input)		6		nV/ √(Hz)	
Random Jitter (rms)		0.2		ps rms	At 5 Gbps with ±100 mV overdrive
Deterministic Jitter (Peak-to-Peak)		2		ps	At 5 Gbps with ±100 mV overdrive
POWER SUPPLIES (INCLUDING LOAD)					
Positive Supply Voltage Input Stage (V_{CCI})	3.135	3.3	3.465	V	
Positive Supply Voltage Output Stage (V_{CCO})	1.8	3.3	3.465	V	
Negative Power Supply (V_{EE})	−3.15	−3.0	−2.85	V	
Positive Supply Current Input Stage (I_{CCI})	13.4	14.9	16.5	mA	
Positive Supply Current Output Stage (I_{CCO})	70	72.3	79.6	mA	
Negative Current (I_{EE})	28.3	29.9	31.6	mA	
Power Disipation (P_D)		240		mW	

[1] V_{OD} is the input overdrive voltage, for example, $V_{WIN} - V_{RT} = V_{OD}$ or $V_{WIN} - V_{RB} = V_{OD}$.

[2] Equivalent input bandwidth is calculated with the following formula: $B_{WEQ} = 0.22/\sqrt{(TR_{COMP}^2 - TR_{IN}^2)}$, where B_{WEQ} is the equivalent bandwidth formula, TR_{IN} is the 20% to 80% transition time of a quasi Gaussian signal applied to the comparator input, and TR_{COMP} is the effective transition time digitized by the comparator.

TIMING DIAGRAM

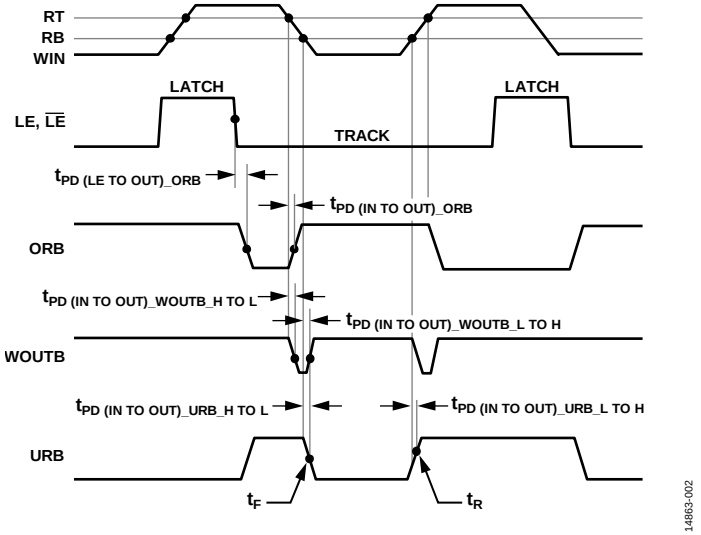


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Input Supply Voltage (V_{CCI} to GND)	−0.5 V to +4 V
Output Supply Voltage (V_{CCO} to GND)	−0.5 V to +4 V
Positive Supply Differential ($V_{CCI} - V_{CCO}$)	−0.5 V to +3 V
Negative Supply (V_{EE} to GND)	−3.3 V to +0.5 V
Input Voltage	−2 V to +2 V
Differential Input Voltage	−2 V to +2 V
Output Current	40 mA
Junction Temperature	125°C
Continuous Power Dissipation (T = 85°C; derate 20.4 mW/°C above 85°C)	0.816 W
Thermal Resistance (θ_{JC})	49 °C/W
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
ESD Sensitivity (HBM)	Class 1B

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

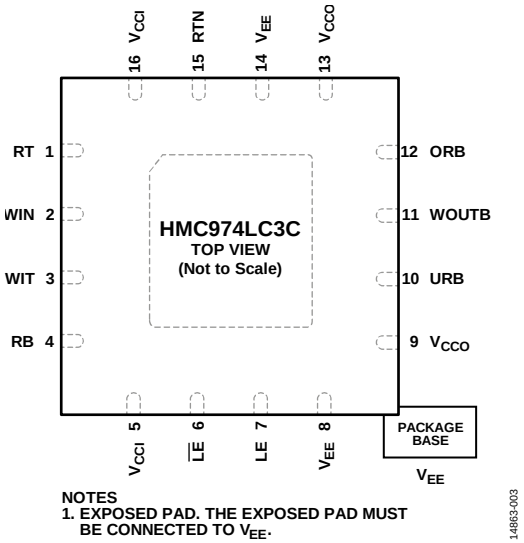


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RT	Termination Resistor for Reference Top.
2	WIN	Analog Input Window.
3	WIT	Common Mode Window for Termination Resistors.
4	RB	Termination Resistor Return for Reference Bottom.
5, 16	V_{CCI}	Positive Supply Voltage Input Stage.
6	$\overline{LE}$	Inverting Latch Enable Input.
7	LE	Noninverting Latch Enable Input.
8, 14	V_{EE}	Negative Power Supply
9, 13	V_{CCO}	Positive Supply Voltage Output Stage.
10	URB	Underange Output. URB is asserted low when the analog input voltage is below the RB pin voltage.
11	WOUTB	Window Output. WOUTB is asserted low when the analog input voltage is between the RB pin voltage and the RT pin voltage.
12	ORB	Overrange output. ORB is asserted low when the analog input voltage range is above the RT pin voltage.
15	RTN	ESD Protection Return.
	EPAD	Exposed Pad. The exposed pad must be connected to V_{EE}.

INTERFACE SCHEMATICS

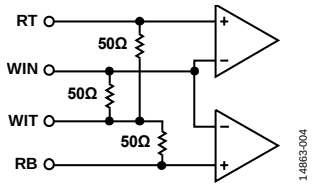


Figure 4. Interface Schematic for RT, RB, WIN, and WIT

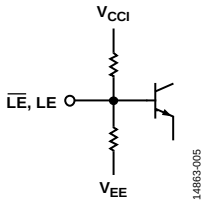


Figure 5. Interface Schematic for LE and $\overline{LE}$

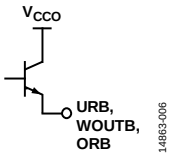


Figure 6. Interface Schematic for URB, WOUTB, and ORB

TYPICAL PERFORMANCE CHARACTERISTICS

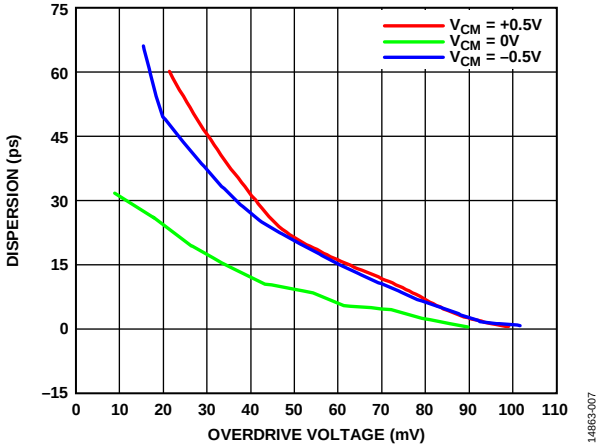


Figure 7. Dispersion vs. Overdrive Voltage

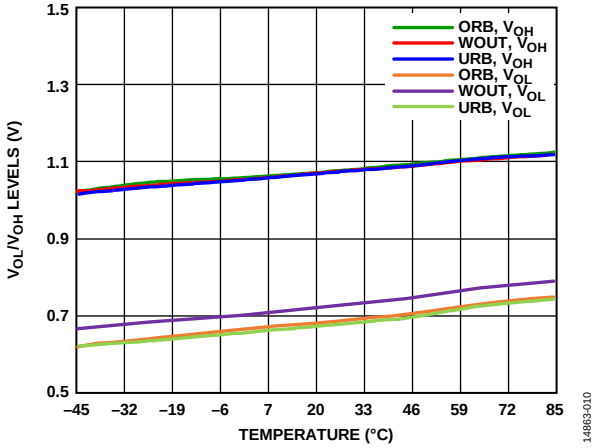


Figure 10. V_{OL}/V_{OH} Levels vs. Temperature

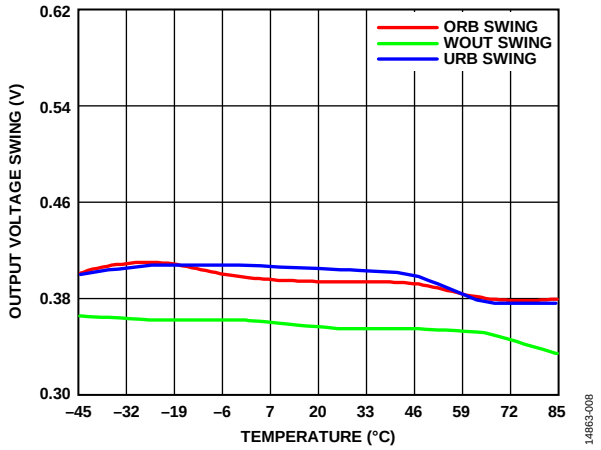
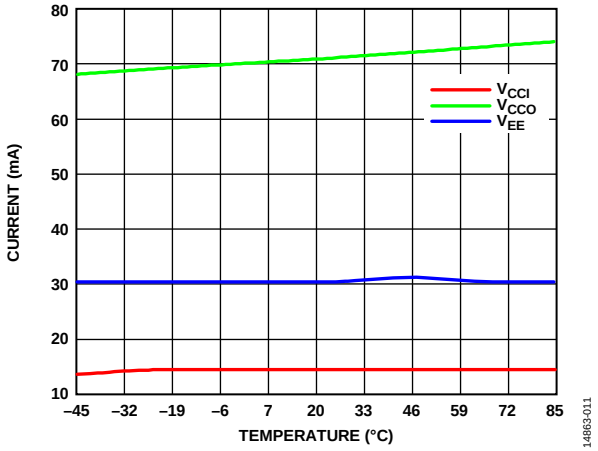


Figure 8. Output Voltage Swing vs. Temperature



0Figure 11. Power Supply Currents

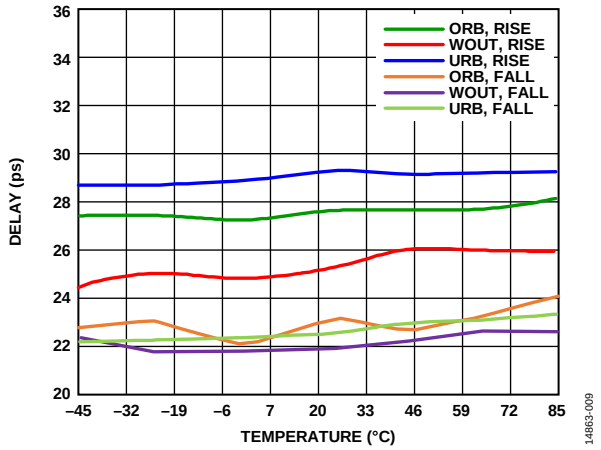


Figure 9. Output Rise and Fall Time

THEORY OF OPERATION

The HMC974LC3C is a window comparator where the range of the window is defined with RT as the top of the voltage window range and RB as the bottom of the voltage window range. The comparator has two modes of operation: track mode and latch mode. While in track mode, the comparator determines three things:

1. If the signal is below the window voltage value, RT, and above the window voltage value, RB, represented by the WOUTB output.
2. If the signal is above the window voltage value RT, which is represented by the ORB output.
3. If the signal is below the window voltage value RB, which is represented by the URB output.

A typical 5 Gbps output eye is shown in Figure 12 with specific details outlined in Table 4.

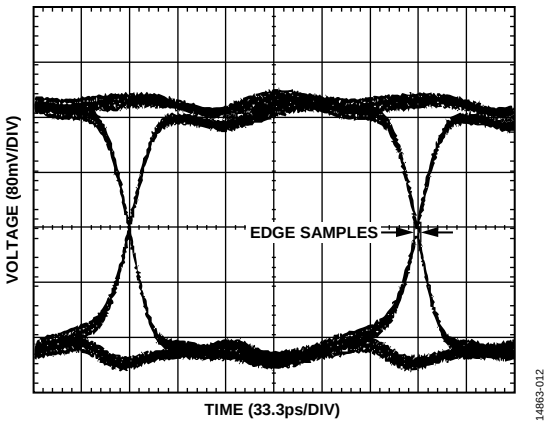


Figure 12. Eye Diagram at 5 Gbps

Table 4. Eye Diagram Details

Parameter	Value
Bit Rate	5 Gbps
Pattern Length	$2^{15} - 1$
Deterministic Jitter (Peak-to-Peak)	2.15 ps
Vertical Scale	80 mV/div
Time Scale	33.3 ps/div

POWER SEQUENCING

Use the following supplies sequentially to power up the device:

1. V_{EE}
2. V_{CCI} and V_{CCO} (if $V_{CCO} = V_{CCI}$)
3. V_{CCO} (if different than ground)

The power-down sequence is the reverse of the previous sequence:

1. V_{CCO} (if different than ground)
2. V_{CCI} and V_{CCO} (if $V_{CCO} = V_{CCI}$)
3. V_{EE}

Apply power to the HMC974LC3C before applying the input signals (WIN and WIT) and remove the input signals (WIN and WIT) prior to powering it down.

APPLICATIONS INFORMATION

EVALUATION BOARD

The HMC974LC3C evaluation printed circuit board (PCB) must use RF circuit design techniques. Signal lines must have 50 Ω impedance while the package ground leads must connect directly to the ground plane of the PCB. The exposed metal package base must connect to V_{EE}. Ensure the top and bottom ground planes connect together with via holes. The evaluation PCB shown in Figure 13 is available from Analog Devices, Inc., upon request.

Figure 14 shows the EVAL-HMC974LC3C schematic. Figure 15 shows the typical application circuit.

Table 5. Bill of Materials

Reference Designator	Description
J1	Eight-position vertical header
J2 to J7	K connector, SRI
J8	Terminal strip, single row, 3-pin
JP1, JP2	Two position vertical header
C1 to C3, C5, C6, C8 to C10, C15	100 pF capacitor, 0402
C4, C7, C11	330 pF capacitor, 0402
C12 to C14	4.7 µF tantalum capacitor
TP1 to TP4	DC pin
U1	HMC974LC3C window comparator
PCB	EVAL-HMC974LC3C evaluation board, circuit board material is either Rogers 4350 or Arlon 25FR

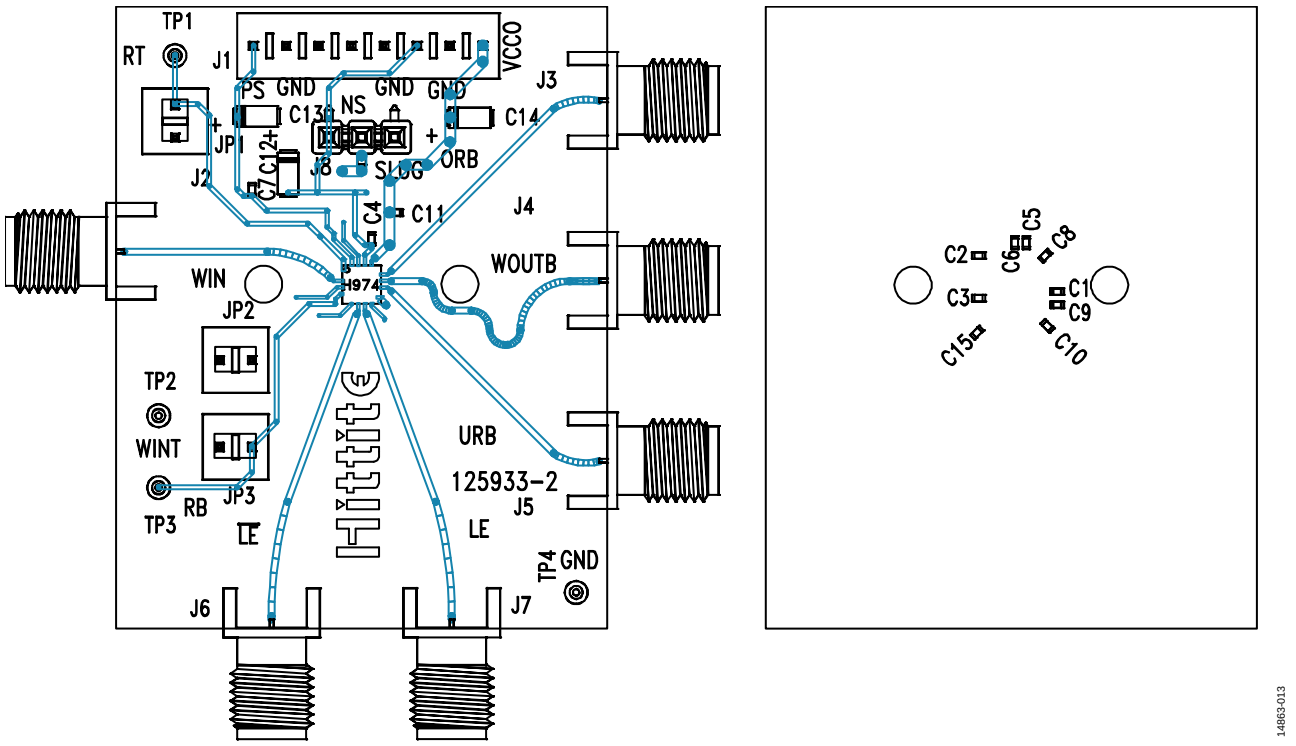


Figure 13. Evaluation Printed Circuit Board

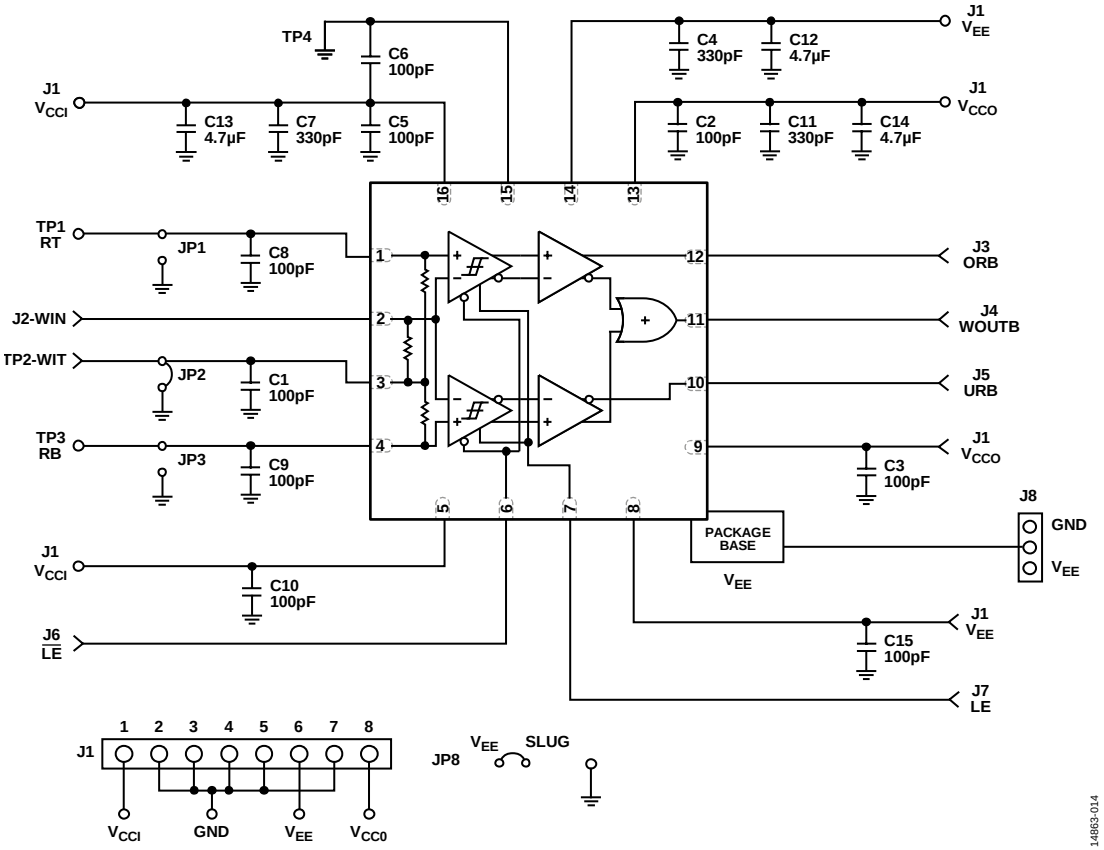


Figure 14. Evaluation Board Schematic

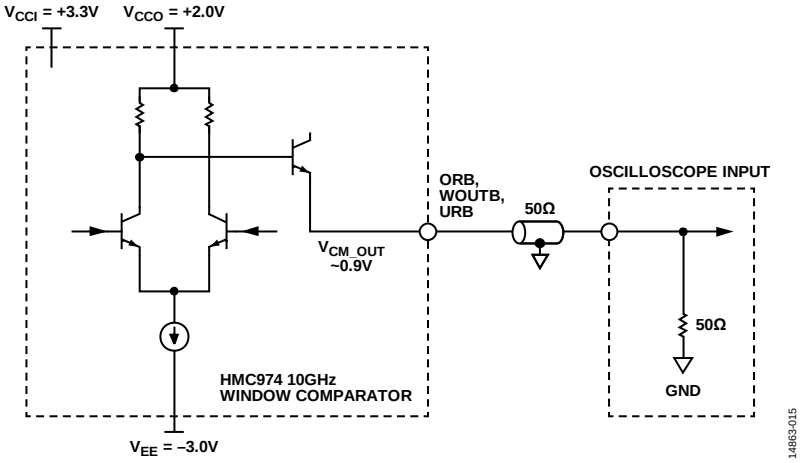


Figure 15. Typical Application Circuit

OUTLINE DIMENSIONS

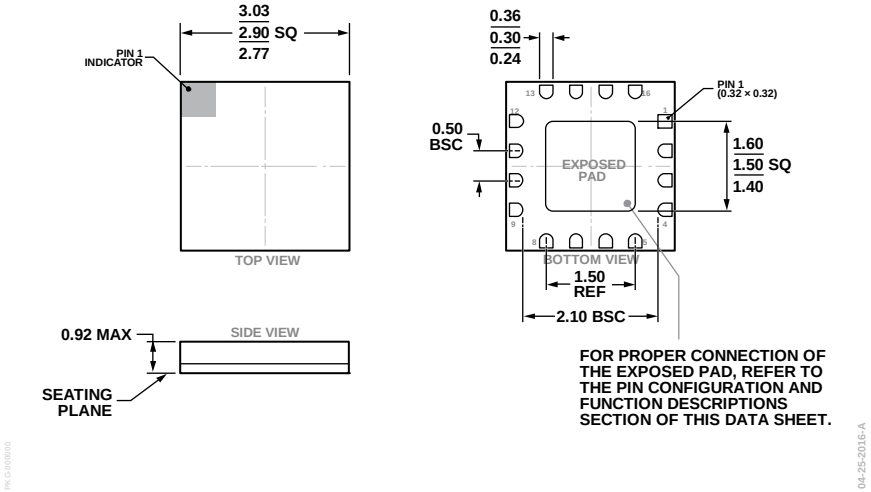


Figure 16. 16-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description[3]	Package Option	Branding
HMC974LC3C	−40°C to +85°C	MSL3	16-Terminal LCC	E-16-1	H974 XXXX
HMC974LC3CTR	−40°C to +85°C	MSL3	16-Terminal LCC	E-16-1	H974 XXXX
HMC974LC3CTR-R5	−40°C to +85°C	MSL3	16-Terminal LCC	E-16-1	H974 XXXX
129538-HMC974LC3C			HMC974LC3C Evaluation Board		

[1] The HMC974LC3C, the HMC974LC3CTR, and the HMC974LC3CTR-R5 are RoHS Compliant Parts.
[2] See the Absolute Maximum Ratings section.
[3] Alumina and white package body material with a gold over nickel lead finish.