

NLSX0102

2-Bit 20 Mb/s Dual-Supply Level Translator

The NLSX0102 is a 2-bit configurable dual-supply bidirectional auto sensing translator that does not require a directional control pin. The I/O V_{CC} and I/O V_L ports are designed to track two different power supply rails, V_{CC} and V_L respectively. Both the V_{CC} and V_L supply rails are configurable from 1.5 V to 5.5 V. This allows voltage logic signals on the V_L side to be translated into lower, higher or equal value voltage logic signals on the V_{CC} side, and vice-versa.

The NLSX0102 translator has integrated 10 k Ω pull-up resistors on the I/O lines. The integrated pull-up resistors are used to pull-up the I/O lines to either V_L or V_{CC} . The NLSX0102 is an excellent match for open-drain applications such as the I²C communication bus.

Features

- V_L can be Less than, Greater than or Equal to V_{CC}
- Wide V_{CC} Operating Range: 1.5 V to 5.5 V
Wide V_L Operating Range: 1.5 V to 5.5 V
- High-Speed with 24 Mb/s Guaranteed Data Rate
- Low Bit-to-Bit Skew
- Enable Input and I/O Pins are Overvoltage Tolerant (OVT) to 5.5 V
- Non-preferential Power-up Sequencing
- Integrated 10 k Ω Pull-up Resistors
- Small Space Saving Package
– 1.9 mm x 0.9 mm x 0.5 mm Flipchip8
- This is a Pb-Free Device

Typical Applications

- I²C, SMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

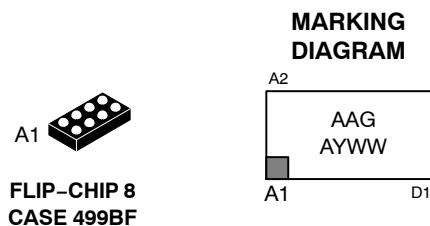
Important Information

- ESD Protection for All Pins
– Human Body Model (HBM) > 7000 V



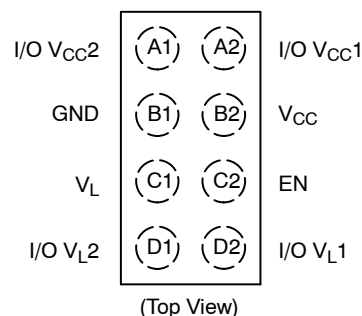
ON Semiconductor®

<http://onsemi.com>

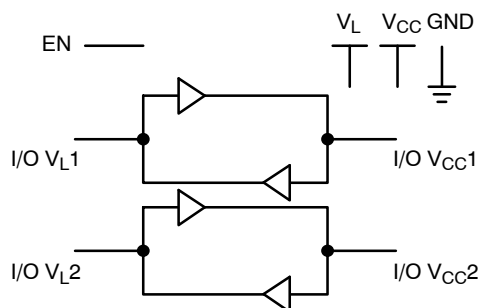


AAG = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENTS



LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NLSX0102

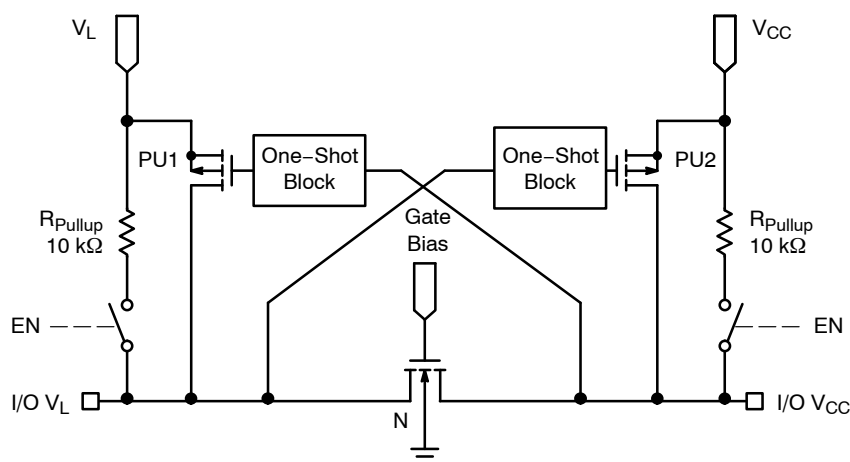


Figure 1. Block Diagram (1 I/O Line)

PIN ASSIGNMENT

| Pins | Description |
|----------------------|---|
| V _{CC} | V _{CC} Supply Voltage |
| V _L | V _L Supply Voltage |
| GND | Ground |
| EN | Output Enable, referenced to V _L |
| I/O V _{CCn} | I/O Port, referenced to V _{CC} |
| I/O V _{Ln} | I/O Port, referenced to V _L |

FUNCTION TABLE

| EN | Operating Mode |
|----|---------------------|
| L | Hi-Z |
| H | I/O Buses Connected |

MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Unit |
|---------------------|---|--------------|----------------------|------|
| V _{CC} | High-side DC Supply Voltage | -0.5 to +7.0 | | V |
| V _L | Low-side DC Supply Voltage | -0.5 to +7.0 | | V |
| I/O V _{CC} | V _{CC} -referenced DC Input / Output Voltage | -0.5 to +7.0 | | V |
| I/O V _L | V _L -referenced DC Input / Output Voltage | -0.5 to +7.0 | | V |
| V _{EN} | Enable Control Pin DC Input Voltage | -0.5 to +7.0 | | V |
| I _{I/O_SC} | Short-Circuit Duration (I/O V _L and I/O V _{CC} to GND) | ±50 | Continuous | mA |
| I _{I/O_K} | Input / Output Clamping Current (I/O V _L and I/O V _{CC}) | -50 | V _{I/O} < 0 | mA |
| T _{STG} | Storage Temperature | -65 to +150 | | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NLSX0102

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-----------------|--|-----|-----|------|
| V _{CC} | High-side Positive DC Supply Voltage | 1.5 | 5.5 | V |
| V _L | Low-side Positive DC Supply Voltage | 1.5 | 5.5 | V |
| V _{EN} | Enable Control Pin Voltage | GND | 5.5 | V |
| V _{IO} | I/O Pin Voltage | GND | 5.5 | V |
| Δt/ΔV | Input Transition Rise and Fall Rate I/O V _L and I/O V _{CC} Ports, Push-Pull Driving | | 10 | ns/V |
| | Control Input | | 10 | |
| T _A | Operating Temperature Range | -40 | +85 | °C |

DC ELECTRICAL CHARACTERISTICS (T_A = -40 to +85 °C, unless otherwise specified)

| Symbol | Parameter | Test Conditions (Note 1) | V _L | V _{CC} | -40 °C to +85 °C | | | Unit |
|---------------------|---|--|----------------|-----------------|-----------------------|---------------------|-----------------------|------|
| | | | | | Min | Typ (Notes 1, 2) | Max | |
| V _{IHC} | I/O V _{CC} Input HIGH Voltage | | 1.5 to 5.5 | 1.5 to 5.5 | V _{CC} - 0.4 | | - | V |
| V _{ILC} | I/O V _{CC} Input LOW Voltage | | 1.5 to 5.5 | 1.5 to 5.5 | | | 0.15 | V |
| V _{IHL} | I/O V _L Input HIGH Voltage | | 1.5 to 5.5 | 1.5 to 5.5 | V _L - 0.4 | | - | V |
| V _{ILL} | I/O V _L Input LOW Voltage | | 1.5 to 5.5 | 1.5 to 5.5 | | | 0.15 | V |
| V _{IH} | Control Pin Input HIGH Voltage | | 1.5 to 5.5 | 1.5 to 5.5 | 0.65 * V _L | | - | V |
| V _{IL} | Control Pin Input LOW Voltage | | 1.5 to 5.5 | 1.5 to 5.5 | | | 0.35 * V _L | V |
| V _{OHC} | I/O V _{CC} Output HIGH Voltage | I/O V _{CC} source current = -20 μA | 1.5 to 5.5 | 1.5 to 5.5 | 2/3 * V _{CC} | | - | V |
| V _{OLC} | I/O V _{CC} Output LOW Voltage | I/O V _{CC} sink current = 1 mA | 1.5 to 5.5 | 1.5 to 5.5 | | | 0.4 | V |
| V _{OHL} | I/O V _L Output HIGH Voltage | I/O V _L source current = -20 μA | 1.5 to 5.5 | 1.5 to 5.5 | 2/3 * V _L | | - | V |
| V _{OLL} | I/O V _L Output LOW Voltage | I/O V _L sink current = 1 mA | 1.5 to 5.5 | 1.5 to 5.5 | | | 0.4 | V |
| I _{QVL} | V _L Supply Current Supply Current | I/O V _{CC} and I/O V _L unconnected, V _{EN} = V _L | 1.5 to 5.5 | 1.5 to 5.5 | | | 2.0 | μA |
| | | | 5.5 | 0 | | | 2.0 | |
| | | | 0 | 5.5 | | | -1.0 | |
| I _{QVCC} | V _L Supply Current Supply Current | I/O V _{CC} and I/O V _L unconnected, V _{EN} = V _L | 1.5 to 5.5 | 1.5 to 5.5 | | | 2.0 | μA |
| | | | 5.5 | 0 | | | 2.0 | |
| | | | 0 | 5.5 | | | -1.0 | |
| I _{TS-VCC} | V _{CC} Tri-state Output Mode | I/O V _{CC} and I/O V _L unconnected, V _{EN} = GND | 1.5 to 5.5 | 1.5 to 5.5 | | | 1.0 | μA |
| I _{TS-VL} | V _L Tri-state Output Mode Supply Current | I/O V _{CC} and I/O V _L unconnected, V _{EN} = GND | 1.5 to 5.5 | 1.5 to 5.5 | | | 1.0 | μA |

1. Typical values are for V_{CC} = +3.3 V, V_L = +1.8 V and T_A = +25°C.

2. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

NLSX0102

DC ELECTRICAL CHARACTERISTICS ($T_A = -40$ to $+85$ °C, unless otherwise specified)

| Symbol | Parameter | Test Conditions (Note 1) | V_L | V_{CC} | -40 °C to +85 °C | | | Unit |
|----------|---|-----------------------------|---------------|---------------|------------------|---------------------|-----|------------|
| | | | | | Min | Typ (Notes 1, 2) | Max | |
| I_I | Enable Pin Input Leakage Current | | 1.5 to 5.5 | 1.5 to 5.5 | | | 1.0 | μA |
| I_{OZ} | I/O Tri-state Output Mode Leakage Current | | 1.5 to 5.5 | 1.5 to 5.5 | | | 1.0 | μA |
| R_{PU} | Pull-Up Resistors I/O V_L and V_C | | | | | 10 | | k Ω |

1. Typical values are for $V_{CC} = +3.3$ V, $V_L = +1.8$ V and $T_A = +25$ °C.
2. All units are production tested at $T_A = +25$ °C. Limits over the operating temperature range are guaranteed by design.

Timing Characteristics – Rail-to-Rail Driving Configuration

(I/O test circuits of Figures 2, 3 and 7, $C_{LOAD} = 15$ pF, driver output impedance ≤ 50 Ω , $R_{LOAD} = 1$ M Ω , unless otherwise specified)

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | | | | Unit |
|--------|-----------|------------|---------------------------|-----|---------------------------|-----|---------------------------|-----|------|
| | | | $V_{CC} = 2.3$ to 2.7 V | | $V_{CC} = 3.0$ to 3.6 V | | $V_{CC} = 4.5$ to 5.5 V | | |
| | | | Min | Max | Min | Max | Min | Max | |

$V_L = 1.65$ to 1.95 V

| | | | | | | | | | |
|------------------|--|----------|-----|------|-----|------|-----|------|------|
| t_{RVL} | I/O V_L Rise Time | Figure 8 | 0.6 | 9.5 | 2.3 | 12.5 | 0.8 | 7.6 | nS |
| t_{RVCC} | I/O V_{CC} Rise Time | Figure 8 | 4.0 | 10.8 | 2.7 | 9.1 | 2.7 | 7.6 | nS |
| t_{FVL} | I/O V_L Fall Time | Figure 8 | 2.0 | 9.7 | 1.9 | 8.1 | 1.7 | 13.3 | nS |
| t_{FVCC} | I/O V_{CC} Fall Time | Figure 8 | 2.9 | 13.8 | 2.8 | 16.2 | 2.8 | 16.2 | nS |
| $t_{PHL-VL-VCC}$ | Propagation Delay (Driving I/O V_L , V_L to V_{CC}) | Figure 2 | | 5.6 | | 7.1 | | 6.8 | nS |
| $t_{PLH-VL-VCC}$ | | | | 6.5 | | 7.1 | | 7.4 | |
| $t_{PHL-VCC-VL}$ | Propagation Delay (Driving I/O V_{CC} , V_{CC} to V_L) | Figure 3 | | 4.8 | | 5.3 | | 2.0 | nS |
| $t_{PLH-VCC-VL}$ | | | | 4.8 | | 5.0 | | 3.5 | |
| t_{EN} | Enable Time | Figure 7 | | 50 | | 40 | | 35 | nS |
| t_{DIS} | Disable Time | Figure 7 | | 316 | | 225 | | 215 | nS |
| t_{PPSKEW} | Part-to-Part Skew | | | 0.7 | | 0.7 | | 0.7 | nS |
| MDR | Maximum Data Rate | | 21 | | 22 | | 24 | | Mbps |

$V_L = 2.3$ to 2.7 V

| | | | | | | | | | |
|------------------|--|----------|-----|-----|-----|-----|-----|------|------|
| t_{RVL} | I/O V_L Rise Time | Figure 8 | 2.8 | 7.7 | 2.6 | 8.1 | 1.8 | 10.3 | nS |
| t_{RVCC} | I/O V_{CC} Rise Time | Figure 8 | 3.2 | 9.2 | 2.9 | 8.8 | 2.4 | 6.4 | nS |
| t_{FVL} | I/O V_L Fall Time | Figure 8 | 1.9 | 8.3 | 1.9 | 7.8 | 1.8 | 7.4 | nS |
| t_{FVCC} | I/O V_{CC} Fall Time | Figure 8 | 2.2 | 8.3 | 2.4 | 8.0 | 2.6 | 10.0 | nS |
| $t_{PHL-VL-VCC}$ | Propagation Delay (Driving I/O V_L , V_L to V_{CC}) | Figure 2 | | 3.2 | | 3.7 | | 3.9 | nS |
| $t_{PLH-VL-VCC}$ | | | | 4.8 | | 5.3 | | 6.0 | |
| $t_{PHL-VCC-VL}$ | Propagation Delay (Driving I/O V_{CC} , V_{CC} to V_L) | Figure 3 | | 2.5 | | 1.6 | | 1.0 | nS |
| $t_{PLH-VCC-VL}$ | | | | 4.5 | | 4.3 | | 3.4 | |
| t_{EN} | Enable Time | Figure 7 | | 50 | | 40 | | 35 | nS |
| t_{DIS} | Disable Time | Figure 7 | | 225 | | 225 | | 215 | nS |
| t_{PPSKEW} | Part-to-Part Skew | | | 0.7 | | 0.7 | | 0.7 | nS |
| MDR | Maximum Data Rate | | 20 | | 22 | | 24 | | Mbps |

NLSX0102

Timing Characteristics – Rail-to-Rail Driving Configuration

(I/O test circuits of Figures 2, 3 and 7, $C_{LOAD} = 15 \text{ pF}$, driver output impedance $\leq 50 \Omega$, $R_{LOAD} = 1 \text{ M}\Omega$, unless otherwise specified)

| Symbol | Parameter | Conditions | -40°C to +85°C | | | | | | Unit |
|--------|-----------|------------|--|-----|--|-----|--|-----|------|
| | | | $V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$ | | $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$ | | $V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$ | | |
| | | | Min | Max | Min | Max | Min | Max | |

$V_L = 3.0 \text{ to } 3.6 \text{ V}$

| | | | | | | | | | |
|------------------|--|----------|--|--|-----|-----|-----|-----|------|
| t_{FVL} | I/O V_L Rise Time | Figure 8 | | | 2.3 | 6.5 | 1.9 | 8.0 | nS |
| t_{RVCC} | I/O V_{CC} Rise Time | Figure 8 | | | 2.5 | 6.5 | 2.1 | 7.4 | nS |
| t_{FVL} | I/O V_L Fall Time | Figure 8 | | | 2.0 | 7.2 | 1.9 | 5.9 | nS |
| t_{FVCC} | I/O V_{CC} Fall Time | Figure 8 | | | 2.3 | 8.0 | 2.4 | 9.3 | nS |
| $t_{PHL-VL-VCC}$ | Propagation Delay (Driving I/O V_L , V_L to V_{CC}) | Figure 2 | | | | 2.4 | | 3.1 | nS |
| $t_{PLH-VL-VCC}$ | | | | | | 3.8 | | 3.8 | |
| $t_{PHL-VCC-VL}$ | Propagation Delay (Driving I/O V_{CC} , V_{CC} to V_L) | Figure 3 | | | | 2.5 | | 2.6 | nS |
| $t_{PLH-VCC-VL}$ | | | | | | 3.6 | | 3.1 | |
| t_{EN} | Enable Time | Figure 7 | | | | 40 | | 35 | nS |
| t_{DIS} | Disable Time | Figure 7 | | | | 225 | | 235 | nS |
| t_{PPSKEW} | Part-to-Part Skew | | | | | 0.7 | | 0.7 | nS |
| MDR | Maximum Data Rate | | | | 23 | | 24 | | Mbps |

Timing Characteristics – Open Drain Driving Configuration

(I/O test circuits of Figures 4, 5 and 7, $C_{LOAD} = 15 \text{ pF}$, driver output impedance $\leq 50 \Omega$, $R_{LOAD} = 1 \text{ M}\Omega$, unless otherwise specified)

| Symbol | Parameter | Conditions | -40°C to +85°C | | | | | | Unit |
|--------|-----------|------------|--|-----|--|-----|--|-----|------|
| | | | $V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$ | | $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$ | | $V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$ | | |
| | | | Min | Max | Min | Max | Min | Max | |

$V_L = 1.65 \text{ to } 1.95 \text{ V}$

| | | | | | | | | | |
|-----------------|--|----------|------|------|------|------|------|------|------|
| t_{FVL} | I/O V_L Rise Time | Figure 8 | 38 | 340 | 30 | 245 | 22.0 | 134 | nS |
| t_{RVCC} | I/O V_{CC} Rise Time | Figure 8 | 34 | 330 | 23 | 218 | 10.0 | 120 | nS |
| t_{FVL} | I/O V_L Fall Time | Figure 8 | 4.4 | 11.1 | 4.3 | 12.0 | 4.2 | 14.2 | nS |
| t_{FVCC} | I/O V_{CC} Fall Time | Figure 8 | 6.9 | 11 | 7.5 | 16.2 | 7.0 | 16.2 | nS |
| $t_{PHLVL-VCC}$ | Propagation Delay (Driving I/O V_L , V_L to V_{CC}) | Figure 2 | 2.3 | 27 | 2.4 | 20.0 | 2.6 | 23.0 | nS |
| $t_{PLHVL-VCC}$ | | | 45 | 260 | 36.0 | 208 | 27.0 | 208 | |
| $t_{PHLVCC-VL}$ | Propagation Delay (Driving I/O V_{CC} , V_{CC} to V_L) | Figure 3 | 1.9 | 22 | 1.1 | 22.0 | 1.2 | 22.0 | nS |
| $t_{PLHVCC-VL}$ | | | 45.0 | 200 | 36 | 150 | 27.0 | 112 | |
| t_{EN} | Enable Time | Figure 7 | | 80 | | 70 | | 35 | nS |
| t_{DIS} | Disable Time | Figure 7 | | 250 | | 277 | | 290 | nS |
| t_{PPSKEW} | Part-to-Part Skew | | | 0.7 | | 0.7 | | 0.7 | nS |
| MDR | Maximum Data Rate | | 2 | | 2 | | 2 | | Mbps |

NLSX0102

Timing Characteristics – Open Drain Driving Configuration

(I/O test circuits of Figures 4, 5 and 7, $C_{LOAD} = 15 \text{ pF}$, driver output impedance $\leq 50 \Omega$, $R_{LOAD} = 1 \text{ M}\Omega$, unless otherwise specified)

| Symbol | Parameter | Conditions | -40°C to +85°C | | | | | | Unit |
|--------|-----------|------------|--|-----|--|-----|--|-----|------|
| | | | $V_{CC} = 2.3 \text{ to } 2.7 \text{ V}$ | | $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$ | | $V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$ | | |
| | | | Min | Max | Min | Max | Min | Max | |

$V_L = 2.3 \text{ to } 2.7 \text{ V}$

| | | | | | | | | | |
|-----------------|--|----------|------|------|------|------|------|------|------|
| t_{RVL} | I/O V_L Rise Time | Figure 8 | 34 | 400 | 28.0 | 300 | 24.0 | 208 | nS |
| t_{RVCC} | I/O V_{CC} Rise Time | Figure 8 | 35.0 | 352 | 24.0 | 280 | 12.0 | 180 | nS |
| t_{FVL} | I/O V_L Fall Time | Figure 8 | 4.4 | 6.9 | 4.3 | 6.2 | 4.2 | 7.8 | nS |
| t_{FVCC} | I/O V_{CC} Fall Time | Figure 8 | 4.3 | 8.8 | 4.9 | 9.4 | 5.4 | 10.4 | nS |
| $t_{PHLVL-VCC}$ | Propagation Delay (Driving I/O V_L , V_L to V_{CC}) | Figure 2 | 1.7 | 14.0 | 2.0 | 14.0 | 2.1 | 14.0 | nS |
| $t_{PLHVL-VCC}$ | | | 43.0 | 250 | 36.0 | 210 | 27.0 | 210 | |
| $t_{PHLVCC-VL}$ | Propagation Delay (Driving I/O V_{CC} , V_{CC} to V_L) | Figure 3 | 1.8 | 13.0 | 2.6 | 13.0 | 1.2 | 13.0 | nS |
| $t_{PLHVCC-VL}$ | | | 44.0 | 225 | 37.0 | 180 | 27.0 | 144 | |
| t_{EN} | Enable Time | Figure 7 | | 50 | | 40 | | 35 | nS |
| t_{DIS} | Disable Time | Figure 7 | | 265 | | 230 | | 215 | nS |
| t_{PPSKEW} | Part-to-Part Skew | | | 0.7 | | 0.7 | | 0.7 | nS |
| MDR | Maximum Data Rate | | 2 | | 2 | | 2 | | Mbps |

$V_L = 3.0 \text{ to } 3.6 \text{ V}$

| | | | | | | | | | |
|-----------------|--|----------|--|--|------|------|------|------|------|
| t_{RVL} | I/O V_L Rise Time | Figure 8 | | | 25.0 | 400 | 19.0 | 278 | nS |
| t_{RVCC} | I/O V_{CC} Rise Time | Figure 8 | | | 26.0 | 375 | 14.0 | 247 | nS |
| t_{FVL} | I/O V_L Fall Time | Figure 8 | | | 2.8 | 6.1 | 2.6 | 5.7 | nS |
| t_{FVCC} | I/O V_{CC} Fall Time | Figure 8 | | | 2.6 | 7.6 | 3.1 | 8.3 | nS |
| $t_{PHLVL-VCC}$ | Propagation Delay (Driving I/O V_L , V_L to V_{CC}) | Figure 2 | | | 1.3 | 10.0 | 1.4 | 8.0 | nS |
| $t_{PLHVL-VCC}$ | | | | | 36.0 | 255 | 28.0 | 243 | |
| $t_{PHLVCC-VL}$ | Propagation Delay (Driving I/O V_{CC} , V_{CC} to V_L) | Figure 3 | | | 1.0 | 124 | 1.0 | 97.0 | nS |
| $t_{PLHVCC-VL}$ | | | | | 3.0 | 185 | 3.0 | 136 | |
| t_{EN} | Enable Time | Figure 7 | | | | 40 | | 35 | nS |
| t_{DIS} | Disable Time | Figure 7 | | | | 250 | | 205 | nS |
| t_{PPSKEW} | Part-to-Part Skew | | | | | 0.7 | | 0.7 | nS |
| MDR | Maximum Data Rate | | | | 2 | | 2 | | Mbps |

NLSX0102

TEST SETUPS

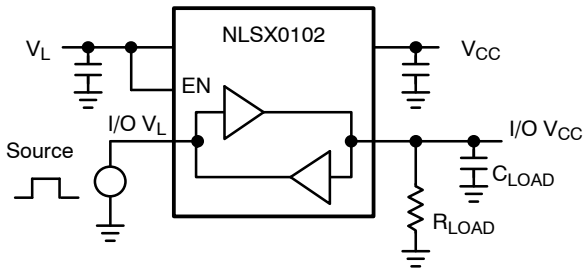


Figure 2. Rail-to-Rail Driving I/O V_L

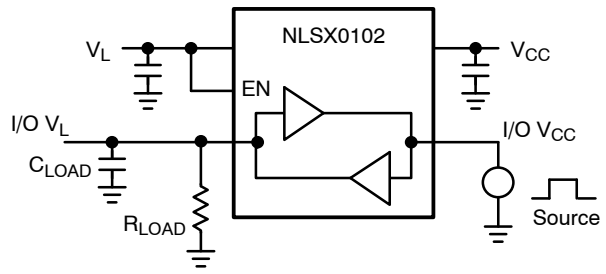


Figure 3. Rail-to-Rail Driving I/O V_{CC}

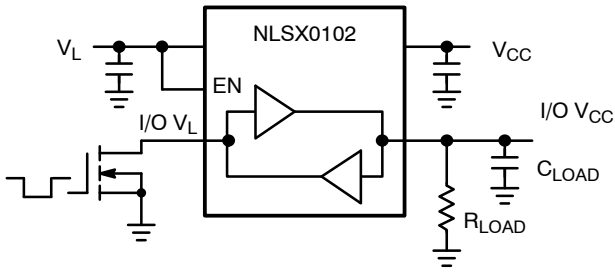


Figure 4. Open-Drain Driving I/O V_L

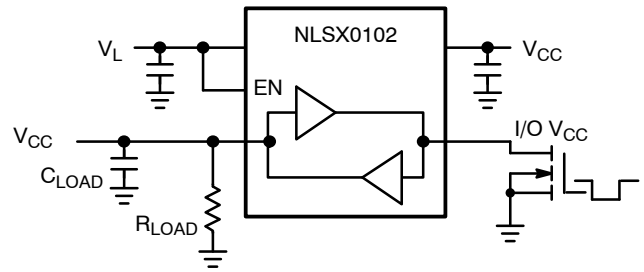


Figure 5. Open-Drain Driving I/O V_{CC}

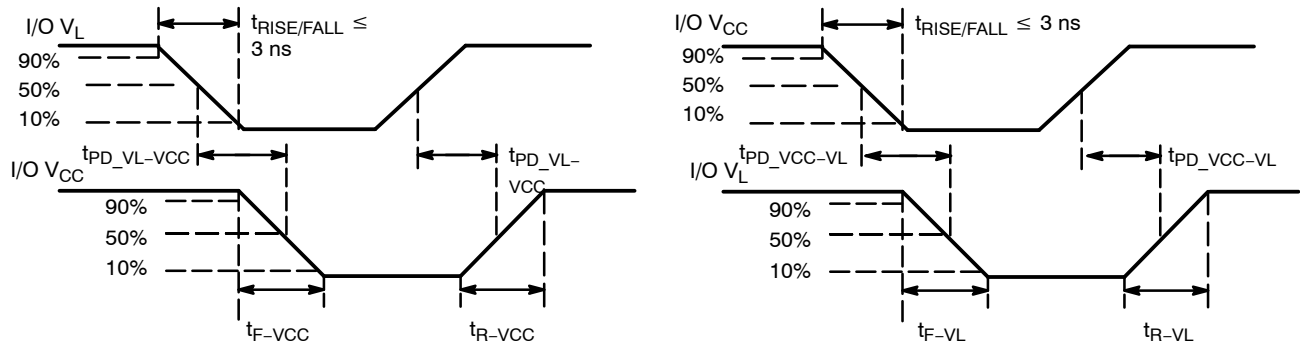
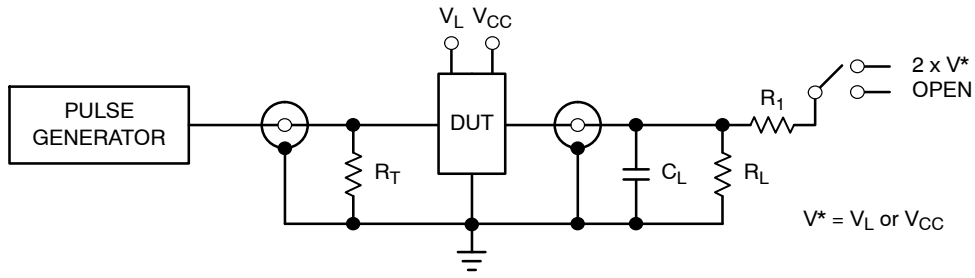


Figure 6. Definition of Timing Specification Parameters

NLSX0102



| Test | Switch |
|--------------------|----------------|
| t_{PZH}, t_{PHZ} | Open |
| t_{PZL}, t_{PLZ} | $2 \times V^*$ |

$C_L = 15 \text{ pF}$ or equivalent (Includes jig and probe capacitance)
 $R_L = R_1 = 50 \text{ k}\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)
 $V^* = V_L$ or V_{CC} for I/O_VL or I/O_VCC measurements, respectively.

Figure 7. Test Circuit for Enable/Disable Time Measurement

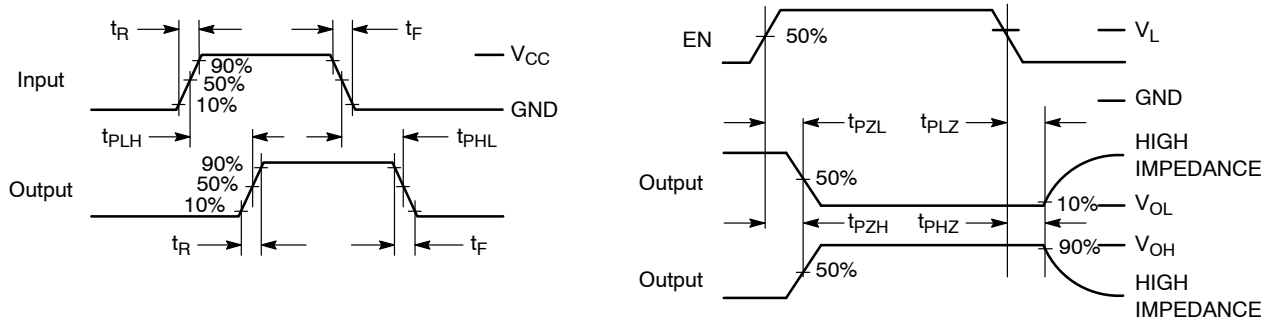


Figure 8. Timing Definitions for Propagation Delays and Enable/Disable Measurement

NLSX0102

APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX0102 auto sense translator provides bi-directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages, V_L and V_{CC} , which set the logic levels on the input and output sides of the translator. When used to transfer data from the V_L to the V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC} . In a similar manner, the V_{CC} to V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L .

The NLSX0102 consists of two bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. The one-shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high-to-low and low-to-high transitions. Each input/output channel has an internal 10 k Ω pull-up. The magnitude of the pull-up resistors can be reduced by connecting external resistors in parallel to the internal 10 k Ω resistors.

Input Driver Requirements

The rise (t_R) and fall (t_F) timing parameters of the open drain outputs depend on the magnitude of the pull-up resistors. In addition, the propagation times (t_{PD}), skew (t_{PSKEW}) and maximum data rate depend on the impedance

of the device that is connected to the translator. The timing parameters listed in the data sheet assume that the output impedance of the drivers connected to the translator is less than 50 k Ω .

Enable Input (EN)

The NLSX0102 has an Enable pin (EN) that provides tri-state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O V_L pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Overvoltage Tolerant (OVT) protection.

Power Supply Guidelines

During normal operation, supply voltage V_L can be greater than, less than or equal to V_{CC} . The sequencing of the power supplies will not damage the device during the power up operation. For optimal performance, 0.01 μ F to 0.1 μ F decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

ORDERING INFORMATION

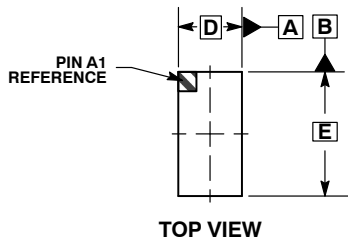
| Device | Package | Shipping [†] |
|---------------|--------------------------|-----------------------|
| NLSX0102FCT1G | Flip-Chip 8 (Pb-Free) | 3000 / Tape & Reel |
| NLSX0102FCT2G | Flip-Chip 8 (Pb-Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

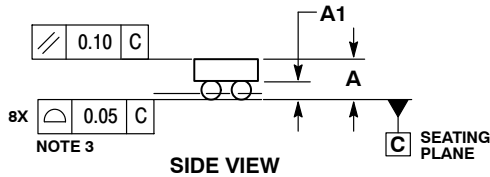
NLSX0102

PACKAGE DIMENSIONS

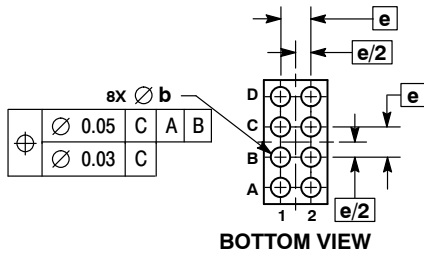
8 PIN FLIP-CHIP, 0.9x1.9, 0.5P CASE 499BF-01 ISSUE O



TOP VIEW



SIDE VIEW



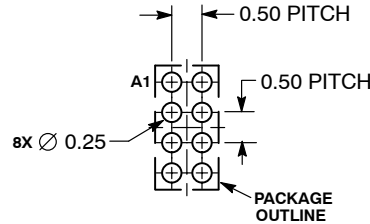
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.44 | 0.50 |
| A1 | 0.15 | 0.19 |
| b | 0.21 | 0.25 |
| D | 0.90 BSC | |
| E | 1.90 BSC | |
| e | 0.50 BSC | |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative