

# High Voltage, High Frequency, BiMOSFET™ Monolithic Bipolar MOS Transistor

## IXBL20N300C



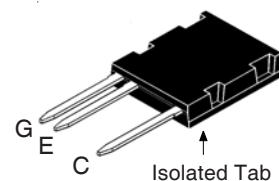
$$V_{CES} = 3000V$$

$$I_{C110} = 20A$$

$$V_{CE(sat)} \leq 6.0V$$

(Electrically Isolated Tab)

ISOPLUS i5-Pak™



G = Gate      C = Collector  
E = Emitter

Symbol	Test Conditions	Maximum Ratings	
$V_{CES}$	$T_J = 25^\circ C$ to $150^\circ C$	3000	V
$V_{CGR}$	$T_J = 25^\circ C$ to $150^\circ C$ , $R_{GE} = 1M\Omega$	3000	V
$V_{GES}$	Continuous	$\pm 20$	V
$V_{GEM}$	Transient	$\pm 30$	V
$I_{C25}$	$T_C = 25^\circ C$	50	A
$I_{C110}$	$T_C = 110^\circ C$	20	A
$I_{CM}$	$T_C = 25^\circ C$ , 1ms	430	A
<b>SSOA</b> <b>(RBSOA)</b>	$V_{GE} = 15V$ , $T_{VJ} = 125^\circ C$ , $R_G = 3\Omega$ Clamped Inductive Load	$I_{CM} = 160$ $V_{CES} \leq 1500$	A V
<b><math>T_{SC}</math></b> <b>(SCSOA)</b>	$V_{GE} = 15V$ , $T_J = 125^\circ C$ , $R_G = 52\Omega$ , $V_{CE} = 1500V$ , Non-Repetitive	10	$\mu s$
$P_C$	$T_C = 25^\circ C$	417	W
$T_J$		-55 ... +150	$^\circ C$
$T_{JM}$		150	$^\circ C$
$T_{stg}$		-55 ... +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ C$
$T_{SOLD}$	Plastic Body for 10s	260	$^\circ C$
$F_C$	Mounting Force with Clip	30..170 / 7..36	N/lb
$V_{ISOL}$	50/60Hz, 5 Seconds	4000	V~
<b>Weight</b>		8	g

### Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Frequency Operation

### Advantages

- Low Gate Drive Requirement
- High Power Density

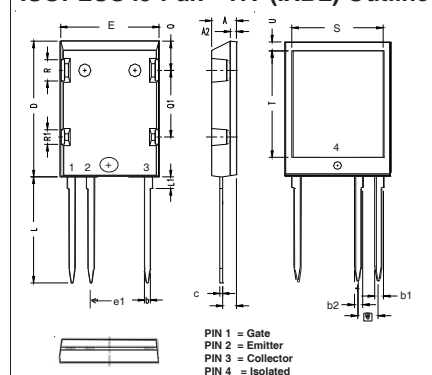
### Applications

- Switch-Mode and Resonant-Mode Power Supplies

Symbol	Test Conditions ( $T_J = 25^\circ C$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{CES}$	$I_C = 250\mu A$ , $V_{GE} = 0V$	3000		V
$V_{GE(th)}$	$I_C = 250\mu A$ , $V_{CE} = V_{GE}$	3.0		5.0 V
$I_{CES}$	$V_{CE} = V_{CES}$ , $V_{GE} = 0V$ Note 2, $T_J = 125^\circ C$			25 $\mu A$ 6.5 mA
$I_{GES}$	$V_{CE} = 0V$ , $V_{GE} = \pm 20V$			$\pm 200$ nA
$V_{CE(sat)}$	$I_C = 20A$ , $V_{GE} = 15V$ , Note 1 $T_J = 125^\circ C$		4.5 5.1	V V

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$I_C = 20\text{A}, V_{CE} = 10\text{V}$ , Note 1	25	43	S
$C_{ies}$	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		10	nF
$C_{oes}$			440	pF
$C_{res}$			160	pF
$Q_{g(on)}$	$I_C = 20\text{A}, V_{GE} = 15\text{V}, V_{CE} = 1000\text{V}$		425	nC
$Q_{ge}$			53	nC
$Q_{gc}$			160	nC
$t_{d(on)}$	<b>Inductive load, <math>T_J = 25^\circ\text{C}</math></b> $I_C = 20\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1500\text{V}, R_G = 3\Omega$ Note 3		33	ns
$t_{ri}$			12	ns
$E_{on}$			23.0	mJ
$t_{d(off)}$			370	ns
$t_{fi}$			110	ns
$E_{off}$			2.6	mJ
$t_{d(on)}$	<b>Inductive load, <math>T_J = 125^\circ\text{C}</math></b> $I_C = 20\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 1500\text{V}, R_G = 3\Omega$ Note 3		33	ns
$t_{ri}$			14	ns
$E_{on}$			23.0	mJ
$t_{d(off)}$			435	ns
$t_{fi}$			175	ns
$E_{off}$			3.7	mJ
$R_{thJC}$			0.30	$^\circ\text{C/W}$
$R_{thCS}$		0.15		$^\circ\text{C/W}$

## ISOPLUS I5-Pak™ HV (IXBL) Outline



SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	0.190	0.205	4.83	5.21
A1	0.102	0.118	2.59	3.00
A2	0.046	0.055	1.17	1.40
b	0.045	0.055	1.14	1.40
b1	0.063	0.072	1.60	1.83
b2	0.058	0.068	1.47	1.73
c	0.020	0.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	0.770	0.799	19.56	20.29
e	0.150 BSC		3.81 BSC	
e1	0.450 BSC		11.43 BSC	
L	0.780	0.820	19.81	20.83
L1	0.080	0.102	2.03	2.59
Q	0.210	0.235	5.33	5.97
Q1	0.490	0.513	12.45	13.03
R	0.150	0.180	3.81	4.57
R1	0.100	0.130	2.54	3.30
S	0.668	0.690	16.97	17.53
T	0.801	0.821	20.34	20.85
U	0.065	0.080	1.65	2.03

## Reverse Diode

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max
$V_F$	$I_F = 20\text{A}, V_{GE} = 0\text{V}$ , Note 1			5.0 V
$t_{rr}$	$I_F = 20\text{A}, V_{GE} = 0\text{V}, -di_F/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GE} = 0\text{V}$		864	ns
$I_{RM}$			31	A
$Q_{RM}$			13.5	$\mu\text{C}$

## Notes:

1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.
3. Switching times & energy losses may increase for higher  $V_{CE}$ (clamp),  $T_J$  or  $R_G$ .

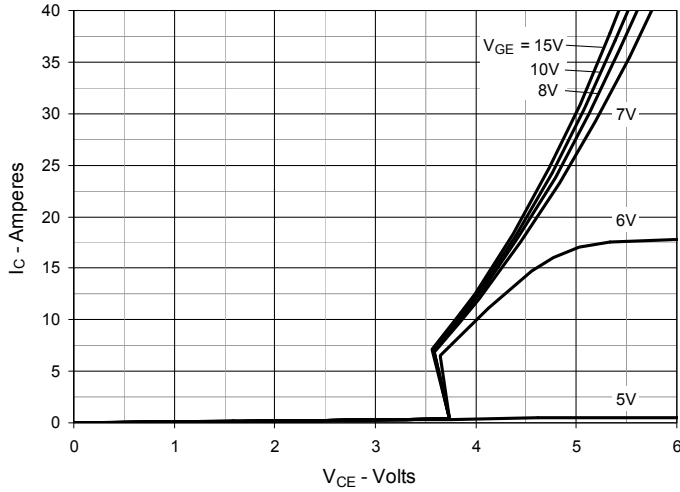
## ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

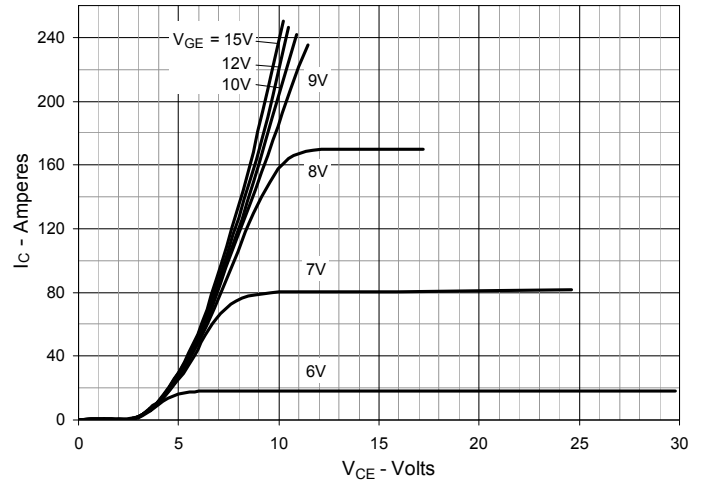
IXYS Reserves the Right to Change Limits, Test Conditions and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

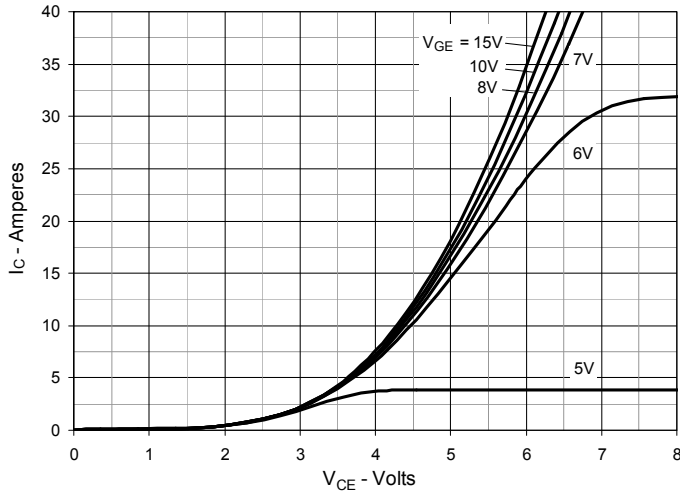
**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$**



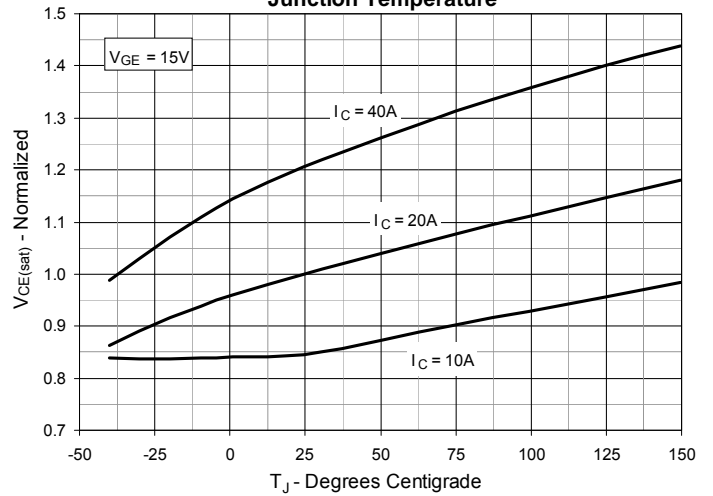
**Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$**



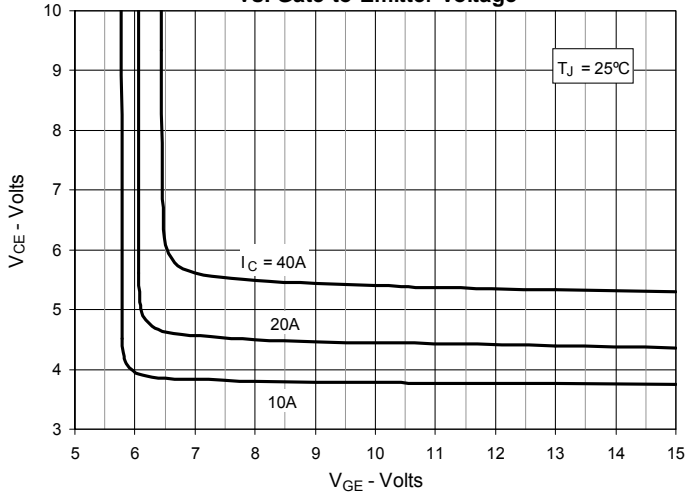
**Fig. 3. Output Characteristics @  $T_J = 125^\circ\text{C}$**



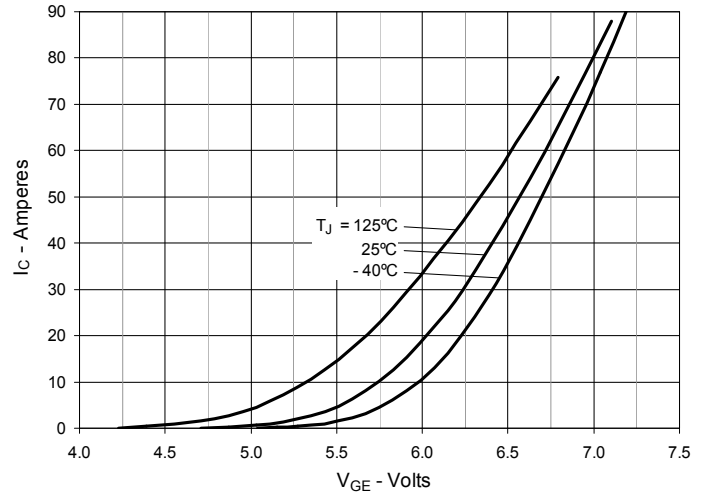
**Fig. 4. Dependence of  $V_{CE(sat)}$  on Junction Temperature**

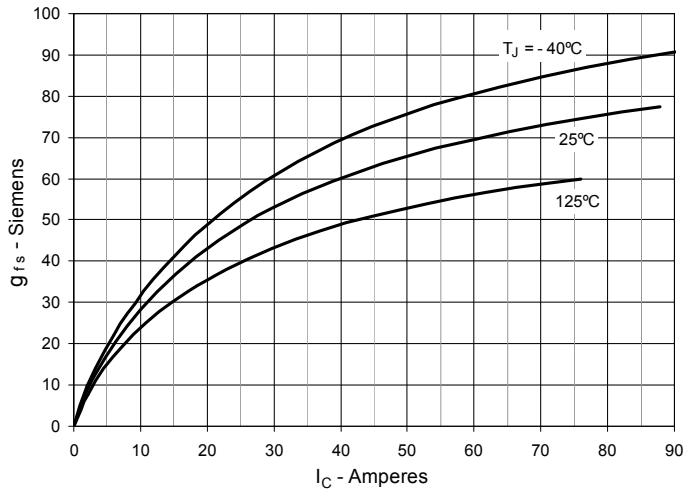
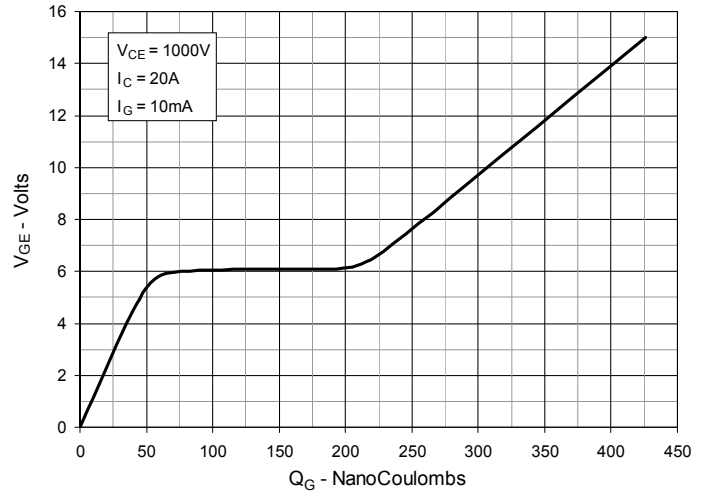
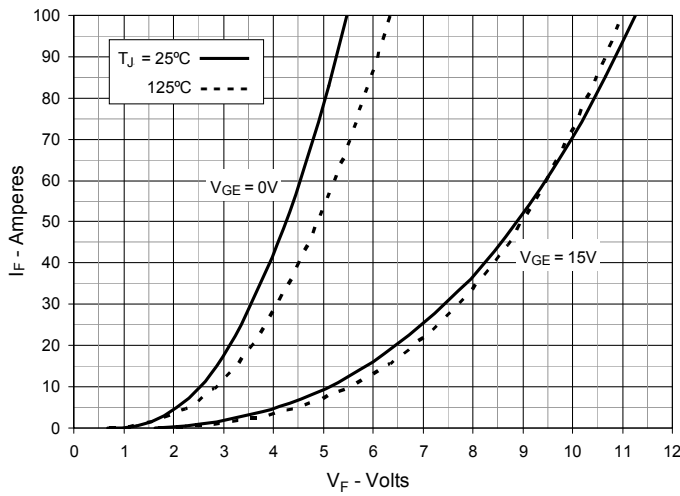
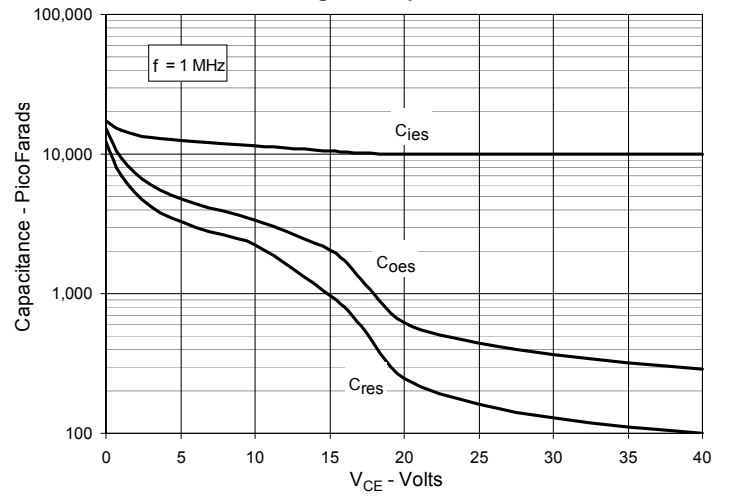
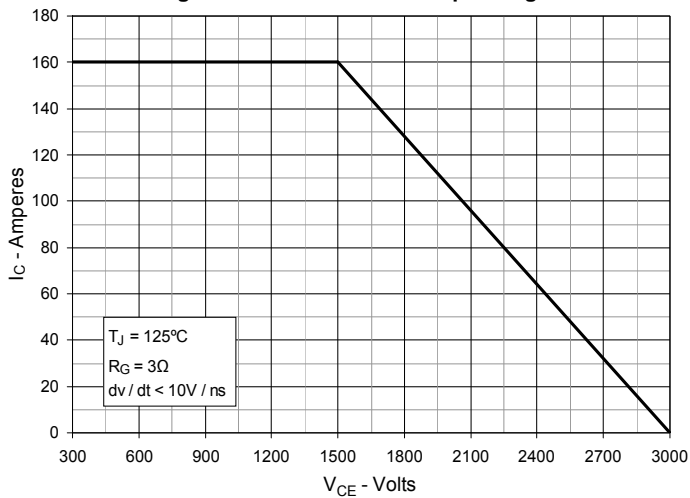
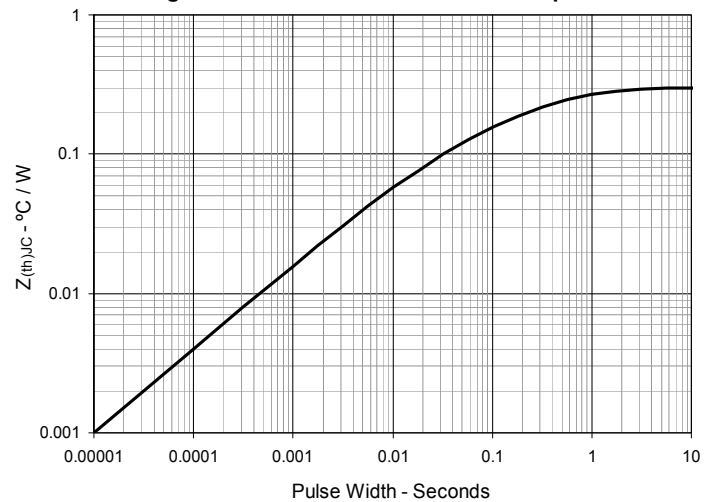


**Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage**

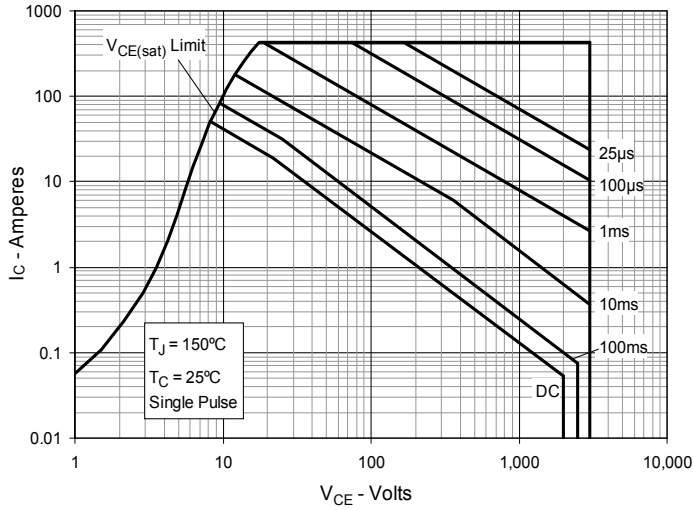


**Fig. 6. Input Admittance**

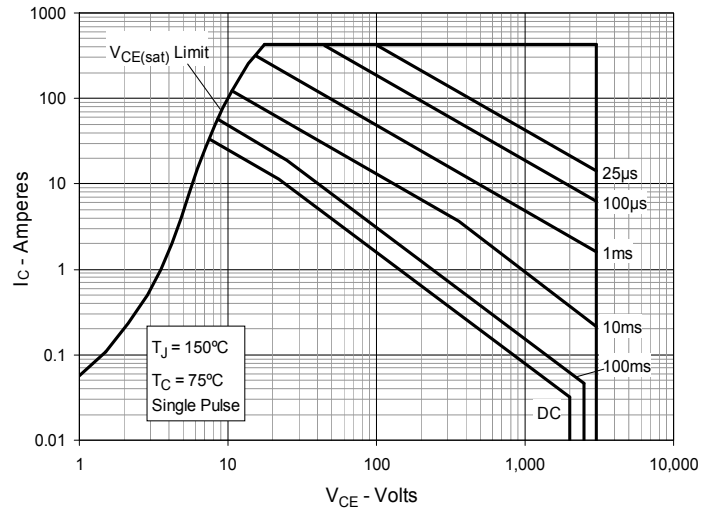


**Fig. 7. Transconductance**

**Fig. 8. Gate Charge**

**Fig. 9. Forward Voltage Drop of Intrinsic Diode**

**Fig. 10. Capacitance**

**Fig. 11. Reverse-Bias Safe Operating Area**

**Fig. 12. Maximum Transient Thermal Impedance**


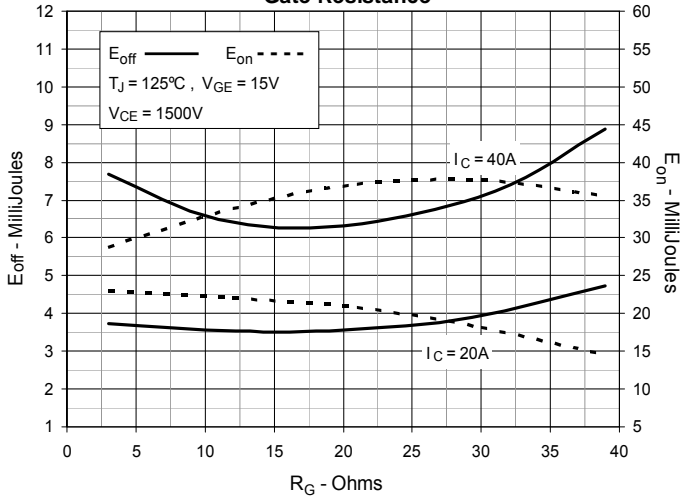
**Fig. 13. Forward-Bias Safe Operating Area @  $T_C = 25^\circ\text{C}$**



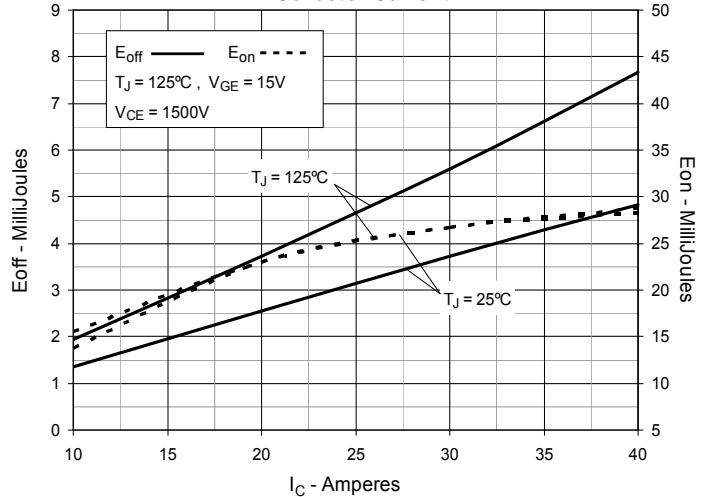
**Fig. 14. Forward-Bias Safe Operating Area @  $T_C = 75^\circ\text{C}$**



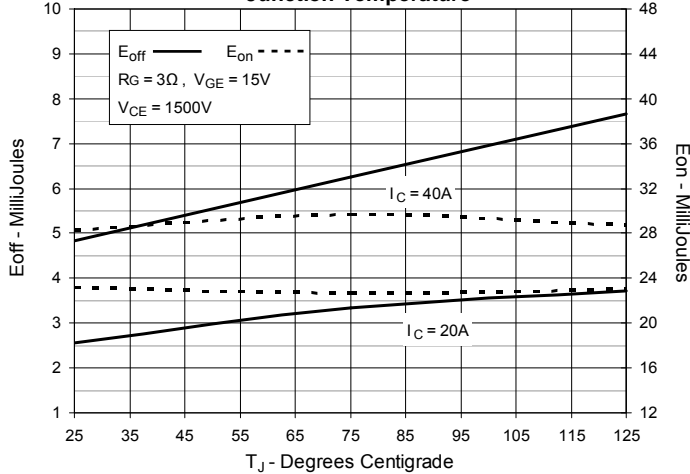
**Fig. 15. Inductive Switching Energy Loss vs. Gate Resistance**



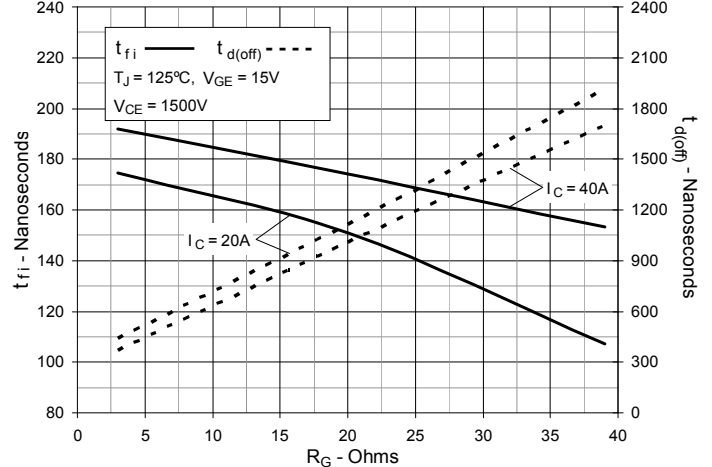
**Fig. 16. Inductive Switching Energy Loss vs. Collector Current**



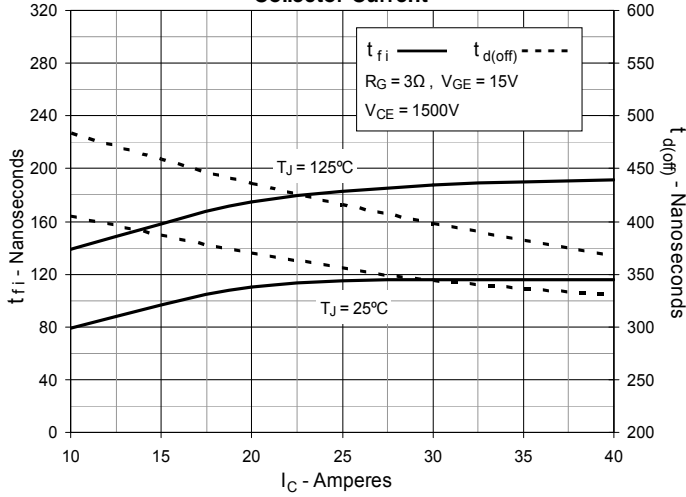
**Fig. 17. Inductive Switching Energy Loss vs. Junction Temperature**



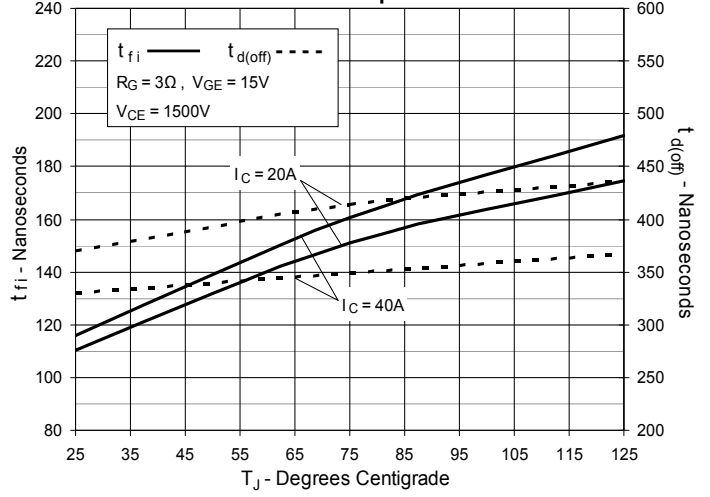
**Fig. 18. Inductive Turn-off Switching Times vs. Gate Resistance**



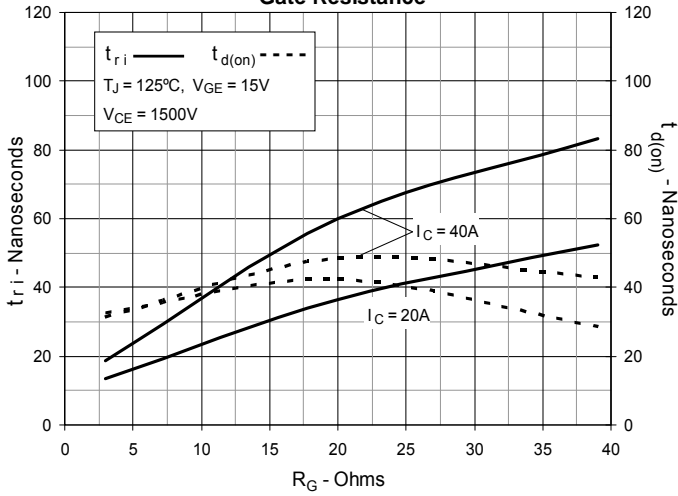
**Fig. 19. Inductive Turn-off Switching Times vs. Collector Current**



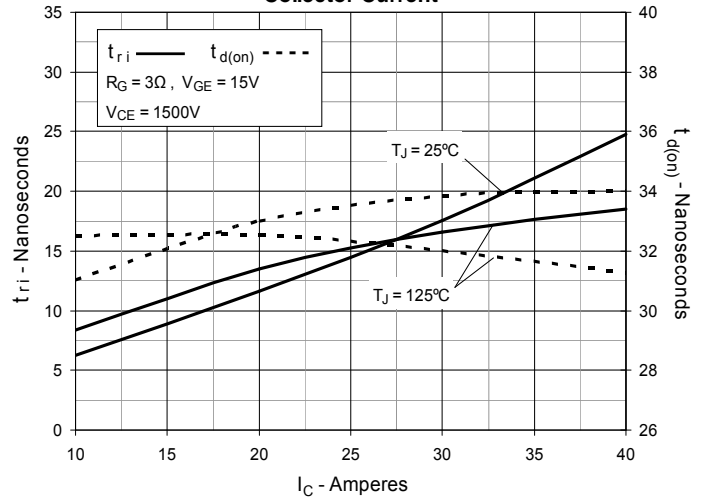
**Fig. 20. Inductive Turn-off Switching Times vs. Junction Temperature**



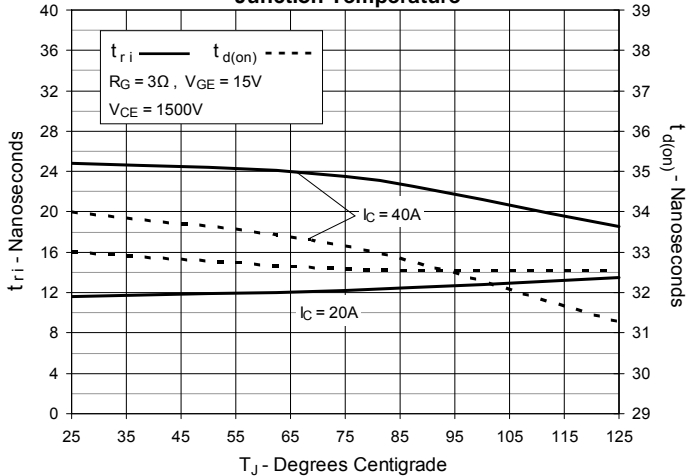
**Fig. 21. Inductive Turn-on Switching Times vs. Gate Resistance**



**Fig. 22. Inductive Turn-on Switching Times vs. Collector Current**



**Fig. 23. Inductive Turn-on Switching Times vs. Junction Temperature**



IXYS Reserves the Right to Change Limits, Test Conditions and Dimensions.