

TRIUNE PRODUCTS

Features

- Low Offset
- High Voltage Input
- Supply voltage: 4V-42V
- Low Temperature Drift
- Low input bias current
- Pedestal Voltage for offset compensation
- Available in 8-pin SOT-23 package
- Product is lead-free, Halogen Free, RoHS / WEEE compliant

Applications

- Multi-standard compliant and non-compliant wireless chargers for:
 - Cell Phones and Smartphones
 - Qi-Compliant Wireless Charging Transmitters
 - Tablets and eReaders
- Notebook Computers
- Telecom Equipment
- Power Management
- Battery Chargers
- Welding Equipment

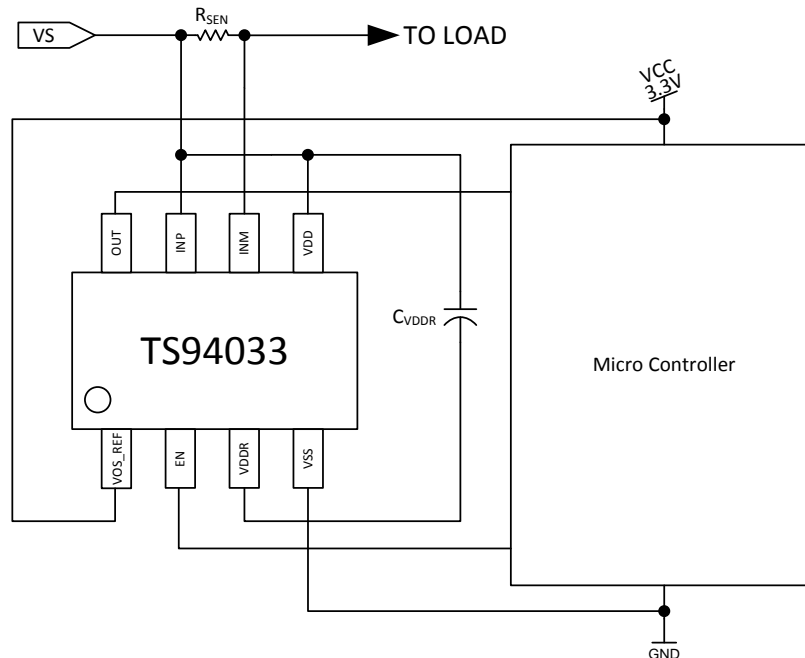
Description

The TS94033 is a low power, low offset high-side current sense amplifier. It utilizes a chopper-stabilized configuration to provide high gain-bandwidth while reducing input offset and 1/f noise. The sense amplifiers offer high voltage inputs and a 0 to 3.3V output. The supply voltage range of 4V to 42V can accommodate a wide variety of applications.

A zero-current output offset is set by providing a bias voltage on the VOS_REF pin. This allows the ability to sense limited negative currents, improves transient response time, and provides a method to detect faults in the current sense system.

The TS94033 operational amplifier is optimal for bridge drive applications where accurate current sensing is needed.

Typical Application Circuit



Pin Description

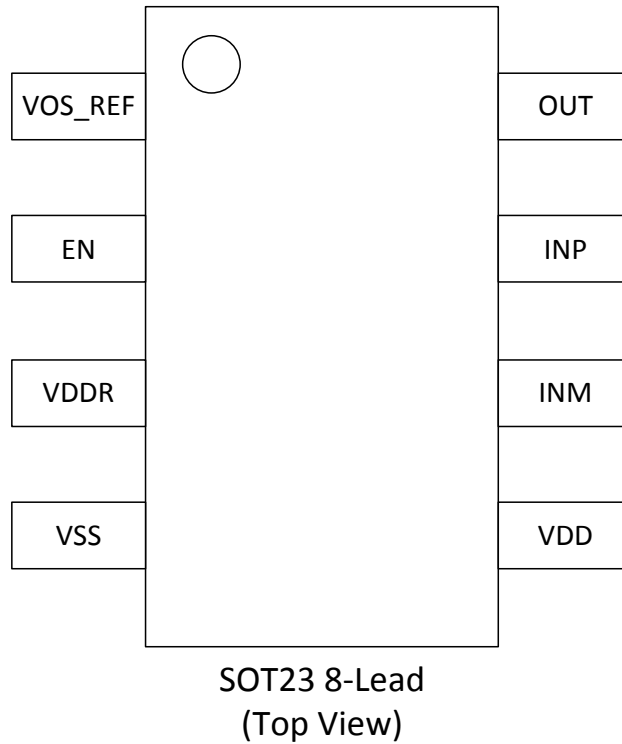


Figure 1: TS94033 Pin Configuration

Pin Number	Pin Name	I/O/P	Description
1	VOS_REF	I	Zero-Current Output Offset Reference
2	EN	I	Enable Input
3	VDDR	O	Supply-Referenced Regulated Voltage Output
4	VSS	P	Power Supply Return, VOS_REF and OUT Signal Reference Voltage (ground)
5	VDD	P	Power Supply Input, Sense Amplifier Input Common-Mode Signal Reference
6	INM	I	Sense Amplifier Inverting Input
7	INP	I	Sense Amplifier Non-Inverting Input
8	OUT	O	Sense Amplifier Output

Functional Block Diagram

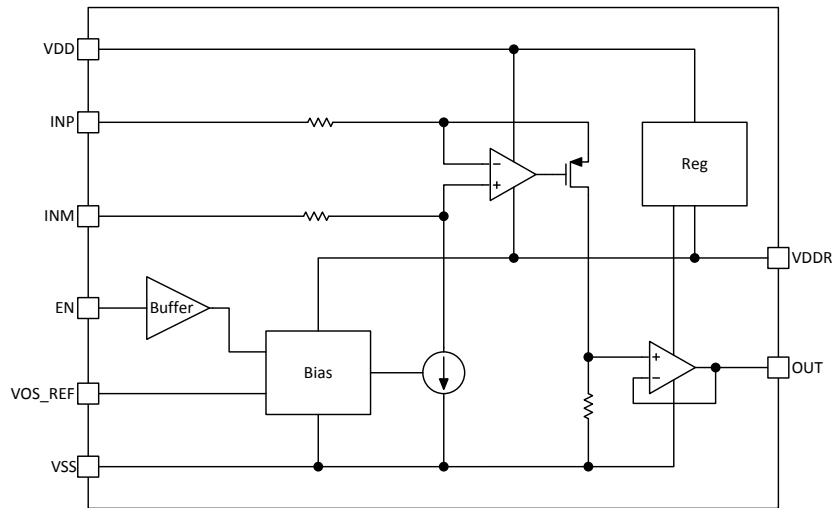


Figure 2: TS94033 Block Diagram

Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted ^(1,2)

Parameter	Value	Unit
Supply Voltage (VDD – VSS)	42	V
Signal Input Voltages (INP, INM, VDDR)	$V_{DD}-5.5$ to $V_{DD}+0.4$	V
VSS-Referenced Signals (EN, OUT, VOS_REF)	-0.3 to 5.5	V
Electrostatic Discharge – Human Body Model	2	kV
Operating Junction Temperature Range, T_J	-40 to 150	°C
Storage Temperature Range, T_{STG}	-65 to 150	°C
Peak IR Reflow Temperature (10 to 30 seconds)	260	°C

Notes:

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	75	°C/W
T_J	Operating Junction Temperature Range	-40 to 125	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_S	Supply Voltage, VDD – VSS	4	42	V
V_{OS_REF}	Output Offset Reference, (VOS_REF – VSS)	0	3.3	V
V_{IN}	Differential Input Voltage, (VINP – VINM)	-4	66	mV
V_{CM}	Input Common-Mode Range, ($V_{DD} - 0.5 * (VINP + VINM)$)	VDD-2	VDD+0.3	V
V_{IH-EN}	High Level Input Voltage, EN Pin	2.4	5.5	V
V_{IL-EN}	Low Level Input Voltage, EN Pin	0	0.4	V
C_L	OUT Pin Load Capacitance		100	nF

Electrical Characteristics

Typical: $T_J = 25^\circ\text{C}$, $V_{DD} = 12\text{V}$

Min and max: $T_J = -40^\circ\text{C}$ to 125°C , $V_{DD} = 4\text{V} \sim 42\text{V}$

Unless otherwise noted $V_{SS} = 0\text{V}$, $V_{CM} = V_{DD}$, INP - INM = 0V, $V_{OS_REF} = 3.3\text{V}$

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{QDD}	Quiescent Current	From VDD		140	315	μA
I_{QVCM}	Quiescent Current	Through INP/INM		28		μA
I_{Q-OFF}	Quiescent Current	From VDD, EN = 0V, $V_{OS_REF}=0$		1.1	8.6	μA
I_{IL-EN}	Input Low Leakage, EN Pin	$V_{EN} = 0\text{V}$		1.1		μA
I_B	Input Bias Current	$V_{OS_REF} = 0\text{V}$		2.1		μA
ΔV_{DDR}	Sense-Amp Supply Voltage	$\Delta V_{DDR} = V_{DD} - V_{DDR}$ $C_{VDDR} = 100\text{nF}$		4.4		V
T_{ON-EN}	Turn-On Time ⁽¹⁾	EN driven from 0V to 3.3V, OUT settled to 90% of final value		600		μs
PSRR	Power Supply Rejection Ratio ¹	100 kHz		-70		dB
LR	Line Regulation	4– 42V step applied on V_{DD}		-83		dB
SR	Slew Rate	$C_L=100\text{nF}$		10		mV/ μs
$ I_{sc} $	Short-Circuit Current, Sourcing or Sinking	OUT shorted to VDD or VSS		1	1.7	mA
V_{OUT}	Voltage Output swing		3.3		3.6	V
CMRR	Common-Mode Rejection Ratio ⁽¹⁾	$-2\text{V} < V_{CM} < 0.4\text{V}$		-110		dB
Gain	Gain	OUT / V_{IN}	48.5	49.25	50	V/V
V_{OS}	Output-Referred Offset Voltage	$V_{OS_REF} = 3.3\text{V}$	155	215	280	mV
Gain _{TC}	Gain Temperature Coefficient ⁽¹⁾	$[(\Delta\text{Gain}/50) / \Delta T] * 10^6$	-60	-20	10	ppm/ $^\circ\text{C}$
V_{OS-TC}	Output Offset Temperature Coefficient ⁽¹⁾		-50		50	$\mu\text{V}/^\circ\text{C}$
Gain _{VOS}	Offset Reference Gain	V_{OS} / V_{OS_REF}		0.06515		V/V
BW	-3 dB Bandwidth ⁽¹⁾	No load		4		kHz

Notes:

(1) This parameter is not tested in production.

Typical Characteristics

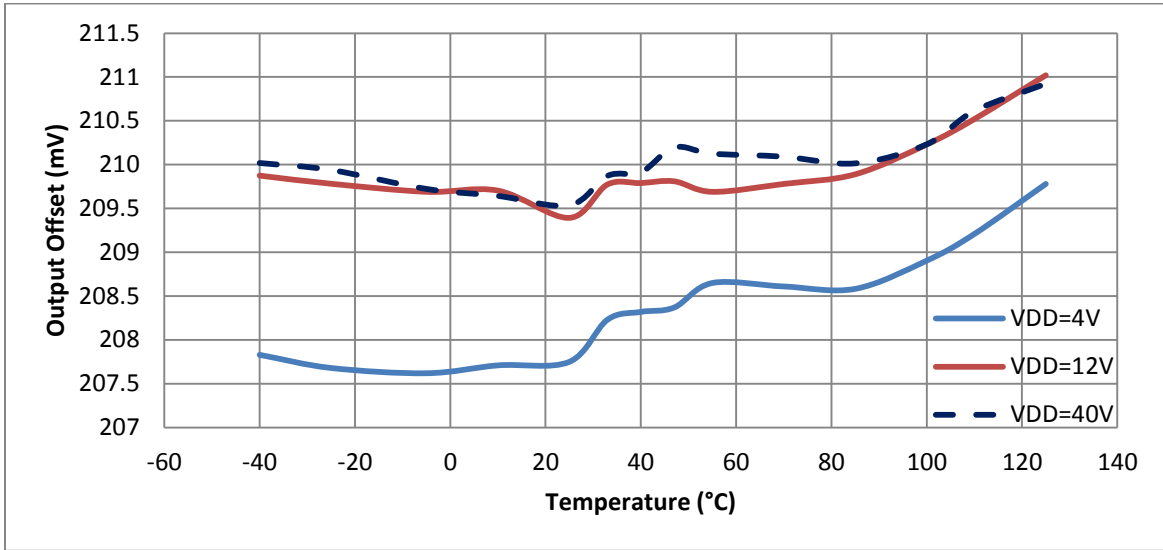


Figure 3: Offset Voltage vs Temperature

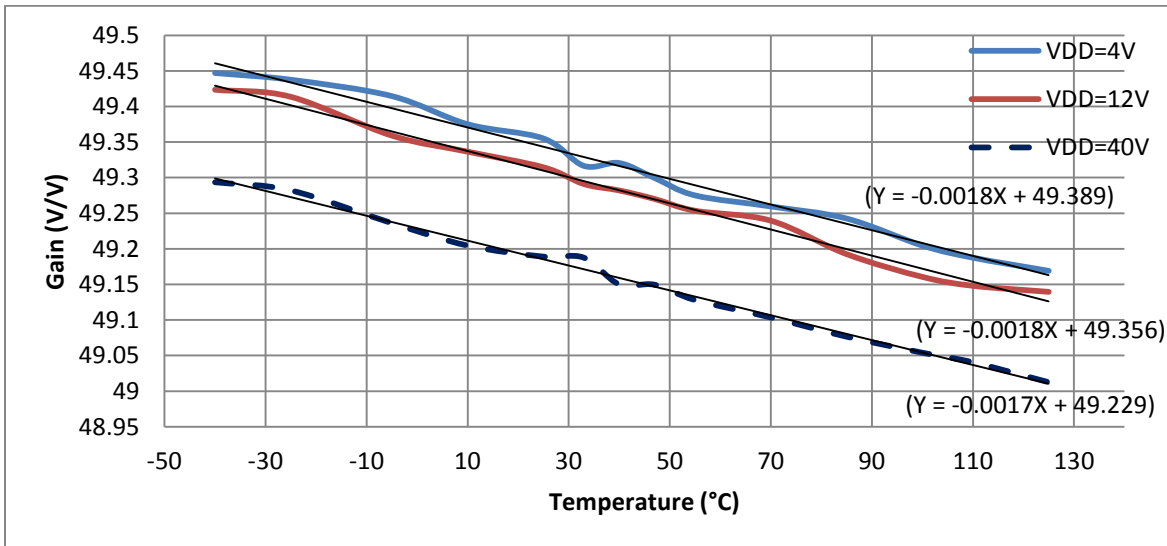


Figure 4: Gain vs Temperature

Operational Modes

The TS94033 is a low power, low offset high-side chopper-stabilized current sense amplifier. The amplifier is supplied on the high-side from the VDD pin and a sub-regulated supply that is generated at the VDDR pin. It is necessary for good supply rejection to have a bypass capacitor, C_{VDDR} closely-coupled between the VDD and VDDR pins.

The INP and INM pins are used to sense the voltage drop across a current-sensing resistor. Though it is usually the case that the INP pin would be connected to the VDD pin, the common-mode voltage can extend above and below VDD as specified by the V_{CM} parameter.

The EN pin may be used to set the device into a low-quiescent current mode when asserted low.

A zero-current output offset is set by providing a bias voltage on the VOS_REF pin. The zero-current offset voltage can be determined by the following relation:

$$V_{OS} = 0.065152 * V_{OS_REF}$$

The output voltage at the VOUT pin is referenced to the VSS pin. The VSS pin should be closely coupled to the circuit monitoring this voltage. The VOS_REF should be bypassed to this VSS as well.

Application Schematic

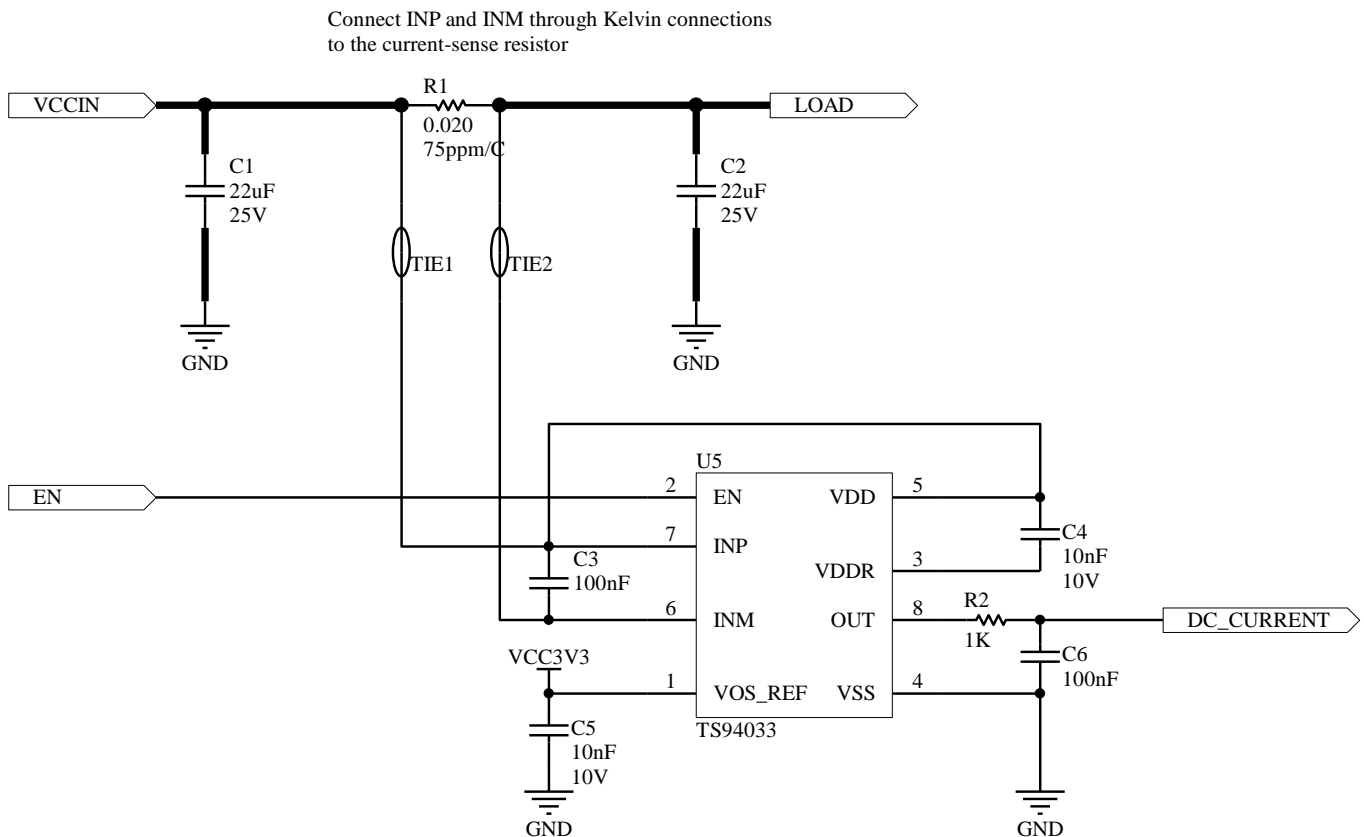
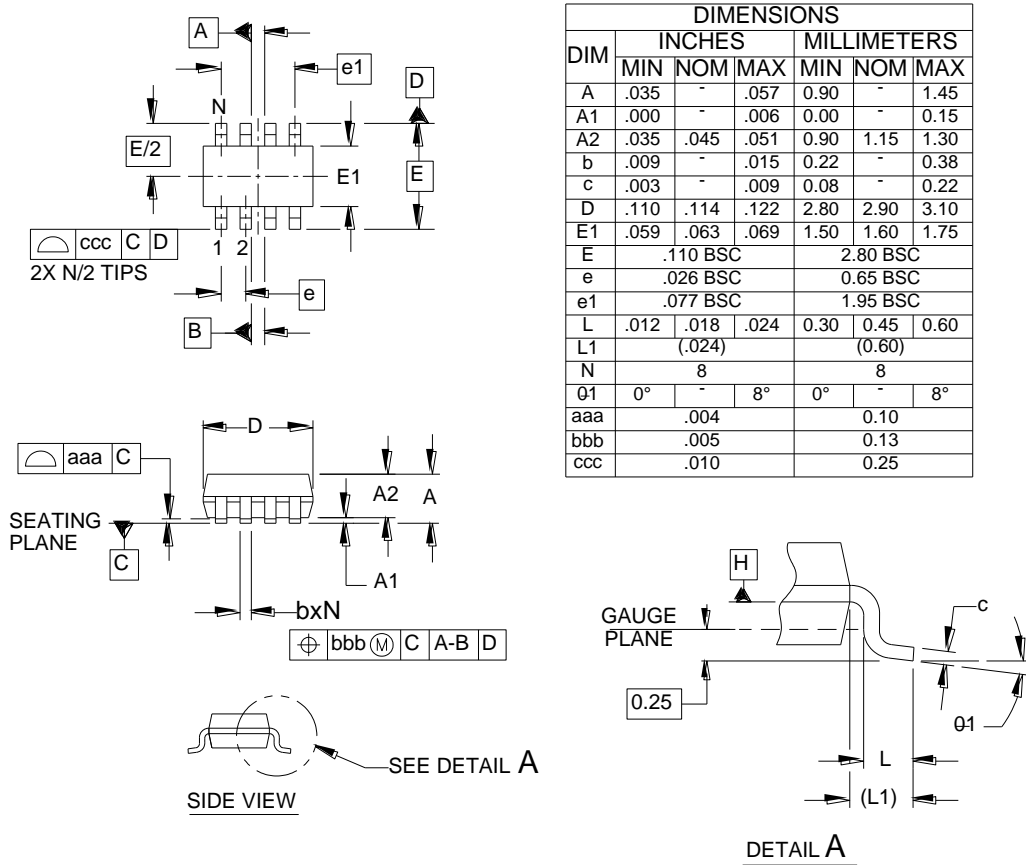


Figure 5: Standard Configuration

Package Information

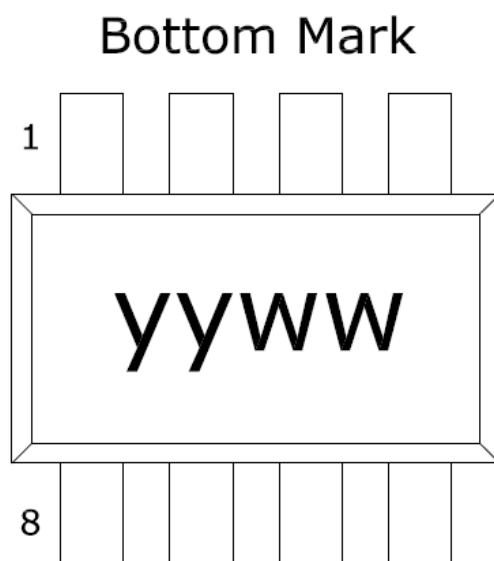
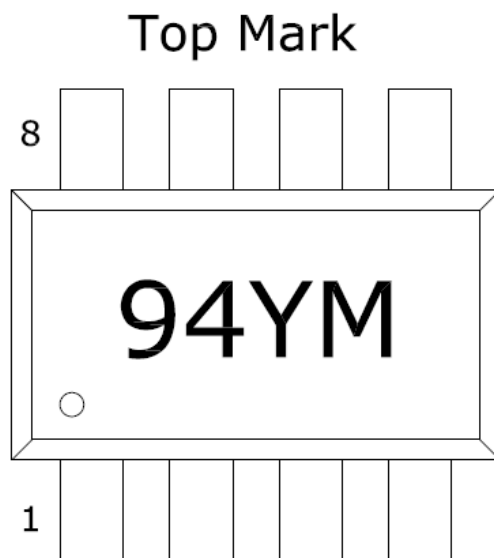


NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-178, VARIATION BA.

Figure 6: Package Outline Drawing

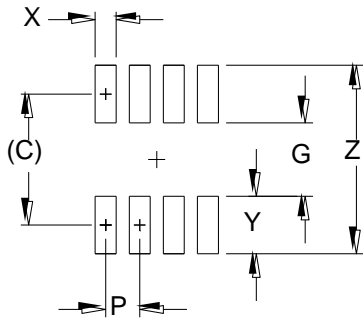
Package Information (continued)



Top Mark:
94YM = Product Marking

Bottom Mark:
yy = year
ww = week

Figure 7: Device Symbolization



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.026	0.65
X	.016	0.40
Y	.043	1.10
Z	.142	3.60

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Figure 8: Recommended Board Layout Land Pattern

Ordering Information

Device Part Number	Description	8-pin SOT-23 Package
TS94033SKTRC	Current Sense Amplifier	Tape & Reel (3000 parts/reel)



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