High Precision ±10 V Reference

AD688

FEATURES

±10 V tracking outputs
Kelvin connections
Low tracking error: 1.5 mV
Low initial error: 2.0 mV
Low drift: 1.5 ppm/°C
Low noise: 6 µV p-p
Flexible output force and sense terminals
High impedance ground sense
Wide body SOIC and CERDIP packages

GENERAL DESCRIPTION

The AD688 is a high precision ±10 V tracking reference. Low tracking error, low initial error, and low temperature drift give the AD688 reference absolute ±10 V accuracy performance previously unavailable in monolithic form. The AD688 uses a proprietary ion-implanted buried Zener diode, and laser wafer drift trimming of high stability thin-film resistors to provide outstanding performance.

The AD688 includes the basic reference cell and three additional amplifiers. The amplifiers are laser-trimmed for low offset and low drift and maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high current loads, delivering the full accuracy of the AD688 where it is required in the application circuit.

The low initial error allows the AD688 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD688 can provide a known voltage for system calibration; the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD688 and calibration software.

The AD688 is available in commercial version. Specified over the −40°C to +85°C temperature range, the AD688 is offered in wide body 16-lead SOIC and 16-lead CERDIP packages,

FUNCTIONAL BLOCK DIAGRAM

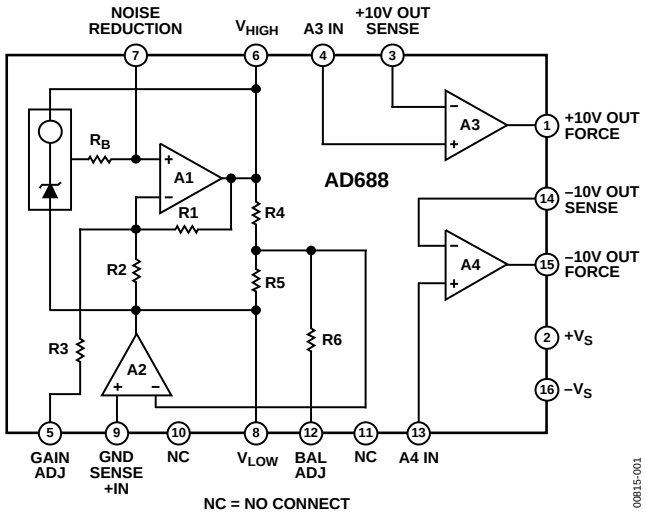

Figure 1.

PRODUCT HIGHLIGHTS

1. Precision Tracking. The AD688 offers precision tracking ±10 V Kelvin output connections with no external components. Tracking error is less than 1.5 mV and fine-trim is available for applications requiring exact symmetry between the +10 V and −10 V outputs.

2. Accuracy. The AD688 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the Zener or the buffer amplifiers and thus does not increase the temperature drift.

3. Low output noise. Output noise of the AD688 is low—typically 6 µV p-p. A pin is provided for broadband noise filtering using an external capacitor.

Rev. B

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AD688* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

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DOCUMENTATION

Application Notes

- AN-713: The Effect of Long-Term Drift on Voltage References

Data Sheet

- AD688: High Precision ±10 V Reference Data Sheet
- AD688: Military Data Sheet

DESIGN RESOURCES

- AD688 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SAMPLE AND BUY

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TECHNICAL SUPPORT

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DOCUMENT FEEDBACK

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REVISION HISTORY

3/05—Rev. A to Rev. B

Updated Format ..... Universal
Added AD688ARWZ ..... Universal
Removed AD688SQ ..... Universal
Updated Outline Dimensions 13
Changes to Ordering Guide 13

SPECIFICATIONS

Typical @ 25°C, +10 V output, V_S = ±15 V unless otherwise noted.[1] Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

Table 1.

	AD688AQ			AD688BQ			AD688ARWZ			
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
OUTPUT VOLTAGE ERROR										
+10 V, −10 V Outputs	**−5**		**+5**	**−2**		**+2**	**−4**		**+4**	mV
±10 V TRACKING ERROR	**−3**		**+3**	**−1.5**		**+1.5**	**−1.5**		**+1.5**	mV
OUTPUT VOLTAGE DRIFT										
+10 V, −10 V Outputs										
0°C to +70°C (A, B)		±2		**−1.5**		**+1.5**				ppm/°C
−40°C to +85°C (A, B)	**−3**		**+3**	**−3**		**+3**	**−8**		**+8**	ppm/°C
GAIN ADJ AND BAL ADJ[2]										
Trim Range		± 5			±5			±5		mV
Input Resistance		150			150			150		kΩ
LINE REGULATION										
T_{MIN} to T_{MAX}[3]	**−200**		**+200**	**−200**		**+200**	**−200**		**+200**	µV/V
LOAD REGULATION										
T_{MIN} to T_{MAX}										
+10 V Output, 0<I_{OUT}<10 mA			±50			±50			±50	µV/mA
−10 V Output, −10<I_{OUT}<0 mA			±50			±50			±50	µV/mA
SUPPLY CURRENT										
T_{MIN} to T_{MAX}		9	**12**		9	**12**			**12**	mA
Power Dissipation		270	360		270	360			360	mW
OUTPUT NOISE (ANY OUTPUT)										
0.1 Hz to 10 Hz		6			6			6		µV p-p
Spectral Density, 100 Hz		140			140			140		nV√Hz
LONG-TERM STABILITY (@ 25°C)		15			15			15		ppm/1000 hours
BUFFER AMPLIFIERS										
Offset Voltage		100			100			100		µV
Offset Voltage Drift		1			1			1		µV/°C
Bias Current		20			20			20		nA
Open-Loop Gain		110			110			110		dB
Output Current A3, A4	**−10**		**+10**	**−10**		**+10**	**−10**		**+10**	mA
Common-Mode Rejection (A3, A4)										
V_{CM} = 1 V p-p		100			100			100		dB
Short-Circuit Current		50			50			50		mA
TEMPERATURE RANGE										
Specified Performance										
A, B Grades	−40		+85	−40		+85	−40		+85	°C

[1] See Figure 4 for output configuration.
[2] Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.
[3] Test Conditions: $+V_S$ = +18 V, $-V_S$ = −18 V; $+V_S$ = +13.5 V, $-V_S$ = −13.5 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
$+V_S$ to $-V_S$	36 V
Power Dissipation (25°C)	
Q Package	600 mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 s)	+300°C
Package Thermal Resistance	
Q (θ_{JA}/θ_{JC})	120/35°C/W
Output Protection:	
All outputs safe if shorted to ground	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

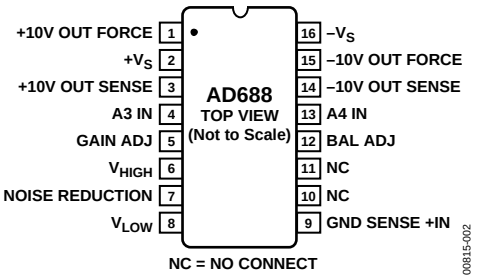


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	+10 V OUT FORCE	+10 V Output with Kelvin Force. Connect to Pin 3.
2	$+V_S$	Positive Power Supply.
3	+10 V OUT SENSE	+10 V Output with Kelvin Sense. Connect to Pin 1.
4	A3 IN	+ Input to A3. Connect to V_{HIGH}, Pin 6.
5	GAIN ADJ	Reference Gain Adjustment for Calibration. See the Calibration section.
6	V_{HIGH}	Unbuffered Reference High Output.
7	NOISE REDUCTION	Noise Filtering Pin. Connect external 1 µF capacitor to ground to reduce output noise, see the Noise Performance and Reduction section. May be left open.
8	V_{LOW}	Unbuffered Reference Low Output.
9	GND SENSE +IN	Gound with Kelvin Sense.
10	NC	No Connection. Leave floating.
11	NC	No Connection. Leave floating.
12	BAL ADJ	Reference Centering Adjustment for Calibration. See the Calibration section.
13	A4 IN	+ Input to A4. Connect to V_{LOW}, Pin 8.
14	−10 V OUT SENSE	−10 V Output with Kelvin Sense. Connect to Pin 15.
15	−10 V OUT FORCE	−10 V Output with Kelvin Force. Connect to Pin 14.
16	$-V_S$	Negative Power Supply.

THEORY OF OPERATION

The AD688 consists of a buried Zener diode reference, amplifiers and associated thin-film resistors as shown in Figure 3. The temperature compensation circuitry provides the device with a temperature coefficient of 1.5 ppm/°C or less.

Amplifier A1 performs several functions. A1 primarily acts to amplify the Zener voltage to the required 20 V. In addition, A1 also provides for external adjustment of the 20 V output through Pin 5 (GAIN ADJ). Using the bias compensation resistor between the Zener output and the noninverting input to A1, a capacitor can be added at the noise reduction pin (Pin 7) to form a low-pass filter and reduce the noise contribution of the Zener to the circuit. Two matched 12 kΩ nominal thin-film resistors (R4 and R5) divide the 20 V output in half.

Ground sensing for the circuit is provided by amplifier A2. The noninverting input (Pin 9) senses the system ground and forces the midpoint of resistors R4 and R5 to be a virtual ground. Pin 12 (BAL ADJ) can be used for fine adjustment of this midpoint transfer.

Amplifiers A3 and A4 are internally compensated and are used to buffer the voltages at Pin 6 and Pin 8 as well as to provide a full Kelvin output. Thus, the AD688 has a full Kelvin capability by providing the means to sense a system ground, and forced and sensed outputs referenced to that ground.

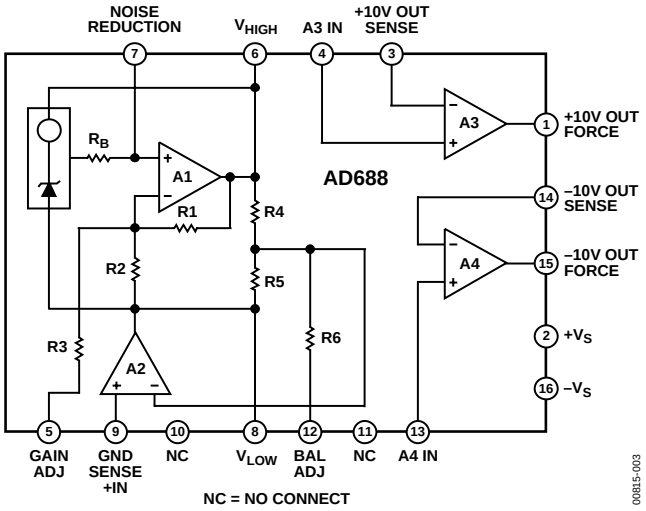


Figure 3. Functional Block Diagram

APPLICATIONS

The AD688 can be configured to provide ±10 V reference outputs as shown in Figure 4. The architecture of the AD688 provides ground sense and uncommitted output buffer amplifiers which offer the user a great deal of functional flexibility. The AD688 is specified and tested in the configuration shown in Figure 4. The user may choose to take advantage of other configuration options available with the AD688; however performance in these configurations is not guaranteed to meet the stringent data sheet specifications.

Unbuffered outputs are available at Pin 6 and Pin 8. Loading of these unbuffered outputs will impair circuit performance.

Amplifiers A3 and A4 can be used interchangeably. However, the AD688 is tested (and the specifications are guaranteed) with the amplifiers connected as indicated in Figure 4. When either A3 or A4 is unused, its output force and sense pins should be connected and the input tied to ground.

Two outputs of the same voltage polarity may be obtained by connecting both A3 and A4 to the appropriate unbuffered output on Pin 6 or Pin 8. Performance in these dual output configurations will typically meet data sheet specifications.

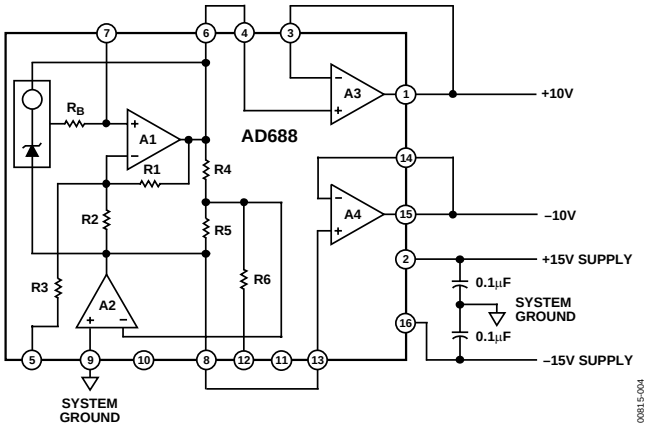


Figure 4. +10 V and −10 V Outputs

CALIBRATION

Generally, the AD688 will meet the requirements of a precision system without additional adjustment. Initial output voltage error of 2 mV and output noise specs of 6 μV p-p allow for accuracies of 12 to 16 bits. However, in applications where an even greater level of accuracy is required, additional calibration may be called for. The provision for trimming has been made through the use of the GAIN ADJ and BAL ADJ pins (Pin 5 and Pin 12, respectively).

The AD688 provides a precision 20 V span with a center tap which is used with the buffer and ground sense amplifiers to achieve the ±10 V output configuration. GAIN ADJ and BAL ADJ can be used to trim the magnitude of the 20 V span voltage and the position of the center tap within the span. The gain adjustment should be performed first. Although the trims are not interactive within the device, the gain trim will move the balance trim point as it changes the magnitude of the span.

Figure 5 shows the gain and balance trims of the AD688. A 100 kΩ 20-turn potentiometer is used for each trim. The potentiometer for the gain trim is connected between Pin 6 (V_{HIGH}) and Pin 8 (V_{LOW}) with the wiper connected to Pin 5 (GAIN ADJ). The potentiometer is adjusted to produce exactly 20 V between Pin 1 and Pin 15, the amplifier outputs. The balance potentiometer, also connected between Pin 6 and Pin 8 with the wiper to Pin 12 (BAL ADJ), is then adjusted to center the span from +10 V to −10 V.

Input impedance on both the GAIN ADJ and the BAL ADJ pins is approximately 150 kΩ. The gain adjustment trim network effectively attenuates the 20 V across the trim potentiometer by a factor of about 1150 to provide a trim range of −5.8 mV to +12.0 mV with a resolution of approximately 900 μV/turn (20-turn potentiometer). The balance adjustment trim network attenuates the trim voltage by a factor of about 1250, providing a trim range of ±8 mV with a resolution of 800 μV/turn.

Trimming the AD688 introduces no additional errors over temperature, so precision potentiometers are not required.

When balance adjustment is not necessary, Pin 12 should be left floating. If gain adjustment is not required, Pin 5 should also be left floating.

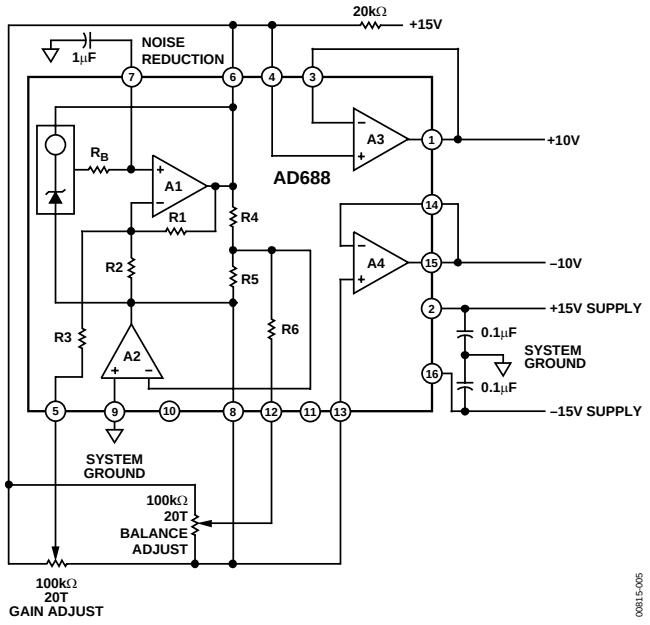


Figure 5. Gain and Balance Adjustment with Noise Reduction

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD688 is typically less than 6 μV p-p over the 0.1 Hz to 10 Hz band. Noise in a 1 MHz bandwidth is approximately 840 μV p-p. The dominant source of this noise is the buried Zener which contributes approximately 140 nV/√Hz. In comparison, the op amp's contribution is negligible. Figure 6 shows the 0.1 Hz to 10 Hz noise of a typical AD688.

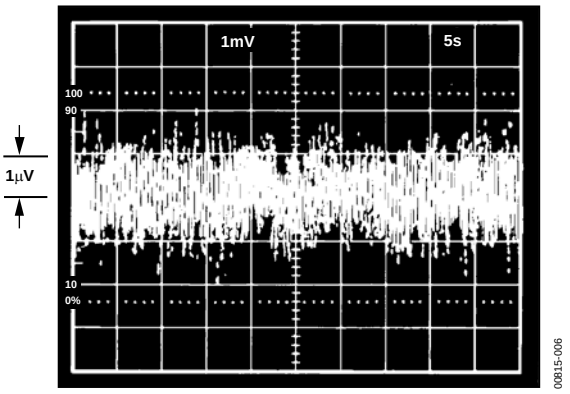


Figure 6. 0.1 Hz to 10 Hz Noise

If further noise reduction is desired, an optional capacitor can be added between the noise reduction pin and ground as shown in Figure 5. This will form a low-pass filter with the 5 kΩ R_B on the output of the Zener cell. A 1 μF capacitor will have a 3 dB point at 32 Hz and will reduce the high frequency noise (to 1 MHz) to about 250 μV p-p. Figure 7 shows the 1 MHz noise of a typical AD688 both with and without a 1 μF capacitor.

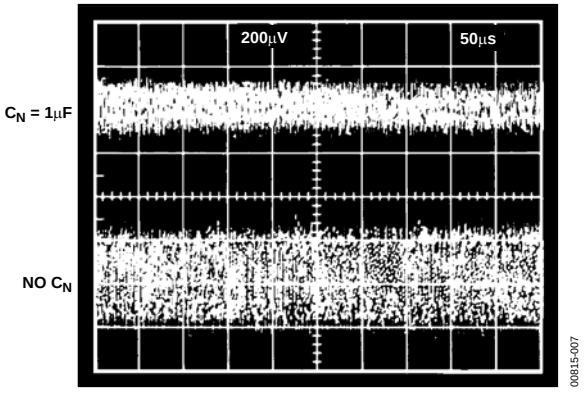


Figure 7. Effect of 1 μF Noise Reduction Capacitor on Broadband Noise

TURN ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error is the turn on settling time. Two components normally associated with this are: time for active circuits to settle and time for thermal gradients on the chip to stabilize. Figure 8 and Figure 9 show the turn on characteristics of the AD688. They show the settling time to be about 600 μs. Note the absence of any thermal tails when the horizontal scale is expanded to 2 ms/cm in Figure 9.

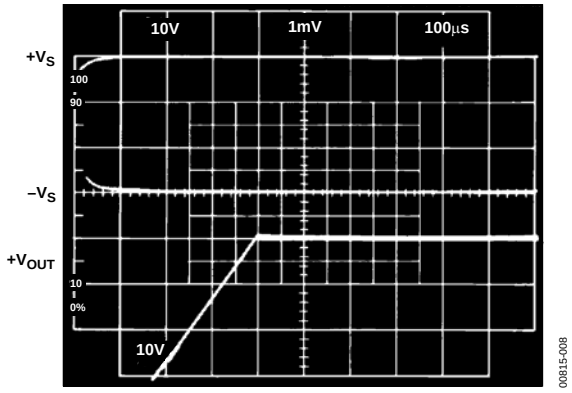


Figure 8. Turn On Characteristics: Electrical Turn On

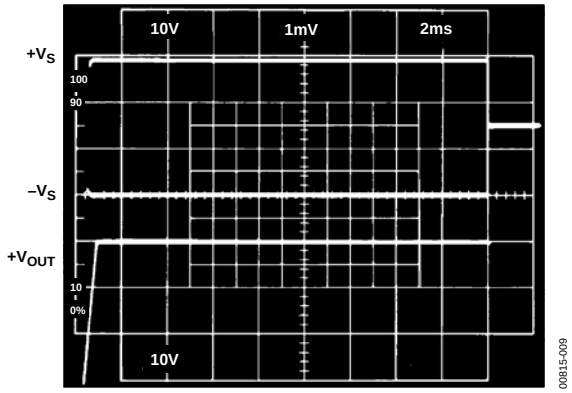


Figure 9. Turn On Characteristics: Extended Time Scale

Output turn on time is modified when an external noise reduction capacitor is used. When present, this capacitor presents an additional load to the internal Zener diode's current source, resulting in a somewhat longer turn on time. In the case of a 1 μF capacitor, the initial turn on time is approximately 100 ms (Figure 10).

When the noise reduction feature is used, a 20 kΩ resistor between Pin 6 and Pin 2 is required for proper startup.

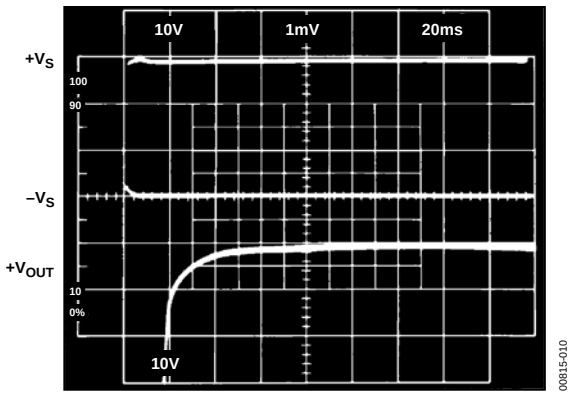


Figure 10. Turn On With 1 μF C_N

TEMPERATURE PERFORMANCE

The AD688 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Figure 11 shows the typical output voltage drift and illustrates the test methodology. The box in Figure 11 is bounded on the sides by the operating temperature extremes, and on top and bottom by the maximum and minimum +10 V output error voltages measured over the operating temperature range. The slopes of the diagonals drawn for both the +10 V and −10 V outputs determine the performance grade of the device.

$$\text{+10V OUTPUT SLOPE} = \text{T.C.} = \frac{E_{MAX} - E_{MIN}}{(T_{MAX} - T_{MIN}) \times 10 \times 10^{-6}}$$

$$= \frac{2.2\text{mV} - -3.2\text{mV}}{(85^{\circ}\text{C} - -40^{\circ}\text{C}) \times 10 \times 10^{-6}}$$

$$= 3\text{ppm}/^{\circ}\text{C}$$

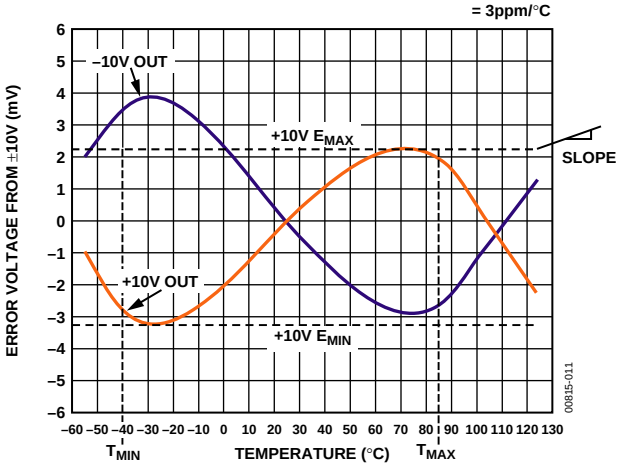


Figure 11. Typical AD688AQ Temperature Drift

Each AD688A and B grade unit is tested at −40°C, −25°C, 0°C, +25°C, +50°C, +70°C, and +85°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range will be contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale will change from device to device as initial error and the shape of the curve vary. Maximum height of the box for the appropriate temperature range is shown in Figure 12.

MAXIMUM OUTPUT CHANGE (mV)		
DEVICE GRADE	0 TO +70°C	–40°C TO +85°C
AD688AQ	1.40 (TYP)	3.75
AD688BQ	1.05	3.75
AD688ARWZ		4.0

00815-012

Figure 12. Maximum + 10 V or −10 V Output Change

Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD688 will produce curves similar to those in Figure 11, but output readings may vary depending on the test methods and equipment utilized.

KELVIN CONNECTIONS

Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. As seen in Figure 13a, the load current and wire resistance produce an error ($V_{ERROR} = R \times I_L$) at the load. The Kelvin connection of Figure 13b overcomes the problem by including the wire resistance within the forcing loop of the amplifier and sensing the load voltage. The amplifier corrects for any errors in the load voltage. In the circuit shown, the output of the amplifier would actually be at 10 V + V_{ERROR} and the voltage at the load would be the desired 10 V.

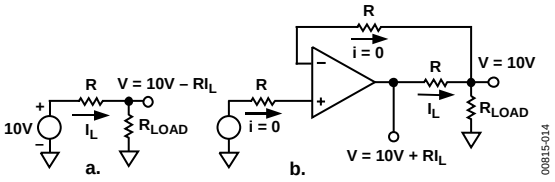


Figure 13. Advantage of Kelvin Connection

The AD688 has three amplifiers which can be used to implement Kelvin connections. Amplifier A2 is dedicated to the ground force-sense function while uncommitted amplifiers A3 and A4 are free for other force-sense chores.

In some applications, one amplifier may be unused. In such cases, the unused amplifier should be connected as a unity-gain follower (force and sense pins tied together) and the input should be connected to ground.

An unused amplifier may be used for other circuit functions as well. Figure 14 through Figure 19 show the typical performance of A3 and A4.

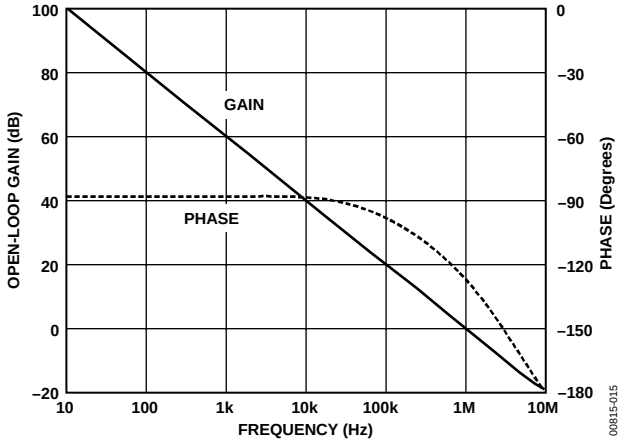


Figure 14. A3, A4 Open-Loop Frequency Response

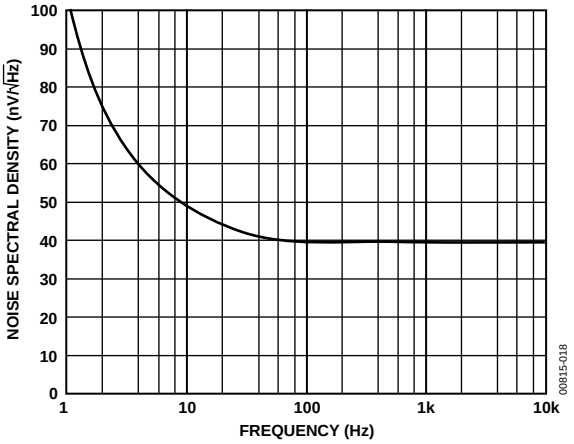


Figure 17. Input Noise Voltage Spectral Density

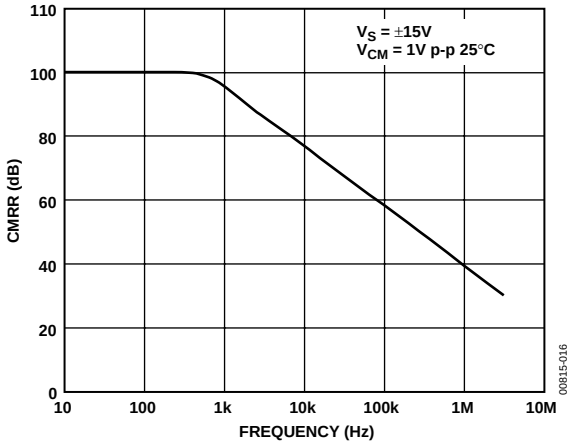


Figure 15. A3, A4 CMR vs. Frequency

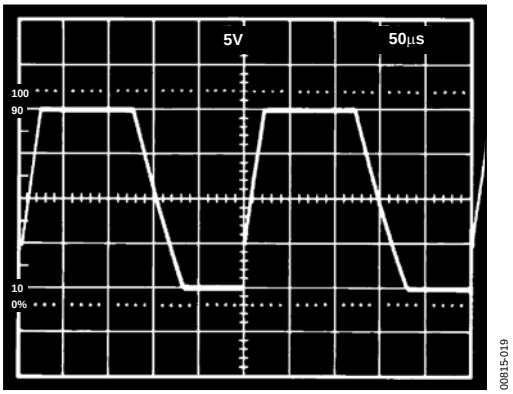


Figure 18. Unity-Gain Follower Pulse Response (Large Signal)

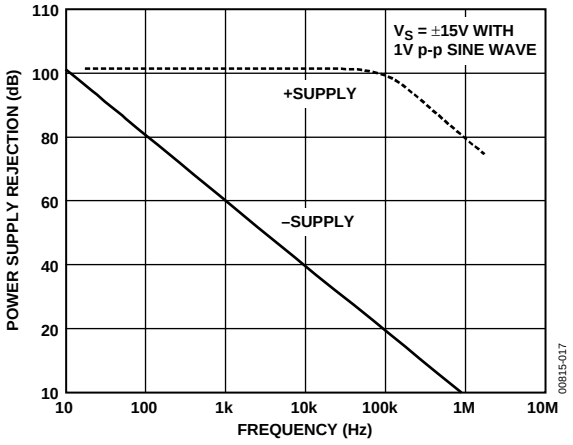


Figure 16. A3, A4 PSR vs. Frequency

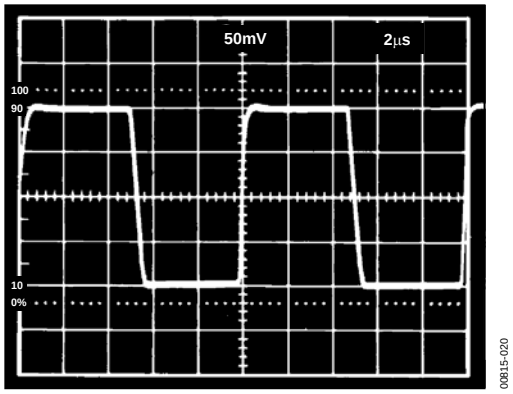


Figure 19. Unity-Gain Follower Pulse Response (Small Signal)

DYNAMIC PERFORMANCE

The output buffer amplifiers (A3 and A4) are designed to provide the AD688 with static and dynamic load regulation superior to less complete references.

Many A/D and D/A converters present transient current loads to the reference, and poor reference response can degrade the converter's performance.

Figure 20, Figure 21, and Figure 22 display the characteristic of the AD688 output amplifier driving a 0 mA to 10 mA load.

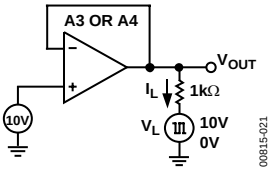


Figure 20. Transient Load Test Circuit

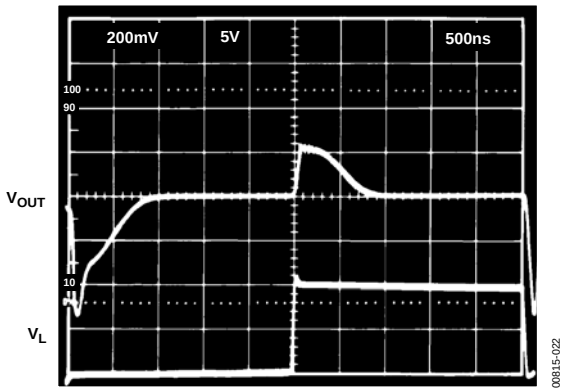


Figure 21. Large-Scale Transient Response

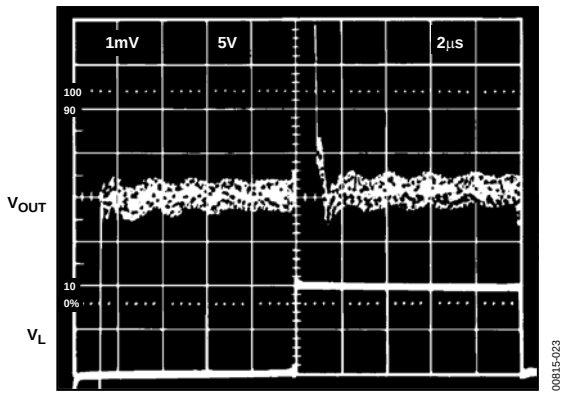


Figure 22. Fine-Scale Settling for Transient Load

Figure 23 and Figure 24 display the output amplifier characteristic driving a 5 mA to 10 mA load, a common situation found when the reference is shared among multiple converters or is used to provide bipolar offset current.

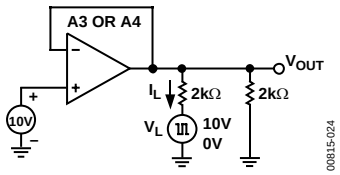


Figure 23. Transient and Constant Load Test Circuit

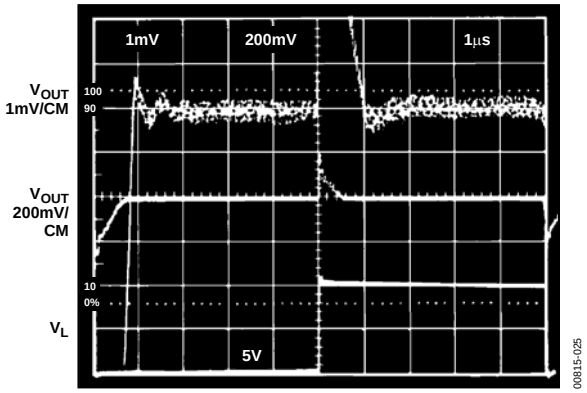


Figure 24. Transient Response 5 mA to 10 mA Load

In some applications, a varying load may be both resistive and capacitive in nature, or may be connected to the AD688 by a long capacitive cable. Figure 25 and Figure 26 display the output amplifier characteristics driving a 1000 pF, 0 mA to 10 mA load.

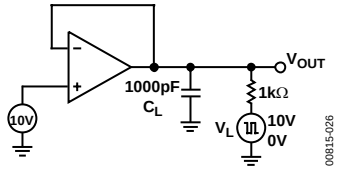


Figure 25. Capacitive Load Transient Response Test Circuit

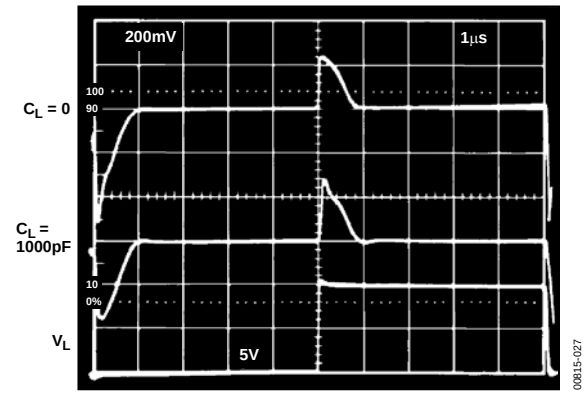


Figure 26. Output Response with Capacitive Load

Figure 27 and Figure 28 display the crosstalk between output amplifiers. The top trace shows the output of A4, dc-coupled and offset by 10 V, while the output of A3 is subjected to a 0 mA to 10 mA load current step. The transient at A4 settles in about 1 µs, and the load-induced offset is about 100 µV.

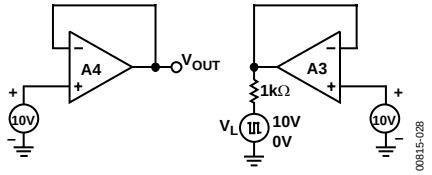


Figure 27. Load Crosstalk Test Circuit

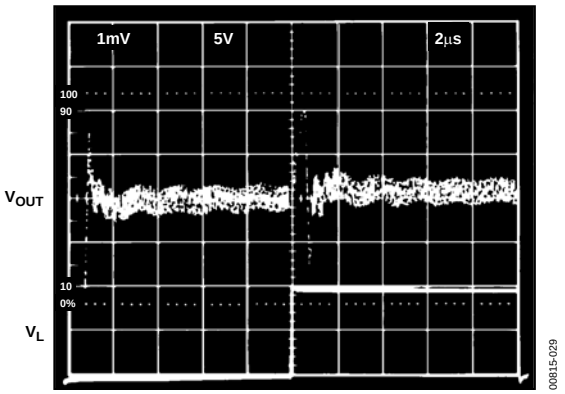


Figure 28. Load Crosstalk

Attempts to drive a large capacitive load (in excess of 1000 pF) may result in ringing or oscillation, as shown in the step response photo (Figure 29). This is due to the additional pole formed by the load capacitance and the output impedance of the amplifier, which consumes phase margin. The recommended method of driving capacitive loads of this magnitude is shown in Figure 30. The 150 Ω resistor isolates the capacitive load from the output stage, while the 10 kΩ resistor provides a dc feedback path and preserves the output accuracy. The 1 µF capacitor provides a high frequency feedback loop. The performance of this circuit is shown in Figure 31.

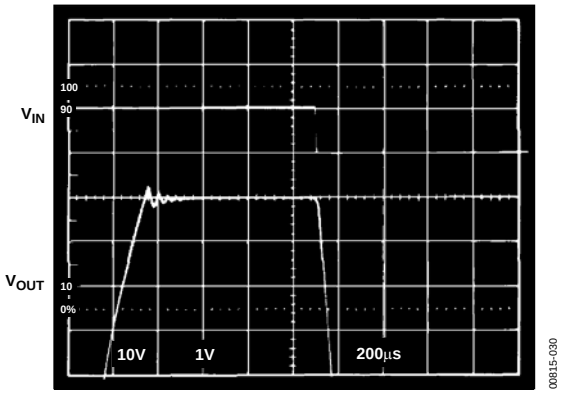


Figure 29. Output Amplifier Step Response, C_L = 1 µF

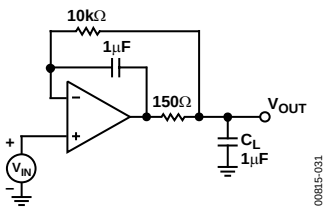


Figure 30. Compensation for Capacitive Loads

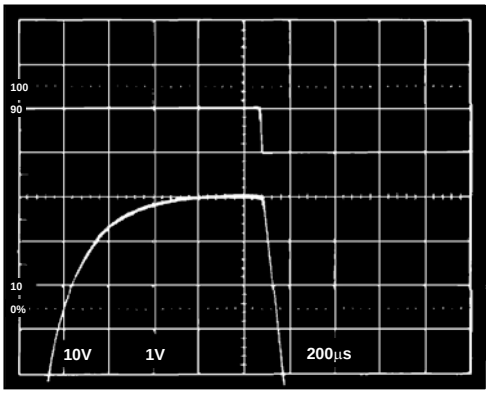


Figure 31. Output Amplifier Step Response Using Figure 30 Compensation

BRIDGE DRIVER CIRCUIT

The Wheatstone bridge is a common transducer. In its simplest form, a bridge consists of four 2-terminal elements connected to form a quadrilateral, a source of excitation connected along one of the diagonals and a detector comprising the other diagonal.

In this unipolar drive configuration, the output voltage of the bridge is riding on a common-mode voltage signal equal to approximately $V_{IN}/2$. Further processing of this signal may necessarily be limited to high common-mode rejection techniques such as instrumentation or isolation amplifiers. However, if the bridge is driven from a pair of bipolar supplies, then the common-mode voltage is ideally eliminated and the restrictions on any processing elements that follow are relaxed.

As shown in Figure 32, the AD688 is an excellent choice for the control element in a bipolar bridge driver scheme. Transistors Q1 and Q2 serve as series pass elements to boost the current drive capability to the 57 mA required by the typical 350 Ω bridge. A differential gain stage may still be required if the bridge balance is not perfect.

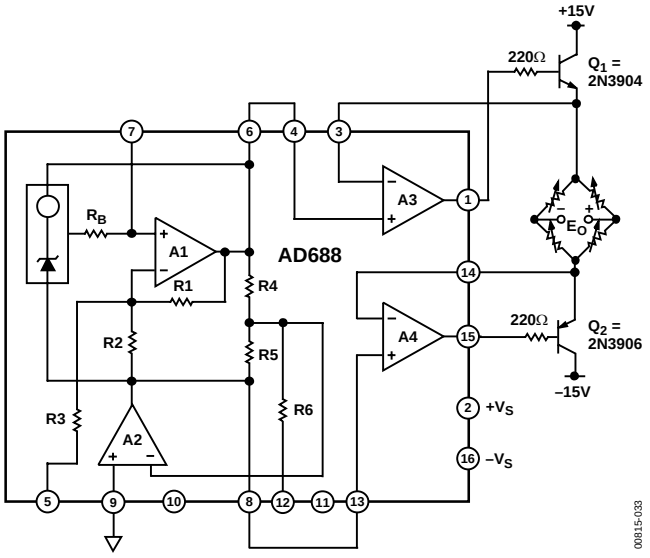
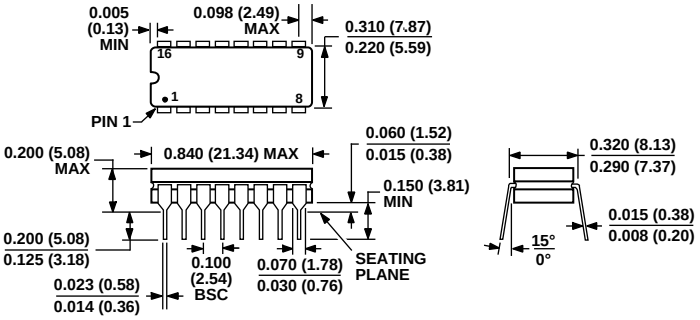


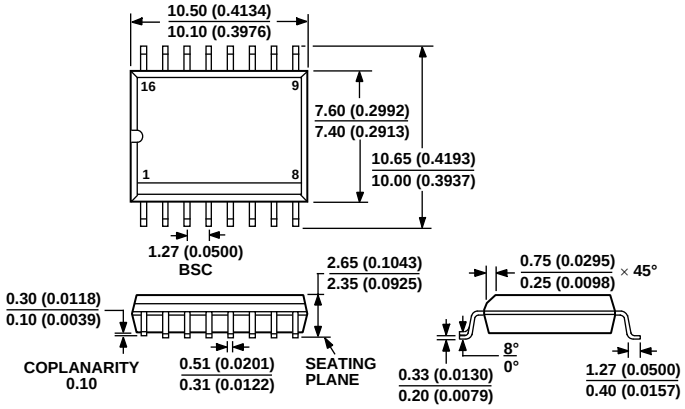
Figure 32. Bipolar Bridge Drive

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 33. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 34. 16-Lead Standard Small Outline Package [SOIC]
Wide Body
(RW-16)
Dimensions shown in millimeter and (inches)

ORDERING GUIDE

Model	Initial Error	Temperature Coefficient	Temperature Range	Package Description	Package Option
AD688AQ	5 mV	3 ppm/°C	−40°C to + 85°C	16-Lead CERDIP	Q-16
AD688BQ	2 mV	3 ppm/°C	−40°C to + 85°C	16-Lead CERDIP	Q-16
AD688ARWZ[1]	4 mV	8 ppm/°C	−40°C to + 85°C	16-Lead SOIC	RW-16

[1] Z = Pb-free part.

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C00815-0-3/05(B)