Document Number: A2T21S260-12S
Rev. 0, 8/2015

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 65 W RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2110 to 2170 MHz.

2100 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 1200 mA, P_{out} = 65 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	18.5	30.4	6.9	–32.6	–17
2140 MHz	18.6	30.3	6.8	–32.8	–13
2170 MHz	18.7	30.6	6.8	–32.0	–11

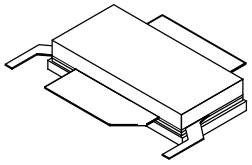
Features

- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

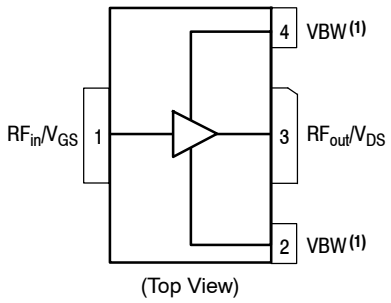
RoHS

A2T21S260-12SR3

2110–2170 MHz, 65 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-780S-2L2L



(Top View)

Figure 1. Pin Connections

1. Device cannot operate with V_{DD} current supplied through pin 2 and pin 4.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	346 3.1	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 65 W CW, 28 Vdc, I_{DQ} = 1200 mA, 2140 MHz	$R_{\theta JC}$	0.28	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 270 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1200 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.9	2.2	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.7 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

Functional Tests (4) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1200 mA, P_{out} = 65 W Avg., f = 2170 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Power Gain	G_{ps}	18.0	18.7	21.0	dB
Drain Efficiency	η_D	29.0	30.6	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.3	6.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	–32.0	–29.0	dBc
Input Return Loss	IRL	—	–11	–8	dB

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf and search for AN1955.
4. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 1200 mA, f = 2140 MHz, 12 μsec(on), 12% Duty Cycle					
VSWR 5:1 at 32 Vdc, 290 W Pulsed CW Output Power (0 dB Input Overdrive from 208 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1200 mA, 2110–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, Pulse	P1dB	—	208	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz bandwidth)	Φ	—	–20.9	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	90	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 65 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.015	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) (1)	ΔP1dB	—	0.013	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T21S260-12SR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel	NI-780S-2L2L

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

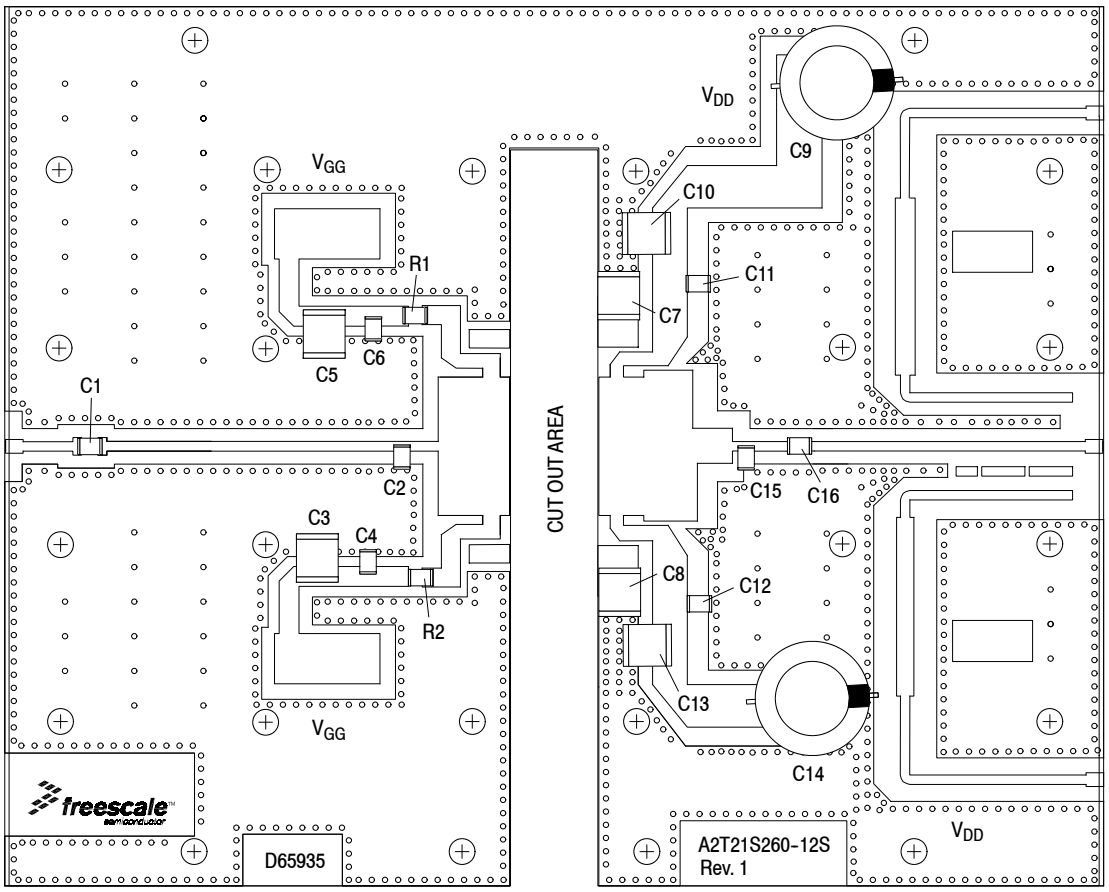


Figure 2. A2T21S260-12SR3 Test Circuit Component Layout

Table 6. A2T21S260-12SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C4, C6, C16	8.2 pF Chip Capacitors	ATC100B8R2CT500XT	ATC
C2	1.0 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C3, C5, C7, C8, C10, C13	10 uF Chip Capacitors	C5750X7S2A106M230KB	TDK
C9, C14	470 uF, 100 V Electrolytic Capacitors	MCGPR100V477M16X32-RH	Multicomp
C11, C12	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C15	0.1 pF Chip Capacitor	ATC600F0R1BT250XT	ATC
R1, R2	2.2 Ω, 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D65939	MTL

TYPICAL CHARACTERISTICS

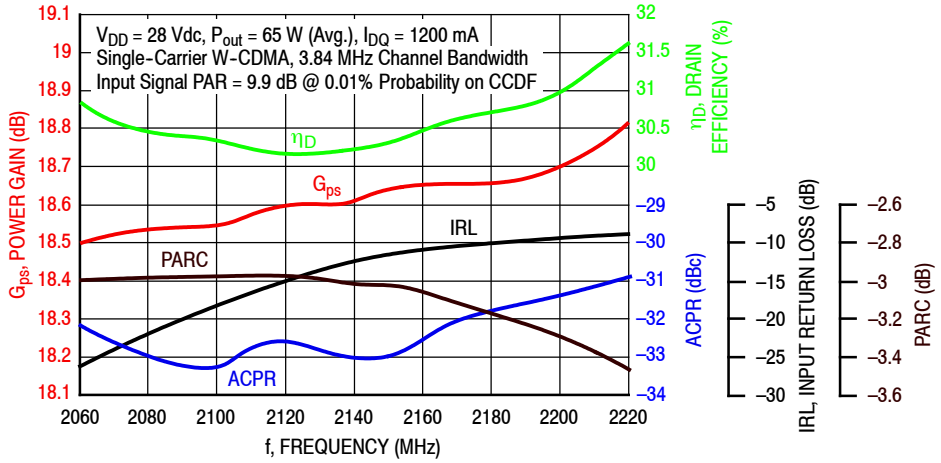


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 65 Watts Avg.

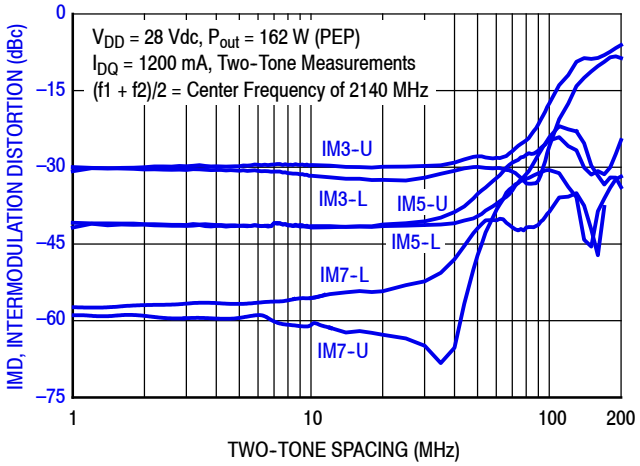


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

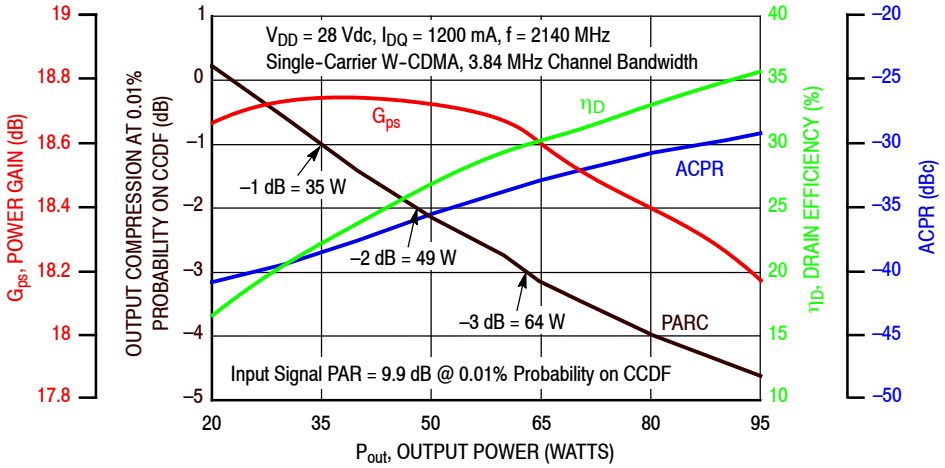


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

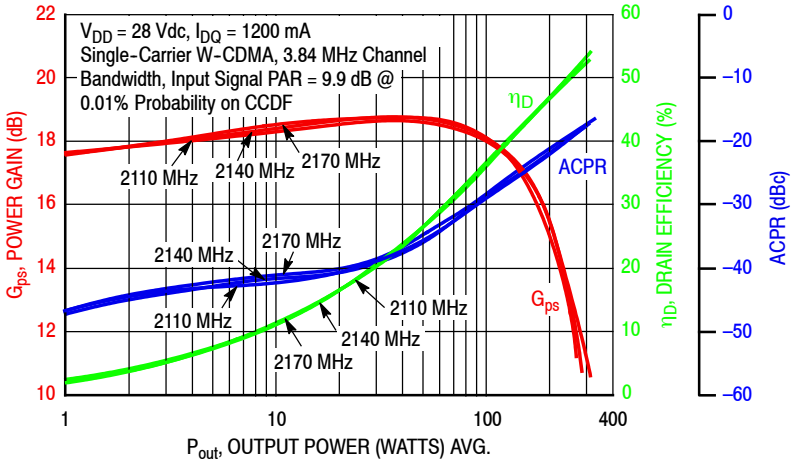


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

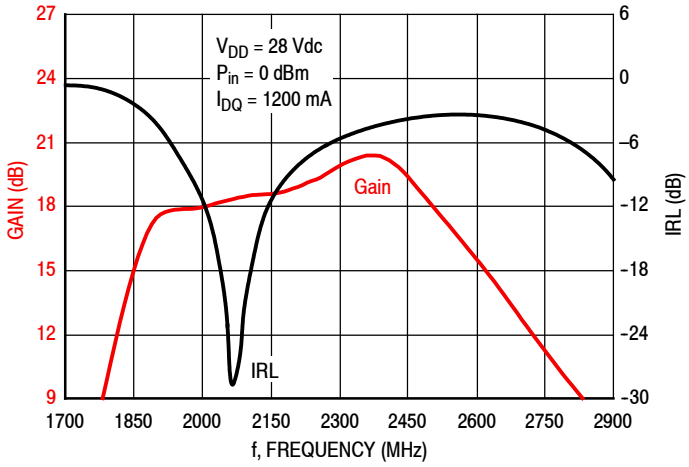


Figure 7. Broadband Frequency Response

Table 7. Load Pull Performance — Maximum Power Tuning — Class AB

V_{DD} = 28 Vdc, I_{DQ} = 1181 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.87 – j5.93	2.53 + j5.00	1.28 – j3.01	18.5	55.3	337	58.4	–19
2140	3.74 – j6.26	3.18 + j5.38	1.32 – j2.92	18.9	55.1	327	57.5	–20
2170	5.24 – j6.85	4.26 + j5.74	1.27 – j2.92	18.9	55.2	328	56.6	–20

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.87 – j5.93	2.60 + j5.30	1.28 – j3.18	16.3	56.0	397	60.1	–24
2140	3.74 – j6.26	3.35 + j5.73	1.35 – j3.09	16.7	55.8	383	59.0	–26
2170	5.24 – j6.85	4.63 + j6.10	1.33 – j3.13	16.7	55.8	384	58.5	–26

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

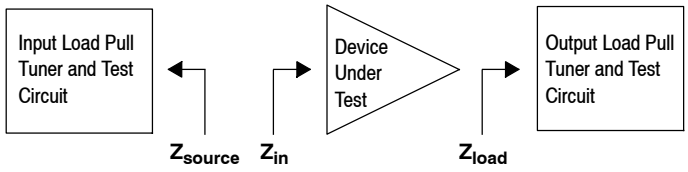
Table 8. Load Pull Performance — Maximum Drain Efficiency Tuning — Class AB

V_{DD} = 28 Vdc, I_{DQ} = 1181 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.87 – j5.93	2.62 + j5.21	2.58 – j1.61	21.3	53.2	208	70.0	–30
2140	3.74 – j6.26	3.31 + j5.58	2.27 – j1.61	21.4	53.3	213	67.7	–30
2170	5.24 – j6.85	4.49 + j5.93	2.03 – j1.59	21.5	53.4	220	68.5	–31

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.87 – j5.93	2.66 + j5.40	2.51 – j2.06	18.9	54.3	268	70.6	–35
2140	3.74 – j6.26	3.50 + j5.81	2.45 – j1.78	19.2	54.0	250	68.6	–38
2170	5.24 – j6.85	4.79 + j6.16	2.15 – j1.87	19.2	54.3	270	69.2	–37

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 2140 MHz — CLASS AB

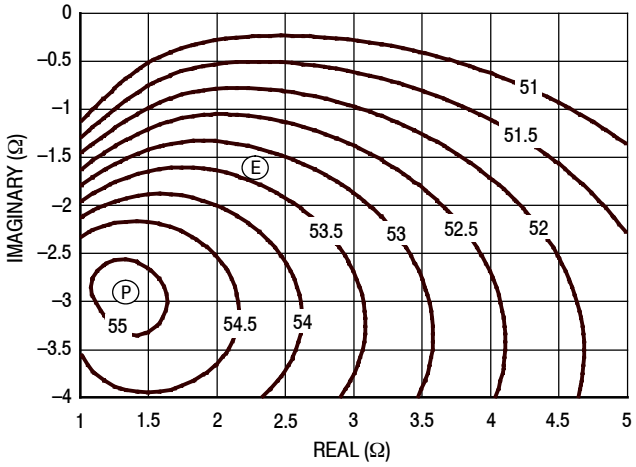


Figure 8. P1dB Load Pull Output Power Contours (dBm)

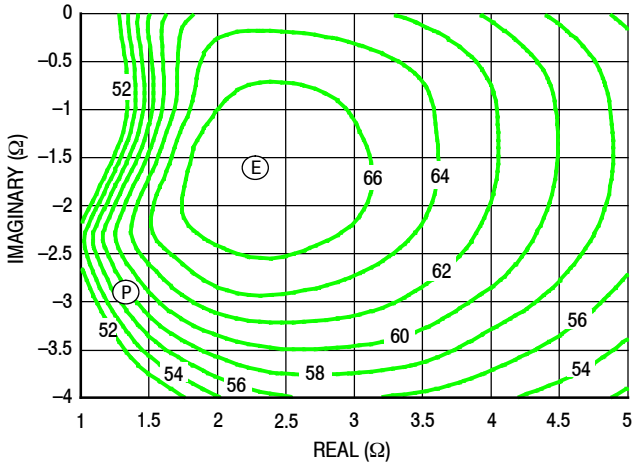


Figure 9. P1dB Load Pull Efficiency Contours (%)

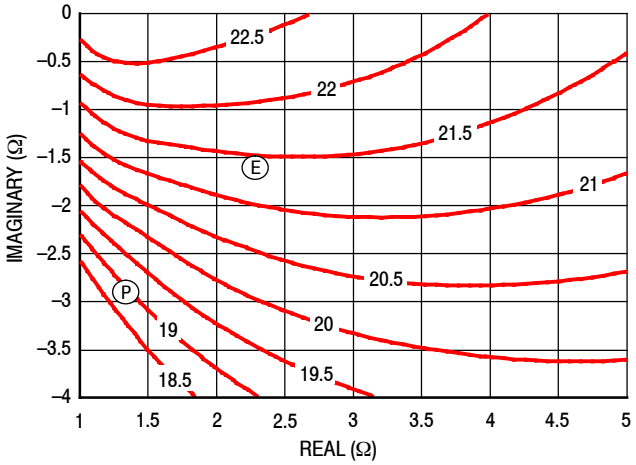


Figure 10. P1dB Load Pull Gain Contours (dB)

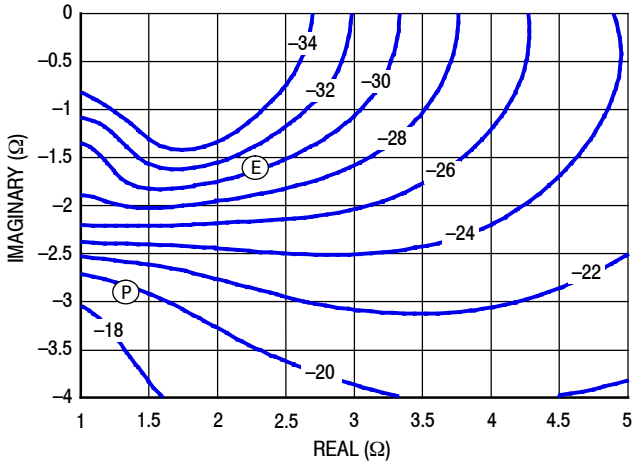


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 2140 MHz — CLASS AB

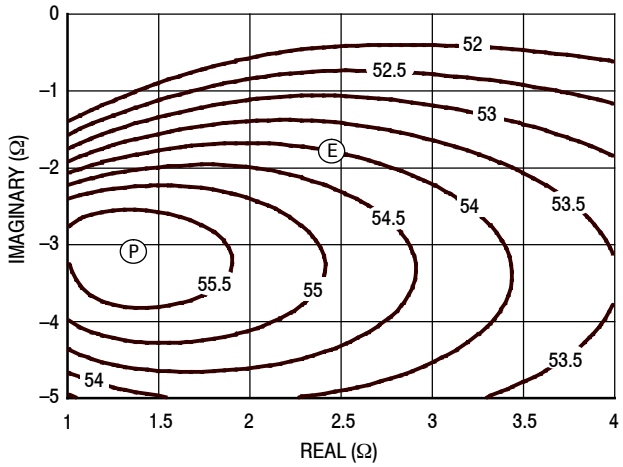


Figure 12. P3dB Load Pull Output Power Contours (dBm)

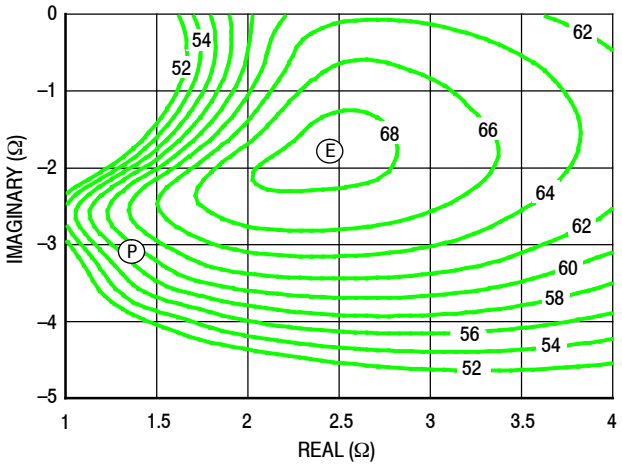


Figure 13. P3dB Load Pull Efficiency Contours (%)

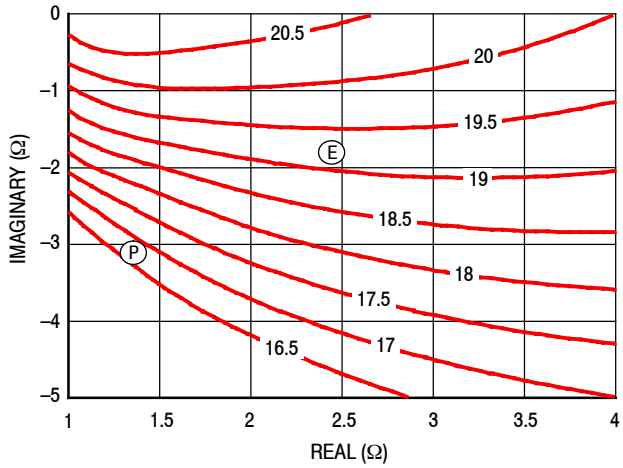


Figure 14. P3dB Load Pull Gain Contours (dB)

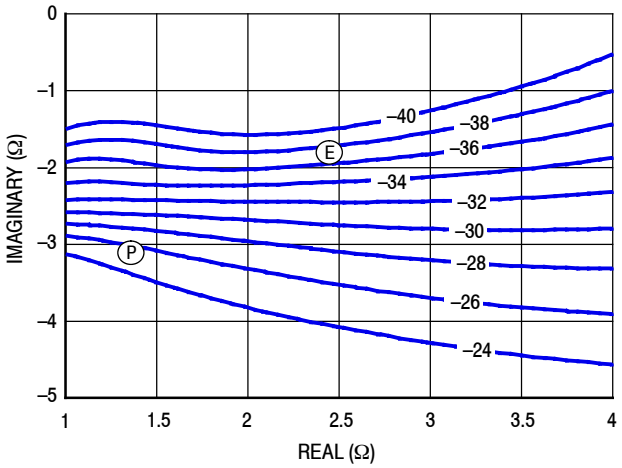


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

Table 9. Load Pull Performance — Maximum Power Tuning — Class C

V_{DD} = 28 Vdc, V_{GSB} = 0.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.40 – j4.69	2.19 + j4.95	1.11 – j3.01	15.1	55.3	341	56.8	–30
2140	3.16 – j5.17	2.83 + j5.43	1.15 – j2.88	15.3	55.3	336	56.9	–31
2170	4.24 – j5.24	3.94 + j5.93	1.13 – j2.89	15.2	55.3	338	56.5	–31

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.40 – j4.69	2.35 + j5.22	1.33 – j3.21	13.2	55.9	393	61.8	–37
2140	3.16 – j5.17	3.15 + j5.73	1.17 – j3.05	13.1	56.0	394	58.4	–38
2170	4.24 – j5.24	4.50 + j6.23	1.15 – j3.05	13.1	56.0	396	58.9	–37

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

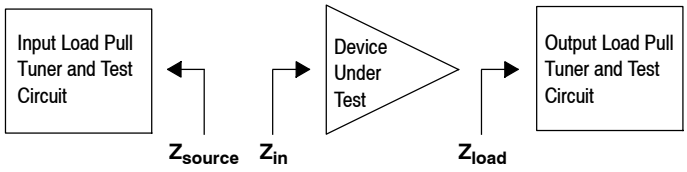
Table 10. Load Pull Performance — Maximum Drain Efficiency Tuning — Class C

V_{DD} = 28 Vdc, V_{GSB} = 0.8 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.40 – j4.69	1.98 + j4.94	2.73 – j2.04	16.4	53.5	223	69.7	–39
2140	3.16 – j5.17	2.59 + j5.44	2.50 – j1.84	16.4	53.4	220	68.1	–40
2170	4.24 – j5.24	3.61 + j5.98	2.33 – j1.78	16.3	53.5	226	69.0	–39

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.40 – j4.69	2.20 + j5.20	2.96 – j2.28	14.2	54.0	250	69.6	–47
2140	3.16 – j5.17	2.94 + j5.73	2.73 – j1.99	14.2	53.9	247	68.1	–49
2170	4.24 – j5.24	4.16 + j6.27	2.56 – j1.69	14.2	53.8	241	69.3	–50

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 2140 MHz — CLASS C

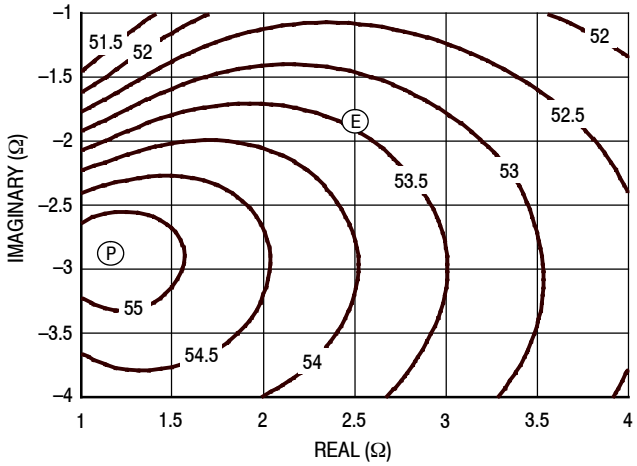


Figure 16. P1dB Load Pull Output Power Contours (dBm)

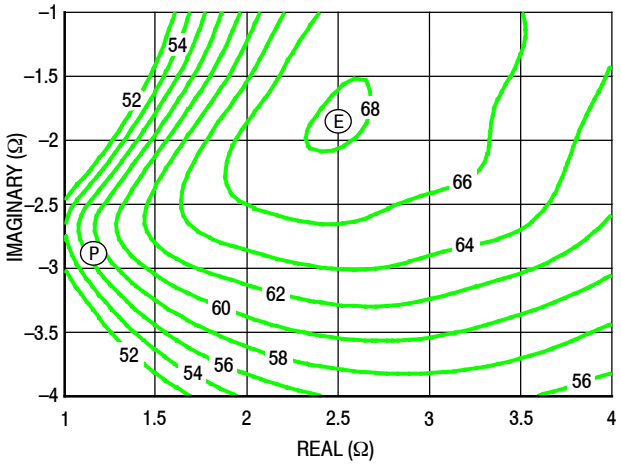


Figure 17. P1dB Load Pull Efficiency Contours (%)

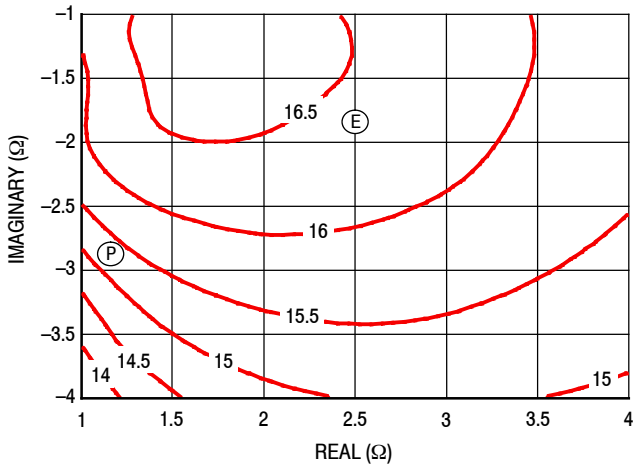


Figure 18. P1dB Load Pull Gain Contours (dB)

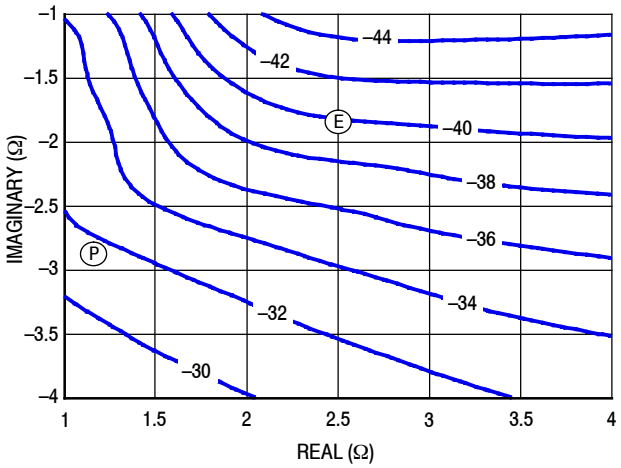


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2140 MHz — CLASS C

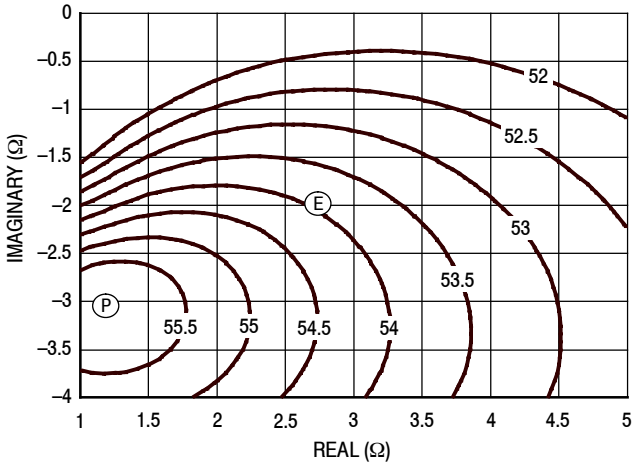


Figure 20. P3dB Load Pull Output Power Contours (dBm)

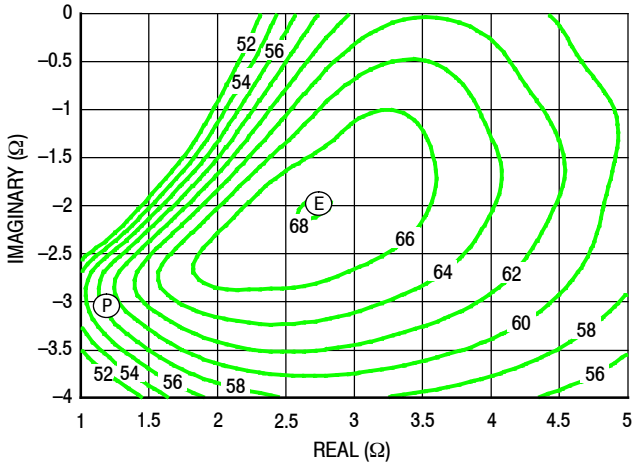


Figure 21. P3dB Load Pull Efficiency Contours (%)

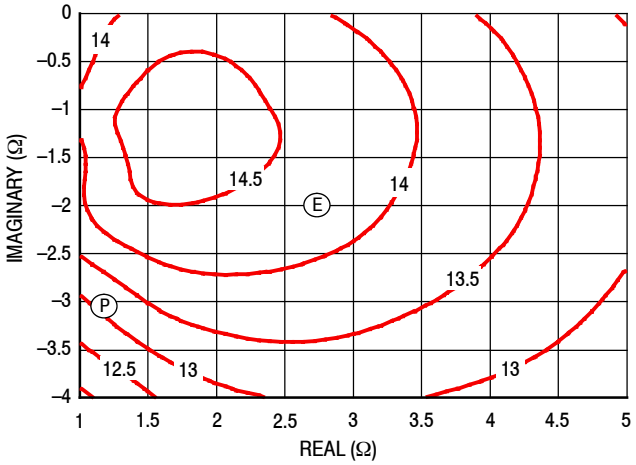


Figure 22. P3dB Load Pull Gain Contours (dB)

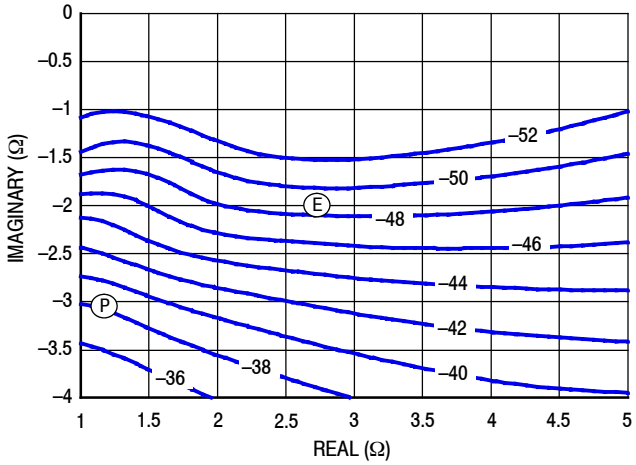
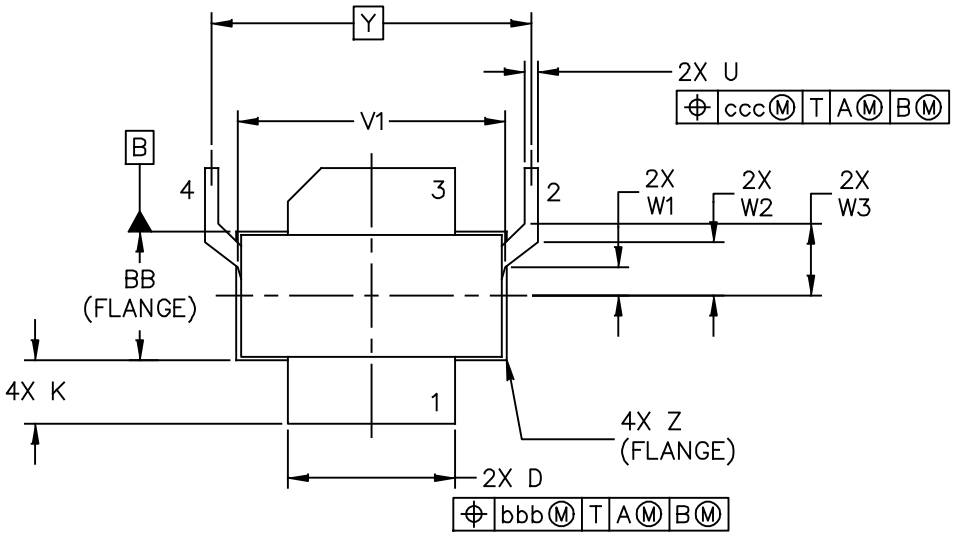


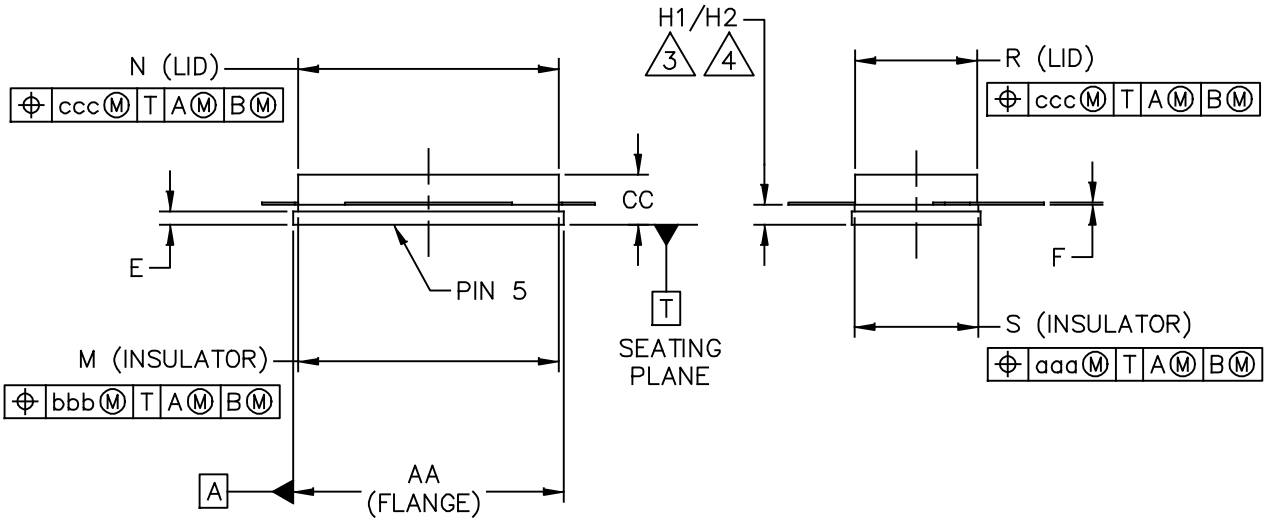
Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS





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NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1 & 3. H2 APPLIES TO PINS 2 & 4.
4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
D	.495	.505	12.57	12.83	V1	.795	.805	20.19	20.45
E	.035	.045	0.89	1.14	W1	.080	.090	2.03	2.29
F	.004	.007	0.10	0.18	W2	.155	.165	3.94	4.19
H1	.057	.067	1.45	1.70	W3	.210	.220	5.33	5.59
H2	.054	.070	1.37	1.78	Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
M	.774	.786	19.66	19.96	aaa	–	.005	–	0.13
N	.772	.788	19.61	20.02	bbb	–	.010	–	0.25
					ccc	–	.015	–	0.38

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.freescale.com/rf
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2015	• Initial Release of Data Sheet

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