SY69753L

3.3V, 125Mbps, 155Mbps Clock and Data Recovery

Use lower-power SY69753AL for new designs

General Description

The SY69753L is a complete Clock Recovery and Data Retiming integrated circuit for OC-3/STS-3 applications at 155Mbps NRZ. The device is ideally suited for SONET/SDH/ATM applications and other high-speed data transmission systems.

Clock recovery and data retiming is performed by synchronizing the on-chip VCO directly to the incoming data stream. The VCO center frequency is controlled by the reference clock frequency and the selected divide ratio. On-chip clock generation is performed through the use of a frequency multiplier PLL with a byte rate source as reference.

The SY69753L also includes a link fault detection circuit.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- 3.3V power supply
- SONET/SDH/ATM compatible
- Clock and data recovery for 125Mbps/155Mbps NRZ data stream
- Two on-chip PLLs: one for clock generation and another for clock recovery
- Selectable reference frequencies
- Differential PECL high-speed serial I/O
- Line receiver input: no external buffering needed
- Link fault indication
- 100k ECL compatible I/O
- Industrial temperature range (–40°C to +85°C)
- Complies with Bellcore, ITU/CCITT and ANSI specifications for OC-3 applications
- Available in 32-pin EPAD-TQFP

Applications

- Ethernet media converter(m)
- SONET/SDH/ATM OC-3
- Proprietary architecture at 135Mbps to 180Mbps

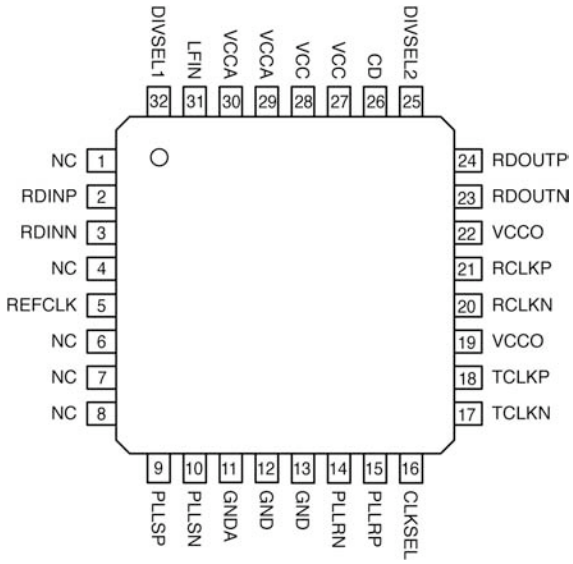
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY69753LHI	H32-1	Industrial	SY69753LHI	Sn-Pb
SY69753LHITR[2]	H32-1	Industrial	SY69753LHI	Sn-Pb
SY69753LHG[3]	H32-1	Industrial	SY69753LHG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY69753LHGTR[2, 3]	H32-1	Industrial	SY69753LHG with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Recommended for new designs.

Pin Configuration



32-Pin EPAD-TQFP (H32-1)

Pin Description

Inputs

Pin Number	Pin Name	Type	Pin Name
2 3	RDINP RDINN	Differential PECL	Serial Data Input: These built-in line receiver inputs are connected to the differential receive serial data stream. An internal receive PLL recovers the embedded clock (RCLK) and data (RDOUT) information.
5	REFCLK	TTL Input	Reference Clock: This input is used as the reference for the internal frequency synthesizer and the "training" frequency for the receiver PLL to keep it centered in the absence of data coming in on the RDIN inputs.
26	CD	PECL Input	Carrier Detect: This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output of optical modules or from external transition detection circuitry. When this input is HIGH, the input data stream (RDIN) is recovered normally by the Receive PLL. When this input is LOW the data on the inputs RDIN will be internally forced to a constant LOW, the data outputs RDOUT will remain LOW, the Link Fault Indicator output LFIN forced LOW and the clock recovery PLL forced to look onto the clock frequency generated from REFCLK.
32 25	DIVSEL1 DIVSEL2	TTL Input	Divider Select: These inputs select the ratio between the output clock frequency (RCLK/TCLK) and the REFCLK input frequency as shown in the “Reference Frequency Selection” table.
16	CLKSEL	TTL Input	Clock Select: This input is used to select either the recovered clock of the receiver PLL (CLKSEL = HIGH) or the clock of the frequency synthesizer (CLKSEL = LOW) to the TCLK outputs.

Outputs

Pin Number	Pin Name	Type	Pin Name
31	LFIN	TTL Output	Link Fault Indicator: This output indicates the status of the input data stream RDIN. Active HIGH signal is indicating when the internal clock recovery PLL has locked onto the incoming data stream. LFIN will go HIGH if CD is HIGH and RDIN is within the frequency range of the Receive PLL (1000ppm) and will be alternating if not. LFIN is an asynchronous output.
23 24	RDOUTN RDOUTP	Differential PECL	Receive Data Output: These ECL 100K outputs represent the recovered data from the input data stream (RDIN). This recovered data is specified against the rising edge of RCLK.
20 21	RCLKN RCLKP	Differential PECL	Clock Output: These ECL 100K outputs represent the recovered clock used to sample the recovered data (RDOUT).
18 17	TCLKP TCLKN	Differential PECL	Clock Output: These ECL 100K outputs represent either the recovered clock (CLKSEL = HIGH) used to sample the recovered data (RDOUT) or the transmit clock of the frequency synthesizer (CLKSEL = LOW).
9 10	PLLSP PLLSN		Clock Synthesis PLL Loop Filter: External loop filter pins for the clock synthesis PLL.
14 15	PLLRN PLLRP		Clock Recovery PLL Loop Filter: External loop filter pins for the receiver PLL.

Power and Ground

Pin Number	Pin Name	Type	Pin Name
27, 28	VCC		Power Supply.(1)
29, 30	VCCA		Analog Power Supply Voltage.(1)
19, 22	VCCO		Output Supply Voltage.(1)
12, 13	GND		Ground.
1, 4, 6, 7, 8	NC		No connect.
11	GNDA		Analog Ground.

Note:

1. VCC, VCCA, VCCO must be the same value.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... -0.5V to +5.0V
Input Voltage (V_{IN}) ..... -0.5V to V_{CC}
Output Current (I_{OUT})
  Continuous ..... ±50mA
  Surge ..... ±100mA
Lead Temperature (soldering, 20sec.) ..... +260°C
Storage Temperature (T_s) ..... -65°C to +150°C

Operating Ratings[2]

Input Voltage (V_{CC}) ..... +3.15V to +3.45V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... +125°C
Package Thermal Resistance[3]
  EPAD-TQFP (θ_{JA})
    Still-air ..... 28°C/W
    500lfpm ..... 20°C/W
  EPAD-TQFP (θ_{JC}) ..... 4°C/W

DC Electrical Characteristics

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.15	3.3	3.45	V
I_{CC}	Power Supply Current			170	230	mA

PECL 100K DC Electrical Characteristics

V_{CC} = V_{CCO} = V_{CCA} = 3.3V ±5%; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		V_{CC}-1.165		V_{CC}-0.880	V
V_{IL}	Input LOW Voltage		V_{CC}-1.810		V_{CC}-1.475	V
V_{OH}	Output HIGH Voltage	50Ω to V_{CC}-2V	V_{CC}-1.075		V_{CC}-0.830	V
V_{OL}	Output LOW Voltage	50Ω to V_{CC}-2V	V_{CC}-1.860		V_{CC}-1.570	V
I_{IL}	Input LOW Current	V_{IN} = V_{IL} (Min)	0.5			µA

TTL DC Electrical Characteristics

V_{CC} = V_{CCO} = V_{CCA} = 3.3V ±5%; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = -0.4mA	2.0			V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA			0.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7V, V_{CC} = Max. V_{IN} = V_{CC}, V_{CC} = Max.	-125		 +100	µA µA
I_{IL}	Input LOW Voltage	V_{IN} = 0.5V, V_{CC} = Max.	-300			µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, (max., 1 sec.)	-15		-100	mA

Notes:

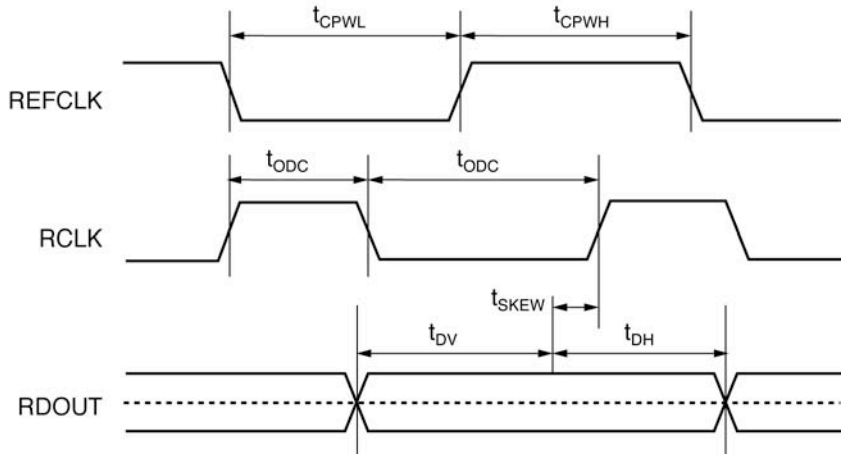
1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Numbers valid with proper thermal design of PCB and exposed pad soldered to island on PCB. Refer to Figure on page 13.

AC Electrical Characteristics

V_{CC} = V_{CCO} = V_{CCA} = 3.3V ±5%; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{VCO}	VCO Center Frequency	f_{REFCLK} x Byte Rate	800		1250	MHz
Δf_{VCO}	VCO Center Frequency Tolerance	Nominal		5		%
t_{ACQ}	Acquisition Lock Time	50Ω to V_{CC}-2V			15	µs
t_{CPWH}	REFCLK Pulse Width HIGH	50Ω to V_{CC}-2V	4			ns
t_{CPWL}	REFCLK Pulse Width LOW	V_{IN} = V_{IL} (Min)	4			ns
t_{DV}	Data Valid		1/(2xf_{RCLK}) -200			ps
t_{DH}	Data Hold		1/(2xf_{RCLK}) -200			ps
t_{ir}	REFCLK Input Rise Time			0.5	2	ns
t_{ODC}	Output Duty Cycle (RCLK/TCLK)		45		55	% of UI
t_{RSKEW}	Recovered Clock Skew		-200		+200	ps
t_r, t_f	ECL Output Rise/Fall Time (20% to 80%)	50Ω to V_{CC}-2	100		400	ps

Timing Waveforms



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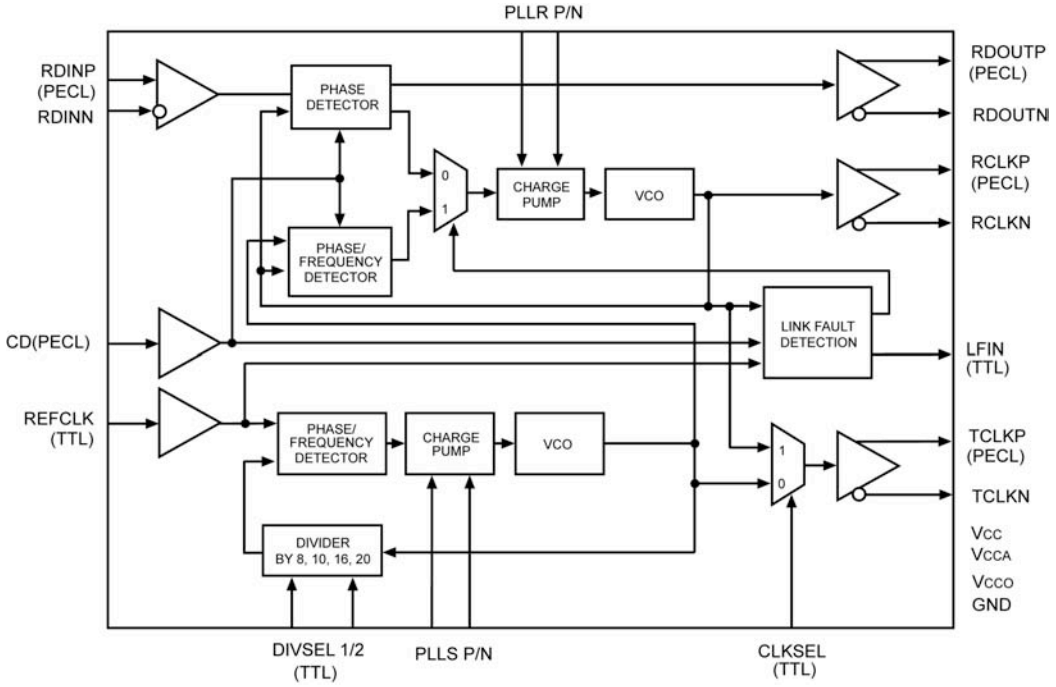
Functional Block



Functional Description

Clock Recovery

Clock Recovery, as shown in the block diagram, generates a clock that is at the same frequency as the incoming data bit rate at the Serial Data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency detector. Output pulses from the detector indicate the required direction of phase correction. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability, without incoming data, is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the Frequency of the incoming signal varies by greater than approximately 1000ppm with respect to the synthesizer frequency, the PLL will be declared out of lock, and the PLL will lock to the reference clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a 30µs data stream of continuous 1's or 0's for random incoming NRZ data.

The total loop dynamic of the clock recovery PLL provides jitter tolerance which is better than the specified tolerance in GR-253-CORE.

Lock Detect

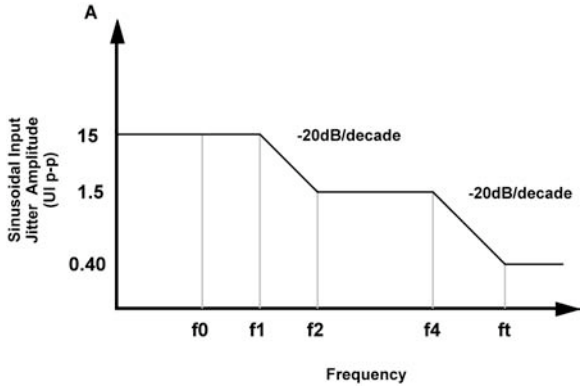
The SY69753L contains a link fault indication circuit, which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, then the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than approximately 1000ppm, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within approximately 1000ppm, the PLL will be declared in lock and the lock detect output will go active.

Performance

The SY69753L PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used with differential inputs and outputs.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1dB optical/electrical power penalty. SONET input jitter tolerance requirement condition is the input jitter amplitude that causes an equivalent of 1dB power penalty.



OC/STS-N Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (Hz)	ft (Hz)
3	10	30	300	6.5	65

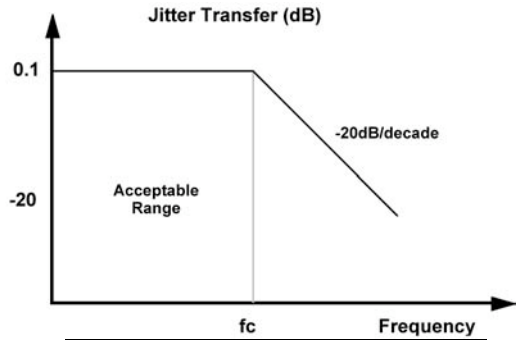
Figure 1. Input Jitter Tolerance

Jitter Transfer

Jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 2.

Jitter Generation

The jitter of the serial clock and serial data outputs shall not exceed .01 U.I. rms when a serial data input with no jitter is presented to the serial data inputs.



OC/STS-N Level	fc (kHz)	P (dB)
3	130	0.1

Figure 2. Jitter Transfer

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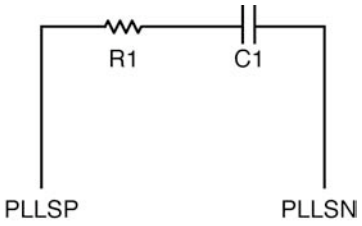
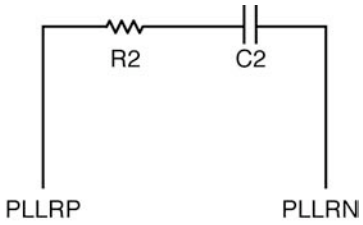
Loop Filter Components[1]



R1 = 350Ω
C1 = 1.5µF (X7R Dielectric)



R2 = 680Ω
C2 = 1.0µF (X7R Dielectric)

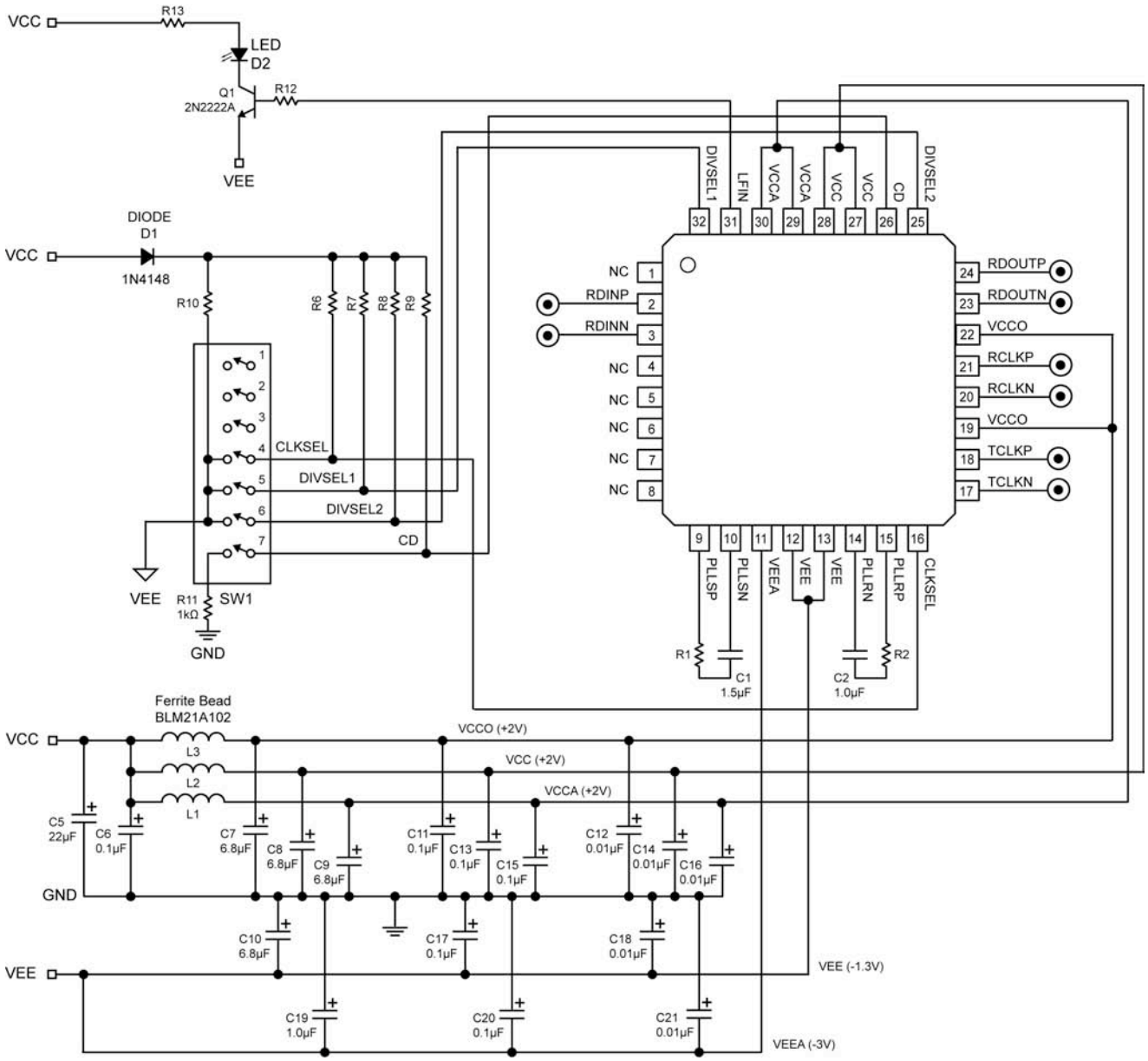
Note:

1. Suggested values. Values may vary for different applications.

Reference Frequency Selection

DIVSEL1	DIVSEL2	f_{RCLK}/f_{REFCLK}
0	0	8
0	1	10
1	0	16
1	1	20

Application Example



Note:

C3, C4 are optional.

C1 = 1.5µF
C2 = 1.0µF
R1 = 350Ω
R2 = 680Ω
R3 through R10 = 5kΩ
R12 = 12kΩ
R13 = 130Ω

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	ECU-V1H104KBW	Panasonic[1]	1.5µF Ceramic Capacitor, Size 1206, X7R Dielectric, Loop Filter, Critical	1
C2	ECU-V1H104KBW	Panasonic[1]	1.0µF Ceramic Capacitor, Size 1206, X7R Dielectric, Loop Filter, Critical	1
C3, C4	ECU-V1H104KBW	Panasonic[1]	0.47µF Ceramic Capacitor, Size 1206, X7R Dielectric, Loop Filter, Optional	2
C5	ECS-T1ED226R	Panasonic[1]	22µF Tantalum Electrolytic Capacitor, Size D	1
C6	ECU-V1H104KBW	Panasonic[1]	0.1µF Ceramic Capacitor, Size 1206, X7R Dielectric Power Supply Decoupling	1
C7, C8, C9, C10	ECS-T1EC685R	Panasonic[1]	6.8µF Tantalum Electrolytic Capacitor, Size C	4
C19	ECJ-3YB1E105K	Panasonic[1]	0.1µF Ceramic Capacitor, Size 1206, X7R Dielectric VEEA Decoupling	1
C11, C13	ECU-V1H104KBW	Panasonic[1]	0.1µF Ceramic Capacitor, Size 1206, X7R Dielectric VCCO/VCC Decoupling	1
C15, C17	ECU-V1H104KBW	Panasonic[1]	0.1µF Ceramic Capacitor, Size 1206, X7R Dielectric VCCA/VEEA Decoupling	1
C20	ECU-V1H104KBW	Panasonic[1]	0.1µF Ceramic Capacitor, Size 1206, X7R Dielectric VEEA Decoupling	1
C12, C14	ECU-V1H103KBW	Panasonic[1]	0.01µF Ceramic Capacitor, Size 1206, X7R Dielectric VCCO/VCC Decoupling	1
C16, C18	ECU-V1H103KBW	Panasonic[1]	0.01µF Ceramic Capacitor, Size 1206, X7R Dielectric VCCA/VEEA Decoupling	1
C21	ECU-V1H103KBW	Panasonic[1]	0.01µF Ceramic Capacitor, Size 1206, X7R Dielectric VEEA Decoupling	1
D1	1N4148		Diode	1
D2	P300-ND/P301-ND	Panasonic[1]	T-1 3/4, Red LED	1
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12	142-0701-851	Johnson Components[2]	Gold Plated, Jack, SMA, PCB Mount	12
L1, L2, L3	BLM21A102F	Murata[3]	Ferrite Beads, Power Noise Suppression	3
Q1	NTE123A	NTE[4]	2N2222A Buffer/Driver Transistor, NPN	1
R1			350Ω Resistor, 2%, Size 1206, Loop Filter Component, Critical	1
R2			680Ω Resistor, 2%, Size 1206, Loop Filter Component, Critical	1
R3, R4, R5, R6, R7, R8, R9, R10			5kΩ Pull-up Resistor, 2%, Size 1206	8
R11			1kΩ Pull-down Resistor, 2%, Size 1206	1
R12			12kΩ Resistor, 2%, Size 1206	1
R13			130Ω Pull-up Resistor, 2%, Size 1206	1
SW1	206-7	CTS[5]	SPST, Gold Finish, Sealed Dip Switch	1

Notes:

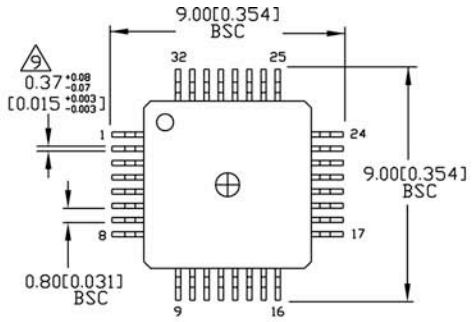
1. Panasonic: www.panasonic.com.
2. Johnson Components: www.johnson-components.com.
3. Murata: www.murata.com.
4. NTE: www.nte.com.
5. CTS: www.cts.com.

Appendix A

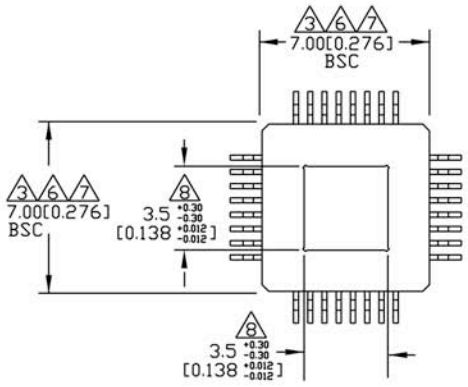
Layout and General Suggestions

1. Establish controlled impedance stripline, microstrip, or coplanar construction techniques.
2. Signal paths should have approximately the same width as the device pads.
3. All differential paths are critical timing paths, where skew should be matched to within ±10ps.
4. Signal trace impedance should not vary more than ±5%. If in doubt, perform TDR analysis of all high-speed signal traces.
5. Maintain compact filter networks as close to filter pins as possible. Provide ground plane relief under filter path to reduce stray capacitance. Be careful of crosstalk coupling into the filter network.
6. Maintain low jitter on the REFCLK input. Isolate the XTAL oscillator from power supply noise by adequately decoupling. Keep XTAL oscillator close to device, and minimize capacitive coupling from adjacent signals.
7. Higher speed operation may require use of fundamental-tone (third-overtone typically has more jitter) crystal-based oscillator for optimum performance. Evaluate and compare candidates by measuring TXCLK jitter.
8. All unused outputs require termination. To conserve power, unused PECL outputs can be terminated with a 1kΩ resistor to VEE.

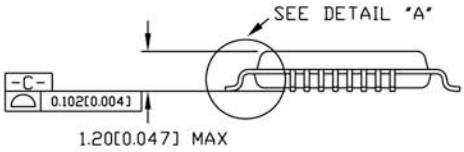
Package Information



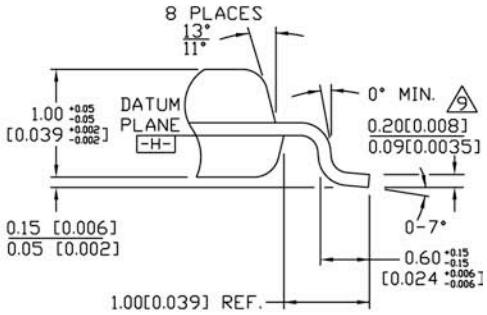
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. EXPOSED PAD SHALL BE COPLANAR WITH PACKAGE BOTTOM WITHIN 0.05mm
EXPOSED PAD: Cu WITH Sn/Pb PLATING
9. DIMENSION INCLUDES LEAD FINISH.

32-Pin EPAD-TQFP (H32-1)

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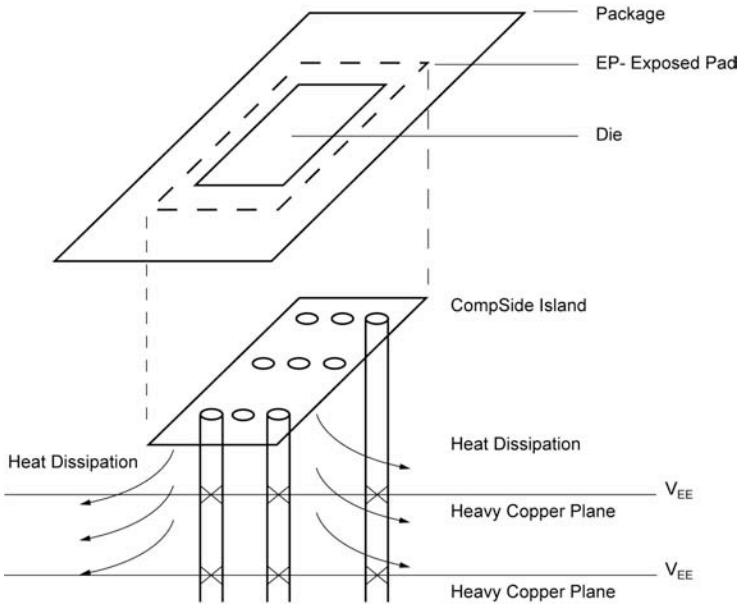

PCB Thermal Consideration for 32-Pin EPAD-TQFP Package

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