NB3N65027

3.3V Programmable 3-PLL Clock Synthesizer with 6 LVTTL/LVCMOS Outputs w/OE

The NB3N65027 is a LVCMOS PLL−synthesized clock generator. It accepts a 10 MHz to 27 MHz clock or fundamental mode crystal as the reference source and drives three independent, low noise phase−locked loops (PLLs).

Control lines ACSx, BCSx and CCS will select their appropriate bank output frequencies. ACS1 and BCS1 are two−level LVTTL/LVCMOS inputs, High and Low. ACS0, BCS0 and CCS are three−level LVCMOS inputs, High, Mid and Low.

The NB3N65027 has three independent LVTTL/LVCMOS output banks of two outputs each. Banks A and B offer a 1X and a 1/2X output. Using a 25 MHz crystal, the selectable output frequencies range from 16 2/3 MHz to 133 1/3 MHz. A 12.5 MHz crystal offers from 8 1/3 MHz to 66 2/3 MHz. In addition, the NB3N65027 will generate a buffered reference LVTTL/LVCMOS output, REFOUT, 10 MHz to 27 MHz. See Tables 2 through 9 for the variety of available output frequencies. The OE pin, when set LOW, will disable the output drivers to high impedance.

The NB3N65027 operates from a single +3.3 V supply across the operating temperature range from −40°C to +85°C, and is offered in a QSOP−20 RoHS compliant package.

The NB3N65027 provides the optimum combination of low cost, flexibility, and high performance for Network, PCI and SDRAM applications.

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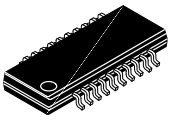


QSOP20
CASE 492AC

MARKING DIAGRAM

3N65027	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

Features

- 12.5 MHz or 25 MHz Fundamental Crystal or Clock Input
- Six Output Clocks with Selectable Frequencies
- Buffered Crystal Reference Output
- SDRAM Frequencies of 67, 83, 100, and 133 MHz
- LVCMOS with 25 mA Output Drive Capability at TTL Levels
- Operating Range: V_{CC} = 3.3 V ±10%
- QSOP−20 Package, 150 mil
- −40°C to +85°C Ambient Operating Temperature
- These Devices are Pb−Free and are RoHS Compliant

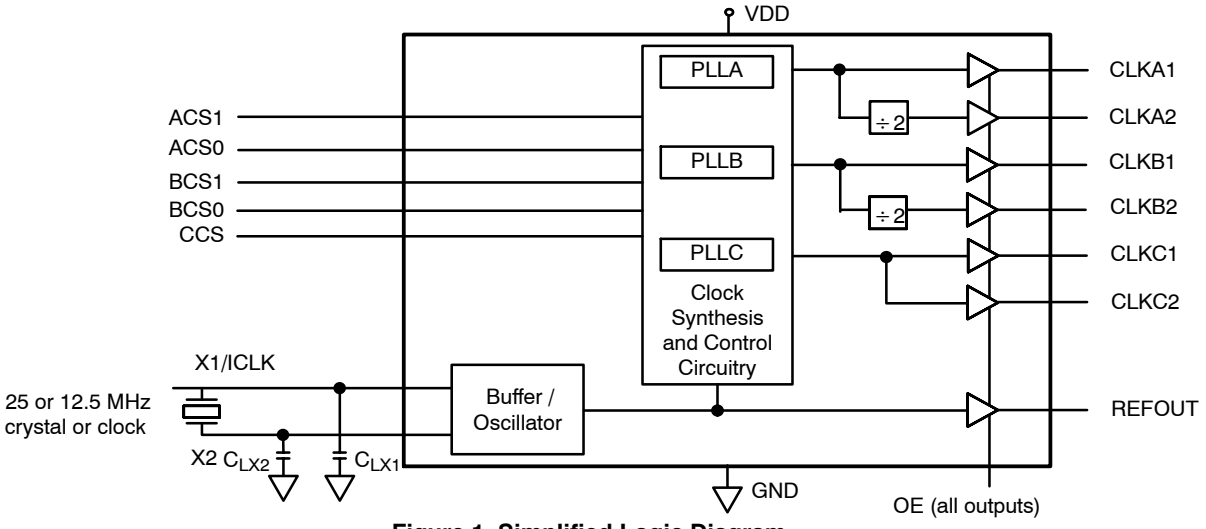


Figure 1. Simplified Logic Diagram

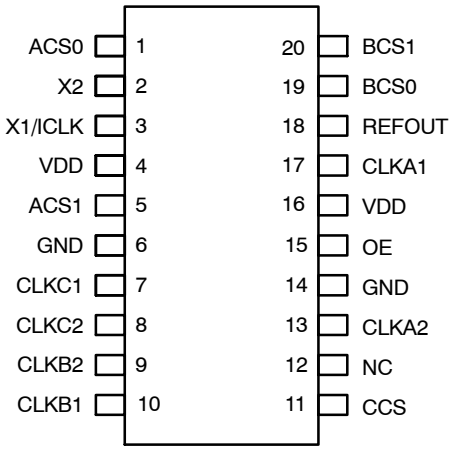


Figure 2. Pinout: QSOP−20 (Top View)

Table 1. PIN DESCRIPTION (Note 1)

Pin Number	Pin Name	Pin Type	Pin Description
1	ACS0	Tri−Level Input	A Clock Select 0. Selects outputs on CLKA1 and CLKA2 per table on page 3.
2	X2	Input	Crystal connection. Connect to a fundamental crystal or leave unconnected for a clock input.
3	X1/ICLK	Input	Crystal or Clock input connection. If a clock input is used, drive it into X1 and leave X2 unconnected.
4	VDD	Power	Connect to +3.3 V. Must be the same as pin 16.
5	ACS1	Two−Level Input	A Clock Select 1. Selects outputs on CLKA1 and CLKA2 per table on page 3. Internal pull−up.
6	GND	Power	Connect to ground.
7	CLKC1	Output	Output Clock C1. Depends on setting of CCS per table on page 3.
8	CLKC2	Output	Output Clock C2. Depends on setting of CCS per table on page 3. Same as CLKC1.
9	CLKB2	Output	Output Clock B2. Depends on setting of BCS1, 0 per table on page 3.
10	CLKB1	Output	Output Clock B1. Depends on setting of BCS1, 0 per table on page 3.
11	CCS	Tri−Level Input	Clock C select pin. Selects outputs on CLKC1 and CLKC2 per table on page 3.
12	NC	−	No Connect
13	CLKA2	Output	Output Clock A2. Depends on setting of ACS1, 0 per table on page 3.
14	GND	Power	Connect to ground.
15	OE	Input	Output enable. Tri−states all outputs when low. Internal pull−up.
16	VDD	Power	Connect to +3.3 V. Must be the same as pin 4.
17	CLKA1	Output	Output Clock A1. Depends on setting of ACS1, 0 per table on page 3.
18	REFOUT	Output	Buffered reference clock output. Same frequency as crystal or clock input.
19	BCS0	Tri−Level Input	B Clock Select 0. Selects outputs on CLKB1 and CLKB2 per table on page 3.
20	BCS1	Two−Level Input	B Clock Select 1. Selects outputs on CLKB1 and CLKB2 per table on page 3. Internal pull−up.

1. All VDD and GND pins must be externally connected to a power supply for proper operation.

FOR A 25 MHz FUNDAMENTAL CRYSTAL OR CLOCK INPUT, THE FOLLOWING FOUR TABLES APPLY:

Table 2. A CLOCKS SELECT TABLE (outputs in MHz)

ACS1	ACS0	CLKA1	CLKA2
0	0	100	off (low)
0	M	Test	Test
0	1	75	off (low)
1	0	33.3333	16.6667
1	M	Test	Test
1	1	66.6667	33.3333

Table 3. B CLOCKS SELECT TABLE (outputs in MHz)

BCS1	BCS0	CLKB1	CLKB2
0	0	Test	Test
0	M	66.6667	33.3333
0	1	100	50
1	0	83.3333	41.6667
1	M	Test	Test
1	1	133.3333	66.6667

Table 4. C Clocks Select Table (outputs in MHz)

CCS	CLKC1	CLKC2
0	125	125
M	Test	Test
1	75	75

Table 5. REFERENCE OUTPUT CLOCK FREQUENCY (in MHz)

REFOUT
25

FOR A 12.5 MHz FUNDAMENTAL CRYSTAL OR CLOCK INPUT, THE FOLLOWING FOUR TABLES APPLY:

Table 6. A CLOCKS SELECT TABLE (outputs in MHz)

ACS1	ACS0	CLKA1	CLKA2
0	0	50	off (low)
0	M	Test	Test
0	1	37.5	off (low)
1	0	16.6667	8.3333
1	M	Test	Test
1	1	33.3333	16.6667

Table 7. B CLOCKS SELECT TABLE (outputs in MHz)

BCS1	BCS0	CLKB1	CLKB2
0	0	Test	Test
0	M	33.3333	16.6667
0	1	50	25
1	0	41.6667	20.8333
1	M	Test	Test
1	1	66.6667	33.3333

Table 8. C CLOCKS SELECT TABLE (outputs in MHz)

CCS	CLKC1	CLKC2
0	62.5	62.5
M	Test	Test
1	37.5	37.5

Table 9. REFERENCE OUTPUT CLOCK FREQUENCY (in MHz)

REFOUT
12.5

0 = connect directly to GND
M = leave unconnected (automatically self biases to $V_{DD}/2$)
1 = connect directly to V_{DD}

Table 10. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
R_{PU} – Internal Input Pull−up Resistor	BCS1, OE ACS1	430 kΩ 120 kΩ
Z_{OUT} – Nominal Output Impedance		20 Ω
Moisture Sensitivity (Note 2)	QSOP−20	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		16700
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 11. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Rating	Unit
V_{DD}	Positive Power Supply	GND = 0 V	4.5	V
V_{IO}	All Inputs and Outputs	GND = 0 V	−0.5 to V_{DD} +0.5	V
T_A	Operating Temperature Range		−40 to +85	°C
T_{stg}	Storage Temperature Range		−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 1 m/s air flow 3 m/s air flow	135 typ 93 typ 78 typ	°C/W °C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case) (Note 3)		60 typ	°C/W
T_{sol}	Wave Solder Tempearture − Pb−Free	≤ 20 sec	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 12. DC CHARACTERISTICS V_{DD} = 3.3V ±10%, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY					
V_{DD}	Power Supply Voltage; GND = 0 V	3.0	3.3	3.6	V
I_{DD}	Power Supply Current for V_{DD} (Inputs and Outputs Open)		40	60	mA
OUTPUTS					
V_{OH}	Output HIGH Voltage; V_{DD} = 3.3V I_{OH} = −25 mA I_{OH} = −8mA	2.4 V_{DD} − 0.4			V
V_{OL}	Output LOW Voltage; I_{OL} = 25 mA			0.8	V
I_{OS}	Output Short Circuit Current, Each Output		±50		mA
X1/CLK INPUT PIN, ONLY					
V_{IH}	Input HIGH Voltage	V_{DD} / 2 + 1			V
V_{IL}	Input LOW Voltage			V_{DD} / 2 − 1	V
TRI−LEVEL TYPE INPUTS: ACS0, BCS0, CCS					
V_{IH}	Input HIGH Voltage	V_{DD} − 0.5			V
V_{IL}	Input LOW Voltage			0.5	V
TWO−LEVEL TYPE INPUTS: ACS1, BCS1, OE					
V_{IH}	Input HIGH Voltage	2.0			V
V_{IL}	Input LOW Voltage			0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 13. AC CHARACTERISTICS V_{DD} = 3.3V ±10%, GND = 0 V, TA = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
f_{IN}	Input Frequency, Crystal or Clock	10	12.5 or 25	27	MHz
t_{DC}	Output Clock Duty Cycle at V_{DD}/2, 15 pF Load	40	50	60	%
	Frequency Error, all clocks, 15 pF Load			0	ppm
t_{or}, t_{of}	Output Rise/Fall Times; 0.8 V to 2.0 V, 15 pF Load			1.5	ns
	Absolute Jitter, short−term; variation from mean, 15 pF Load		±120		ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

External Components

The NB3N65027 requires a minimum number of external components for proper operation.

Decoupling Capacitor

Decoupling capacitors of 0.01 μF must be connected between each V_{DD} and GND (pins 4 and 6, pins 16 and 14), as close to the device as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50 Ω trace (a commonly used trace impedance), place a 33 Ω resistor in series with the clock line as close to the clock output pin as possible. The nominal impedance of the clock output is 20 Ω.

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal load capacitors should be connected from pins X1 to ground and X2 to ground to optimize the frequency accuracy, See Figure 1.

A crystal in parallel resonance will require the spec $\mathbf{C_L}$ as a balanced loading for each side of the crystal, so $\mathbf{C_L}$ is distributed in two equal series load caps, $\mathbf{C_{L1}}$ and $\mathbf{C_{L2}}$. All stray and additional capacitance must be subtracted from this total loading.

1. Crystal load capacitance, CL, is:

$$CL = \left(\frac{C_{L1} \cdot C_{L2}}{C_{L1} + C_{L2}}\right)$$

Where:

C_L = Crystal Spec Load Capacitance

C_{L1} = X1 Pin Total Load Capacitance

C_{L2} = X2 Pin Total Load Capacitance

2. If CL = 18 pF, then $C_{L1} = C_{L2} = 2CL$, or 36 pF.

Stray capacitance, C_{LS1} and C_{LS2}, must be considered and subtracted from each total load capacitance, C_{L1} and C_{L2}.

Furthermore:

$C_{L1} = C_{LX1} + C_{LS1}$

$C_{L2} = C_{LX2} + C_{LS2}$

Where:

C_{LX1} = Load Capacitor Board Component for C_{L1}

C_{LX2} = Load Capacitor Board Component for C_{L2}

C_{LS1} = Stray Load Capacitance at X1

C_{LS2} = Stray Load Capacitance at X2

As an example, for 4 pF of stray capacitance, $C_{LS1} = C_{LS2}$ = 4 pF, then, Board Component Capacitors $C_{LX1} = C_{LX2} = 2CL - C_{LS(1or2)}$, or 36 pF – 4 pF = 32 pF.

Table 14. RECOMMENDED CRYSTAL PARAMETERS

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance
Load Capacitance	18 pF
Operating Range	–40 to +85°C
Shunt Capacitance	5 pF Max
Equivalent Series Resistance (ESR)	50 Ω Max
Correlation Drive Level	1.0 mW Max

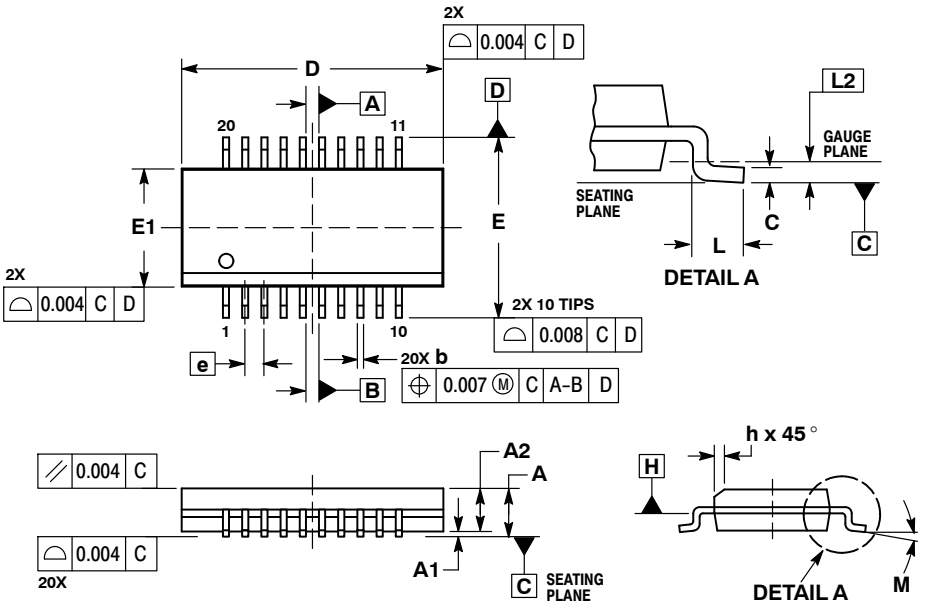
ORDERING INFORMATION

Device	Package	Shipping†
NB3N65027DTG	QSOP20 (Pb–Free)	55 Units / Rail
NB3N65027DTR2G	QSOP20 (Pb–Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

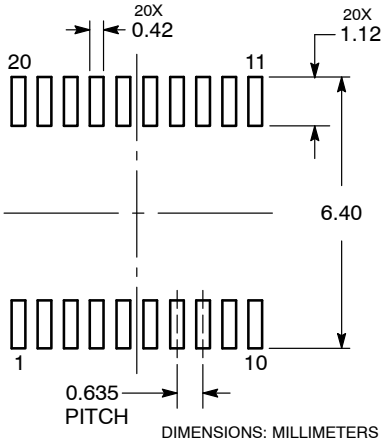
QSOP20
CASE 492AC−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.005 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.069	----	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	----	1.24	----
b	0.008	0.012	0.20	0.30
c	0.004	0.010	0.10	0.25
D	0.341 BSC		8.66 BSC	
E	0.236 BSC		5.99 BSC	
E1	0.154 BSC		3.91 BSC	
e	0.025 BSC		0.635 BSC	
h	0.010	0.020	0.25	0.51
L	0.016	0.050	0.41	1.27
L2	0.010 BSC		0.25 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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