

## Description

The ISL54406EVAL1Z evaluation board is designed to provide a quick and easy method for evaluating the ISL54406 Click and Pop Eliminator IC.

The ISL54406 device is a unique IC. To use this evaluation board properly requires a thorough knowledge of the operation of the IC. Refer to the data sheet (FN6578) for an understanding of the functions and features of the device. Studying the device's truth table along with its pinout diagram on page 2 of the data sheet is the best way to get a quick understanding of how the part works.

A picture of the evaluation board is shown in Figure 1. The ISL54406  $\mu$ TQFN IC is set in a socket on the evaluation board. It is located in the center of the board and is designated as U1.

The ISL54406 IC is a dual SPST analog switch that has four modes of operation: Audio, Mute, Click and Pop, and Shutdown (SHDN) mode. The evaluation board contains standard RCA/BNC connectors and a single headphone jack to allow the user to easily interface with the IC to evaluate its functions, features, and performance in the four modes of operation. The evaluation board has selectable output loads of 20k $\Omega$  and 32 $\Omega$  resistors to simulate an audio amplifier pre-amp or stereo headphones. The board also has DC blocking capacitors at the switch input to remove the DC bias of single supply amplifiers.

This application note will guide the user through the process of configuring and using the evaluation board to evaluate the ISL54406 device for Click and Pop elimination and Audio Muting applications.

## Features

- Selectable Output Resistive Loads and Input DC Blocking Capacitors
- RCA Audio Input/Output Jacks, Stereo Headphone Output Jack and BNC Connectors
- Convenient Test Points and Connections for Test Equipment
- Click and Pop Elimination Circuitry
- High Off-Isolation Audio Muting

## Picture of Evaluation Board (Top View)



FIGURE 1. ISL54406EVAL1Z EVALUATION BOARD

## Board Architecture/Layout

### Basic Layout of Evaluation Board

Refer to Figure 1 and the Board Schematic at the end of this manual. The basic layout of the main board is as follows:

Power (J1), Ground (J2), logic SEL1 (J9/J10) and logic SEL2 (J3/J4) connections are located at the top of the board. Audio Input BNC/RCA connectors are at the right side of the board for LIN input (J11/J12) and RIN input (J13/J14).

Note: The audio inputs have a 200 $\mu$ F series DC blocking capacitance that can be used for AC-coupling audio signals that are DC biased in single supply systems. If the audio source is not DC biased, it is recommended to bypass the capacitors (C3 to C6) by placing a jumper on JP6 for LIN and JP7 for RIN. Note that if the audio source already has a DC blocking capacitor, it is recommended to bypass the capacitor on the evaluation board, otherwise this will increase insertion loss. The capacitance can be reduced to 100 $\mu$ F by depopulating the 0 $\Omega$  resistor on R<sub>6</sub> and R<sub>7</sub>.

Audio output RCA/BNC connectors are on the left side of the board labeled LOU output (J5/J6) and ROU output (J7/J8). In addition, the left and right outputs are also connected to the stereo headphone jack HJ1. Selectable load resistances are available on the evaluation board. When jumpers JP2 and JP3 are in the 1-2 pin position, the load is 20k $\Omega$  and in the 2-3 position the load is 32 $\Omega$ . The load can be bypassed by removing the jumpers altogether.

Located in the center of the board is the ISL54406 IC (U1). The socket for the IC has a pin 1 dot to show how the IC should be oriented on the socket. The IC pin 1 indicator dot needs to be aligned with the socket pin 1 indicator dot that is visible when the socket is unlatched.

### Power Supply

The DC power supply connected at banana jacks J1 (V+) and J2 (GND) provides power to the evaluation board. The IC requires a +2.7V to +5.0V DC power supply for proper operation, although the recommended range is +2.7V to +3.6V. The power supply should be capable of delivering 100 $\mu$ A of current.

### Logic Control

The state of the ISL54406 device is determined by the voltage at the SEL1 (J9/J10) and the SEL2 (J3/J4) inputs. Normally, jumpers JP1 and JP5 should be in the 1-2 pin position. If the user desires to control the logic state of SEL1 and SEL2 via switches S1 and S2 on the board, place jumpers JP1 and JP5 in the 2-3 pin position. In the switch-up position, SEL1 and SEL2 will be tied to V+ (Logic "1"). In the down position, a 4M $\Omega$  resistor internal to the IC will pull SEL1 and SEL2 to GND (Logic "0")

These control pins are 1.8V logic compatible which allows for control via a standard  $\mu$ controller.

Logic "0" (LOW) when  $\leq 0.5V$  (or floating)

Logic "1" (HIGH) when  $\geq 1.4V$

### Logic States

The ISL54406 has four modes of operation that are determined by the SEL1 and SEL2 logic states: Audio Playback Mode, Click and Pop Mode, Audio Mute Mode, and Shutdown (SHDN) Mode.

#### AUDIO PLAYBACK MODE (SEL1 = SEL2 = 1)

If the SEL1 and SEL2 pins are Logic "1", the part will be in the Audio Playback mode. In Audio Playback mode the LIN and RIN pins are connected to the LOUT and ROUT pins, respectively, through a 2.5 $\Omega$  switch path. The Audio Inputs have a selectable 100 $\mu$ F or 200 $\mu$ F series DC blocking capacitor or can be bypassed altogether. The Audio Outputs can be loaded on the evaluation board with a 32 $\Omega$  or a 20k $\Omega$  resistor or can be bypassed altogether.

#### CLICK AND POP MODE (SEL1 = 1; SEL2 = 0)

If SEL1 is Logic "1" and SEL2 is Logic "0", the part will go into Click and Pop Mode. This mode is optimal when powering up or down the DC biased source inputs or muting the signal to the load. In Click and Pop Mode, the 2.5 $\Omega$  audio switches are OFF (high impedance). The Audio Output connections are shunted to ground through 6 $\Omega$  resistors that are internal to the IC and the Audio Input connections are shunted to ground through 40 $\Omega$  resistors that are internal to the IC (Click and Pop circuitry is active).

Before powering down or powering up of a DC biased source input, the ISL54406 should be put in the Click and Pop Mode. In Click and Pop Mode, transients generated at the Audio Input connections due to a DC step voltage at the audio source drivers will not pass to the load, thus eliminating Click and Pop noise.

#### AUDIO MUTE MODE (SEL1 = 0; SEL2 = 1)

If SEL1 is Logic "0" and SEL2 is Logic "1", the part will be in the Audio Mute Mode. In the Audio Mute Mode, the audio switches are OFF (high impedance), the Audio Input Click and Pop shunt circuitry is inactive (high impedance), and the Audio Output connections are shorted through 6 $\Omega$  resistors to ground internal to the IC.

In Audio Mute Mode the ISL54406 IC has excellent Off Isolation for high performance muting of audio signals.

#### SHUTDOWN MODE (SEL1 = SEL2 = 0)

If SEL1 and SEL2 pins are Logic "0", the device will enter a low powered Shutdown Mode. In SHDN, the audio switches are OFF, the 6 $\Omega$  path is high impedance, the Click and Pop circuitry is inactive, and the device will draw a minimal amount of current.

Note: When the logic inputs are floated, the ISL54406 will automatically be placed in SHDN mode due to the internal 4M $\Omega$  pull-down resistors on the logic pins.

Note: Off-Isolation performance is degraded when the device is placed into SHDN. The design of the ISL54406 optimizes low current consumption in SHDN Mode, compromising Off-Isolation performance. Thus, SHDN Mode should not be used for muting audio if Off-Isolation is a concern.

Note: The ISL54406 should not be brought into Audio Playback mode directly from Shutdown mode. A DC transient may occur at the LOUT/ROUT pins when brought from Shutdown directly to Audio Playback mode. The recommended procedure is to place the ISL54406 into Mute mode for at least 100ms when entering or leaving Audio Playback mode.

#### CLICK AND POP OPERATION

Single supply audio sources are biased at a DC offset that generates transients during power on/off of the audio source. This DC offset is coupled through a blocking capacitor, causing a transient voltage at the load. When the source is off and suddenly turned on with a DC offset, the capacitor will develop a voltage equal to the DC offset. If the ISL54406 is in Audio mode, a transient discharge will occur in the speaker, generating a Click and Pop noise.

For proper operation of Click and Pop elimination, the ISL54406 should be placed in Click and Pop mode before the audio source is turned on or off. This allows any transients generated by the source to be discharged through the Click and Pop circuitry first. With a typical DC blocking capacitor of 200 $\mu$ F and the Click and Pop circuitry designed to have a impedance of 40 $\Omega$ , allowing a 100ms dead time in Click and Pop mode for discharging a transient when entering or leaving Audio Playback mode will eliminate the DC transient generated by the blocking capacitor.

## V+ SUPPLY SERIES RESISTOR

The ISL54406 evaluation board has an optional 100Ω series resistor on the V+ supply line. This resistor and the power supply decoupling capacitance form a low pass filter that improves PSRR of the ISL54406. Because the ISL54406 IC current draw is small, the power dissipation and voltage drop due to the 100Ω series resistor is minimal. If the user desires to have the series resistor, simply remove jumper JP4.

## Applications

The main purpose of the ISL54406 device is to eliminate the Click and Pop transients generated by single supply audio codecs and to be used as an audio mute switch for MP3 players, cell phones, and media applications that require audio switching.

## Board Component Definitions

DESIGNATOR	DESCRIPTION
U1	ISL54406IRUZ IC
J1	V+ Positive Connection
J2	GND Connection
J3, J4	SEL2 Logic Input
J5, J6	LOUT Audio Output
J7, J8	ROUT Audio Output
J9, J10	SEL1 Logic Input
J11, J12	LIN Audio Input
J13, J14	RIN Audio Input
S1	SPST Switch for SEL2
S2	SPST Switch for SEL1
HJ1	Stereo Headphone Jack

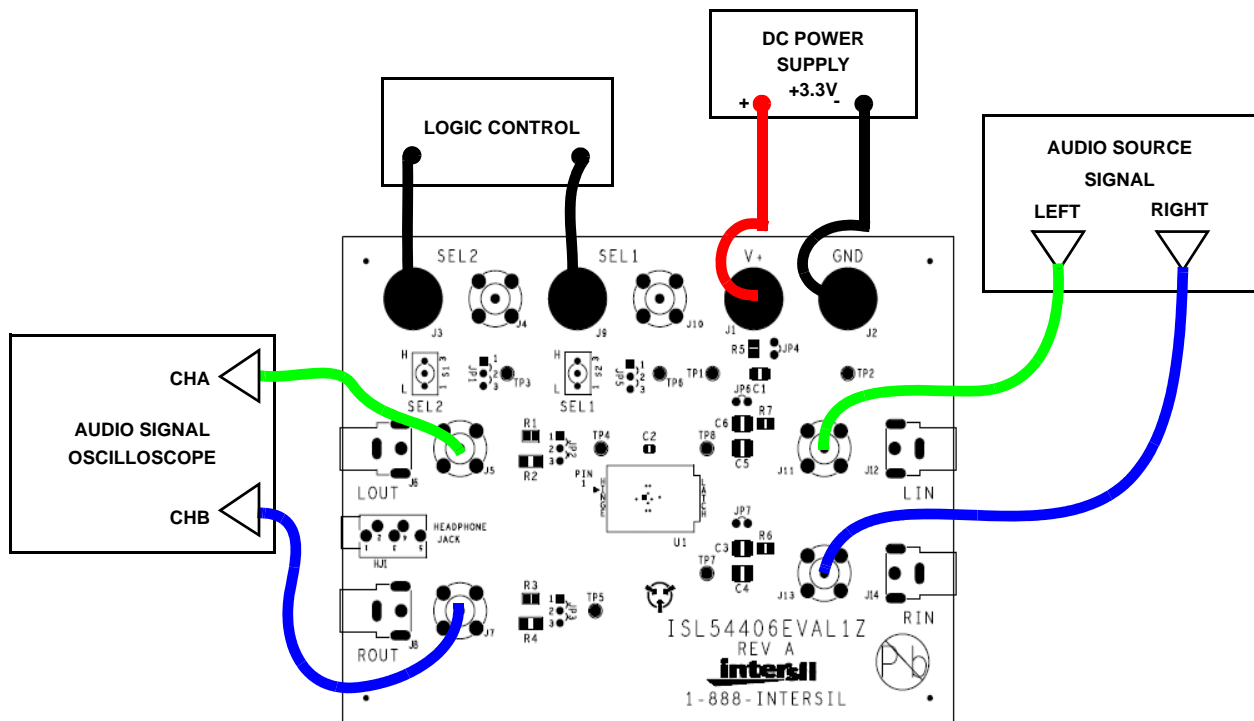


FIGURE 2. BASIC EVALUATION TEST SETUP BLOCK DIAGRAM

## Using the Board (Refer to Figure 2)

### Lab Equipment

The equipment, external supplies and signal sources needed to operate the board are listed below:

1. +2.7V to +3.6V DC Power Supply
2. Audio Signal Generator
3. Audio Signal Oscilloscope
4. Logic Control Generator and/or Pulse Generator

### Initial Board Setup Procedure

1. Attach the evaluation board to the DC power supply at J1 (V+) and J2 (GND). Positive terminal at J1 and negative terminal at J2. The supply should be capable of delivering +2.7V to +3.6V and 100 $\mu$ A of current. Set the supply voltage to +3.3V.
2. Connect the Audio Source Signal to the LIN and RIN BNC inputs (J11 and J13 respectively). The analog input voltage range should not exceed  $\pm 1.5V_{PEAK}$ .
3. Connect the Audio Signal Oscilloscope to the LOUT and ROUT BNC outputs (J5 and J7 respectively).
4. Connect the Logic Control generator to the SEL1 and SEL2 logic inputs.

### Audio Mode

1. With the DC power supply turned on, drive SEL1 and SEL2 to Logic "1" ( $> +1.4V$ ).
2. Select the desired load on the board using jumpers JP1 and JP2 or through external loading.
3. The audio switches are turned on and the audio inputs at LIN and RIN should be seen at the LOUT and ROUT.

### Click and Pop Mode

1. Drive SEL1 to Logic "1" and drive SEL2 to Logic "0" (or float SEL2).
2. The audio switch is now turned off. There is a 40 $\Omega$  impedance to ground at the LIN and RIN inputs. There is a 6 $\Omega$  impedance to ground at the LOUT and ROUT outputs.

### Mute Mode

1. Drive SEL1 to Logic "0" (or float SEL1) and drive SEL2 to Logic "1".
2. The audio switch is now turned off. There is a 6 $\Omega$  impedance to ground at the LOUT and ROUT outputs.

### Shutdown Mode

1. Drive SEL1 to Logic "0" (or float SEL1) and drive SEL2 to Logic "0" (or float SEL2).
2. The audio switch is now turned off. The LIN and RIN terminals are now high impedance. The LOUT and ROUT have an impedance of 220k $\Omega$  in parallel with the output load impedance.

### Test Points

The board has various test points for ease of connecting probes to make measurements. The test points available are described in Table 1.

**TABLE 1. TEST POINT DESCRIPTIONS**

DESIGNATOR	DESCRIPTION
TP1	V+ Test point
TP2	Ground Test Point
TP3	SEL2 Test Point
TP4	LOUT Test Point
TP5	ROUT Test Point
TP6	SEL1 Test Point
TP7	RIN Test Point
TP8	LIN Test Point

*Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)

# Board Schematic

