



PIC18F1220/1320

PIC18F1220/1320 Rev. B4 Silicon/Data Sheet Errata

The PIC18F1220/1320 Rev. B4 parts you have received conform functionally to the Device Data Sheet (DS39605C), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC18F1220/1320 silicon.

The following silicon errata apply only to PIC18F1220/1320 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F1220	00 0111 111	00100
PIC18F1320	00 0111 110	00100

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFEh:3FFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Core (DAW Instruction)

The DAW instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added, using an instruction such as INCFSZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW 0x80      ; .80 (BCD)
ADDLW 0x80      ; .80 (BCD)

BTFSC STATUS, C ; test C
INCFSZ byte2    ; inc next higher LSB
DAW
BTFSC STATUS, C ; test C
INCFSZ byte2    ; inc next higher LSB

This is repeated for each DAW instruction.
```

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: EUSART

The auto-baud measurement may not determine the correct baud rate if the ABDEN bit is set while the RB4/RX pin is low.

Work around

If the wake-up function is being used (WUE is set), wait for the RB4/RX pin to go high following a Break signal before setting the ABDEN bit.

If the wake-up function is not being used, ensure that RB4/RX is Idle (high between bytes) before setting the ABDEN bit.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Data EEPROM

When writing to the data EEPROM, the contents of the data EEPROM memory may not be written as expected.

Work around

Either of two work arounds can be used:

1. Before beginning any writes to the data EEPROM, enable the LVD (any voltage) and wait for the internal voltage reference to become stable. LVD interrupt requests may be ignored. Once the LVD voltage reference is stable, perform all EEPROM writes normally. When writes have been completed, the LVD may be disabled.
2. Configure the BOR as enabled (any voltage). Select a threshold below VDD to allow normal operation. If VDD is below the BOR threshold, the device will be held in Brown-out Reset.

Date Codes that pertain to this issue:

All engineering and production devices.

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4. Module: EUSART

The auto-baud measurement may not determine the correct baud rate if the resulting measurement could overflow the SPBRG register when measuring slow baud rates. In such cases, SPBRGH:SPBRG will contain 0x00FF.

Work around

Either or both of the following work arounds may be used:

1. Use a faster baud rate that can not result in auto-baud measurements greater than 0x00FF.
2. Clear the BRGH bit (TXSTA<2>). This divides the bit clock by 64 rather than dividing it by 16.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Reset

It has been observed that in certain Reset conditions, including power-up, the first GOTO instruction at address 0x0000 may not be executed. This occurrence is rare and affects very few applications.

To determine if your system is affected, test a statistically significant number of applications across the operating temperature, voltage and frequency ranges of the application. Affected systems will repeatably fail normal testing. Systems not affected will continue to not be affected over time.

Work around

Insert a NOP instruction at address 0x0000.

Date Codes that pertain to this issue:

All engineering and production devices.

Clarifications/Corrections to the Data Sheet

In the Device Data Sheet (DS39605C), the following clarifications and corrections should be noted.

1. Module: CCP

In **Section 14.0 “Timer3 Module”**, bit 6 of the T3CON register was incorrectly defined as “unimplemented”. The correct definition for T3CON<6> is T3CCP2 and is shown in **bold** below:

REGISTER 14-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	$\overline{T3SYNC}$	TMR3CS	TMR3ON	
bit 7								bit 0

bit 6, 3 **T3CCP2:T3CCP1:** Timer3 and Timer1 to CCP Enable bits
1x = Timer3 is the clock source for compare/capture CCP module
01 = **Reserved**
00 = Timer1 is the clock source for compare/capture CCP module

2. Module: Data EEPROM Memory

In Table 22-1 on page 254 of the Device Data Sheet, the typical value for parameter D122, Data EEPROM Erase/Write Cycle Time (TDEW) has changed. The new value is 5.5 ms and is shown in **bold** below.

TABLE 22-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D122	TDEW	Erase/Write Cycle Time	—	5.5	—	ms	

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REVISION HISTORY

Rev A Document (12/2003)

First revision of this document, silicon issues 1 (Core), 2 (EUSART) and 3 (Data EEPROM) and Data Sheet Clarification issues 1 (Internal RC Accuracy) and 2 (DC Characteristics Table).

Rev B Document (2/2004)

Added silicon issue 4 (EUSART). Added Data Sheet Clarification issue 3 (Timer1 Oscillator and In-Circuit Serial Programming).

Rev C Document (4/2004)

Added Data Sheet Clarification issues 4 (DC Characteristics) and 5 (LVD Characteristics).

Rev D Document (05/2005)

Added silicon issue 5 (Reset) and removed all Data Sheet Clarification issues with the exception of former issue 3 (Timer1 Oscillator and In-Circuit Serial Programming™), now numbered issue 1 and added issue 2 (CCP).

Rev E Document (08/2005)

Removed Data Sheet Clarification issue 1 and added issue 2 (Data EEPROM Memory).

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