A3250 and A3251

Field-Programmable, Chopper-Stabilized Unipolar Hall-Effect Switches

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: October 31, 2011

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

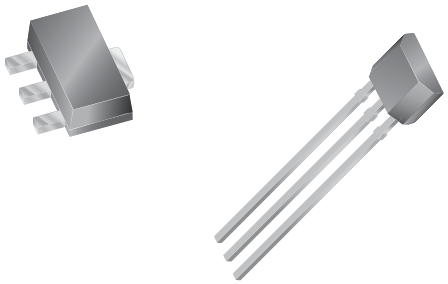
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Field-Programmable, Chopper-Stabilized Unipolar Hall-Effect Switches

Features and Benefits

- Chopper stabilization for stable switchpoints throughout operating temperature range
- Externally programmable operate point (through VCC pin)
- On-board voltage regulator for 4.2 V to 24 V operation
- On-chip protection against:
  - Supply transients
  - Output short-circuits
  - Reverse-battery condition

Package: 3-pin SOT89 (suffix LT) and 3-pin SIP (suffix UA)



Not to scale

Description

The A3250 and A3251 are field-programmable, chopper-stabilized, unipolar Hall-effect switches designed for use in high-temperature applications. These devices use a chopper-stabilization technique to eliminate offset inherent in single-element devices.

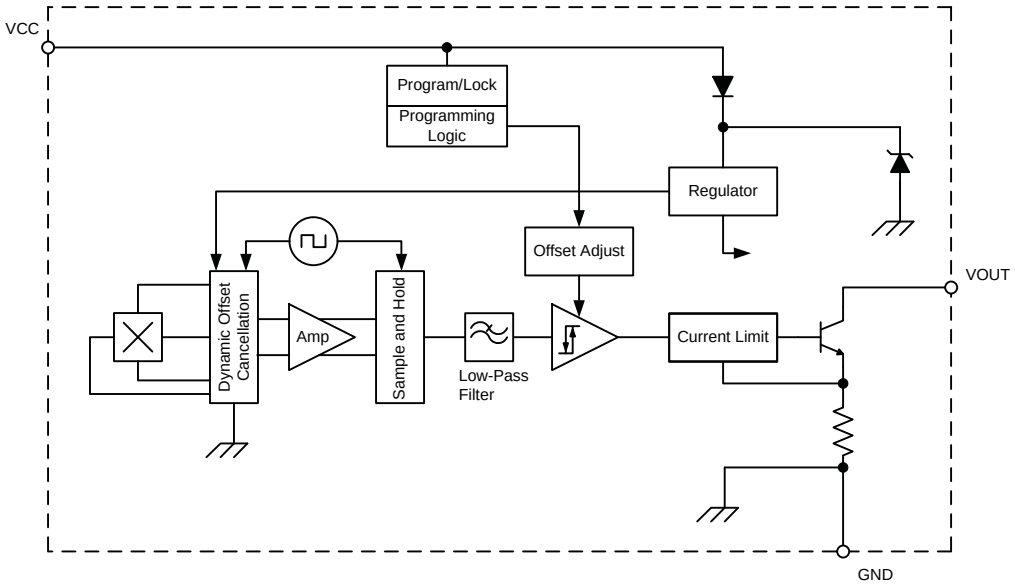
The A3250 and A3251 are externally programmable devices. The devices have a wide range of programmability of the magnetic operate point (B_{OP}) while the hysteresis remains fixed. This advanced feature allows for optimization of the device switchpoint and can drastically reduce the effects of variations found in a production environment, such as magnet and device placement tolerances.

These devices provide on-chip transient protection. A Zener clamp on the power supply protects against overvoltage conditions on the supply line. These devices also include short-circuit protection on the output.

The output of the A3250 switches LOW when subjected to a south-polarity magnetic field with a flux density that exceeds the threshold for B_{OP}, and switches HIGH when the field drops below the magnetic release point, B_{RP}. The output of the A3251 has the opposite polarity, switching HIGH in a south-polarity magnetic field that B_{OP}, and switching LOW when the field drops below B_{RP}.

Continued on the next page…

Functional Block Diagram



Description (continued)

The other differences in the devices are the power-on state. The A3250 powers-on in the HIGH state, while the A3251 powers-on in the LOW state.

Three package styles provide a magnetically optimized package for most applications. Type LT is a miniature SOT89/TO-243AA surface mount package that is thermally enhanced with an exposed ground tab, and type UA is a three-lead ultramini SIP for through-hole mounting. The packages are lead (Pb) free, with 100% matte tin plated leadframes (suffix, –T).

Selection Guide

Part Number	Packing[1]	Package	T_A (°C)	V_{OUT}	
				Power-On	Running[2]
A3250LLTTR-T	7-in. reel, 1000 pieces/reel	Surface mount	–40 to 150	High	Low

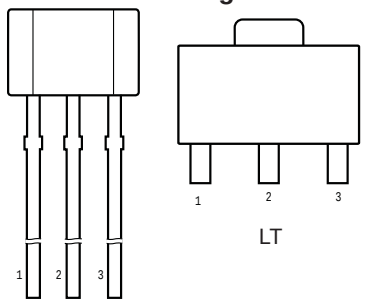
[1]Contact Allegro for additional packing options.

[2]In south polarity magnetic field of sufficient strength.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		26.5	V
Reverse Supply Voltage	V_{RCC}		–18	V
Zener Overvoltage	V_Z		30	V
Output Current	I_{OUT}		20	mA
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range L	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

Pin-out Diagrams



LT

UA

Terminal List

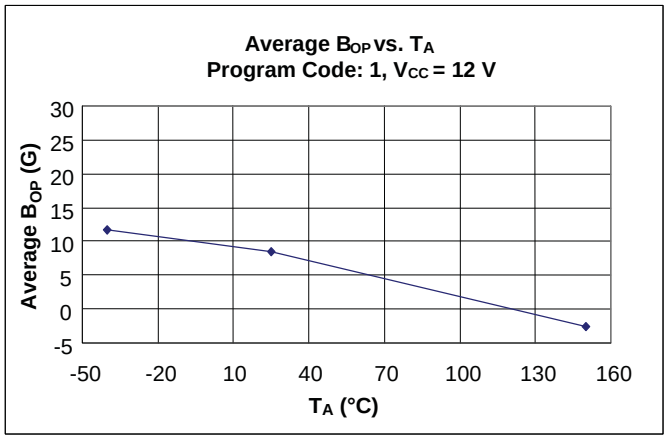
Number	Name	Function
1	VCC	Connects power supply to chip
2	GND	Ground
3	VOUT	Device output

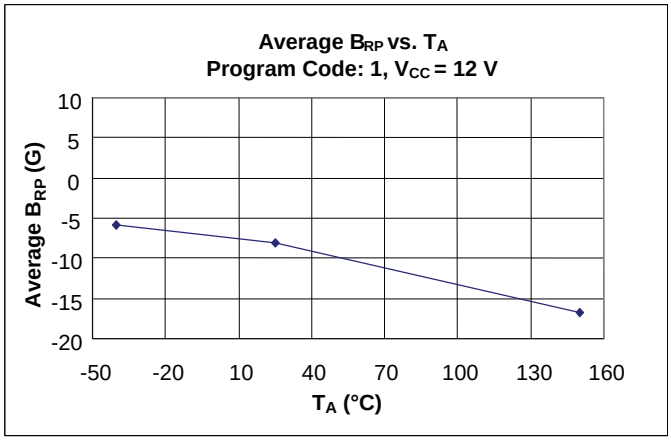
OPERATING CHARACTERISTICS valid over operating T_A and V_{CC}, unless otherwise specified						
Characteristic	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
ELECTRICAL CHARACTERISTICS						
Supply Voltage[1]	V_{CC}	Running mode	4.2	–	24	V
Output Saturation Voltage	$V_{OUT(sat)}$	I_{OUT} = 20 mA; Switch state = ON	–	175	400	mV
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V; Switch state = OFF	–	–	10	µA
Supply Current	$I_{CC(off)}$	A3250; B < B_{RP}; V_{OUT} = HIGH	–	4.0	7.0	mA
		A3251; B > B_{OP}; V_{OUT} = HIGH	–	4.0	7.0	mA
	$I_{CC(on)}$	A3250; B > B_{OP}; V_{OUT} = LOW	–	6.0	10.0	mA
		A3251; B < B_{RP}; V_{OUT} = LOW	–	6.0	10.0	mA
Output Rise Time	t_r	R_{LOAD} = 820 Ω, C_{LOAD} = 10 pF	–	–	5.0	µs
Output Fall Time	t_f	R_{LOAD} = 820 Ω, C_{LOAD} = 10 pF	–	–	5.0	µs
Chopping Frequency	f_C		–	340	–	kHz
Power-Up Time	t_{on}	V_{OUT} = HIGH	–	20	50	µs
Output Current Limit[1,2]	$I_{OUT(lim)}$	Short-circuit protection	60	90	120	mA
Power-On State	POS	A3250; B < B_{RP}, t > t_{on}	–	HIGH	–	mV
		A3251; B < B_{RP}, t > t_{on}	–	LOW	–	mV
MAGNETIC CHARACTERISTICS						
Initial Operate Point	B_{OP}		–20	13	50	G
Temperature Drift of B_{OP}	ΔB_{OP}	B_{OP} ≤ 500 gauss	–35	–	35	G
Hysteresis (B_{OP} – B_{RP})	B_{hys}	Package T_A range = J	5.0	18	35	G
		Package T_A range = L	5.0	13	35	G
PROGRAMMING CHARACTERISTICS						
Programmable B_{OP} Values[3]	$B_{OP(prog)}$		50	–	≥350	G
Number of Programming Bits	–	Switchpoint set	–	6	–	Bit
		Programming lock	–	1	–	Bit
Resolution	B_{RES}		–	7.0	–	G
TRANSIENT PROTECTION CHARACTERISTICS						
Supply Zener Voltage	V_Z		28	–	–	V
Supply Zener Current	I_Z	V_{CC} = 28 V	–	–	13	mA
Reverse Battery Current	I_{RCC}	V_{RCC} = –18 V, T_J < $T_{J(max)}$	–	–	–5.0	mA

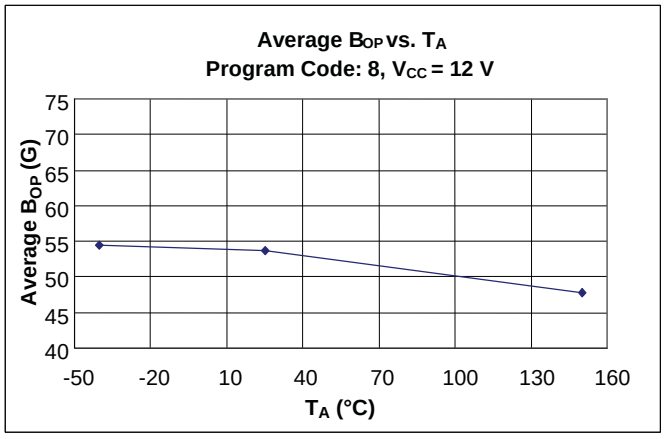
[1] Do not exceed T_J(max): Additional information on power derating is provided in the applications section.
[2] Short-circuit protection is not intended for continuous operation; permanent damage may result.
[3] Device can be used below 50 G but is not guaranteed to be a unipolar switch. It is the responsibility of the programmer to verify that the desired switchpoint has been achieved.

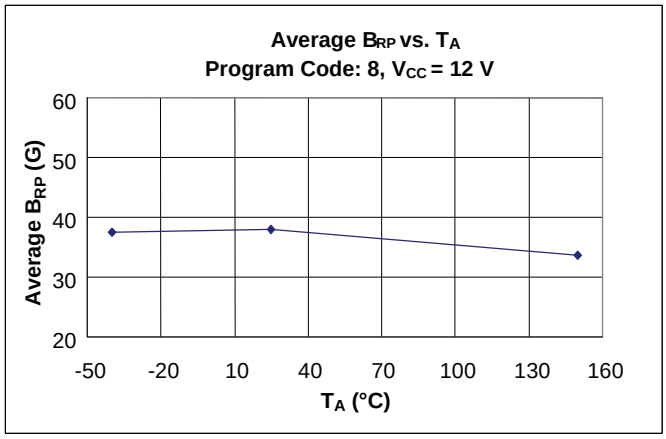
Typical Characterization Data

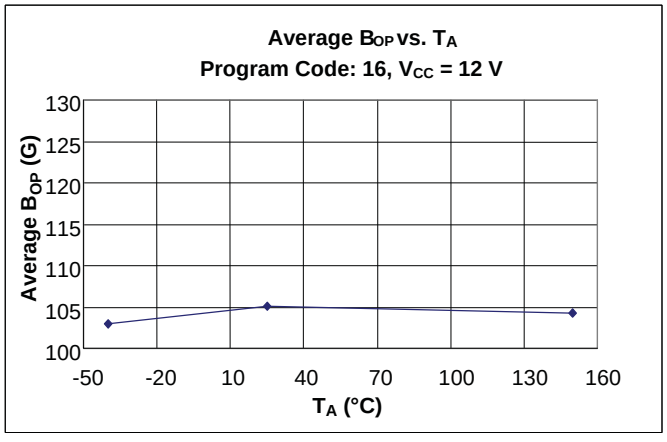
All data are taken with A3250 devices, the average of 3 lots, 30 pieces per lot

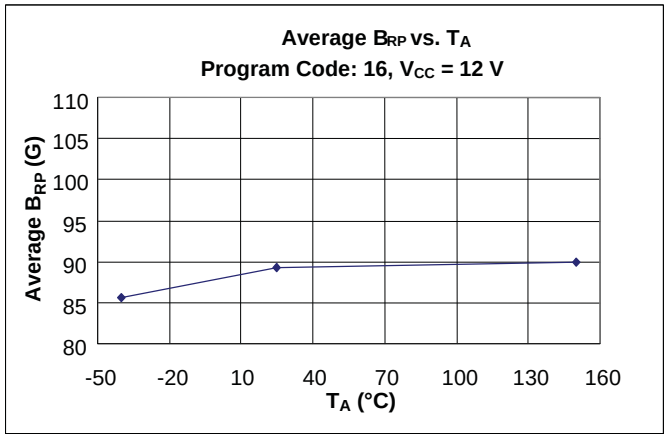






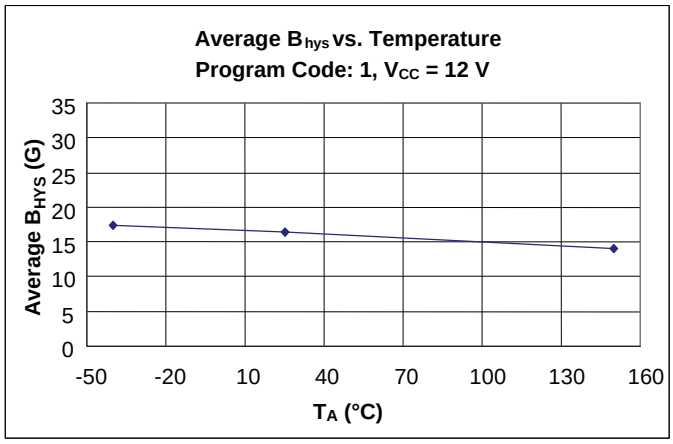


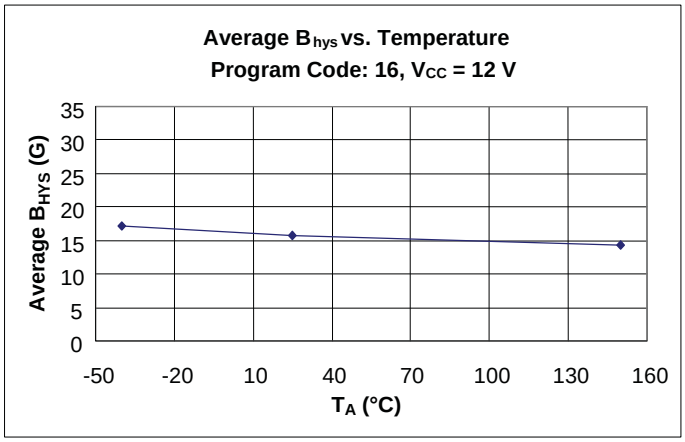


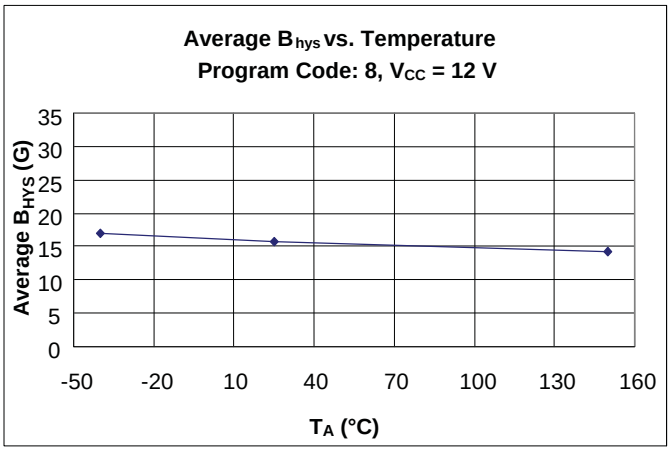


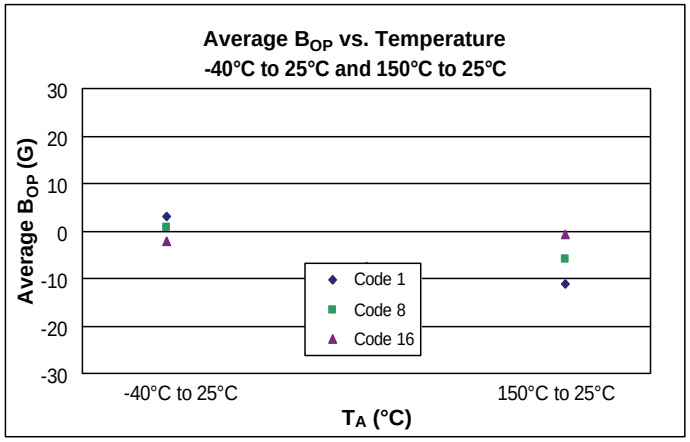
Typical Characterization Data

All data are taken with A3250 devices, the average of 3 lots, 30 pieces per lot



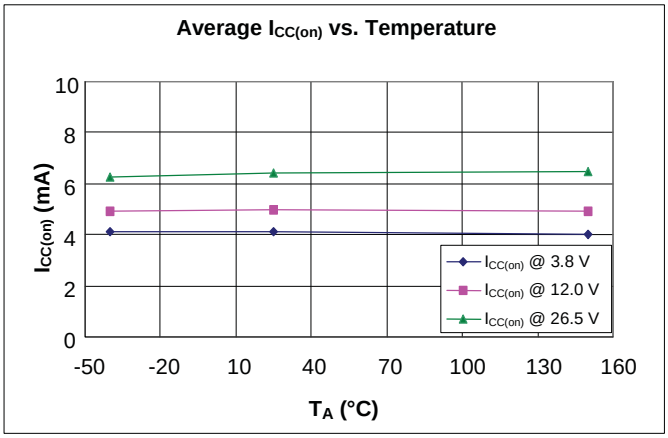


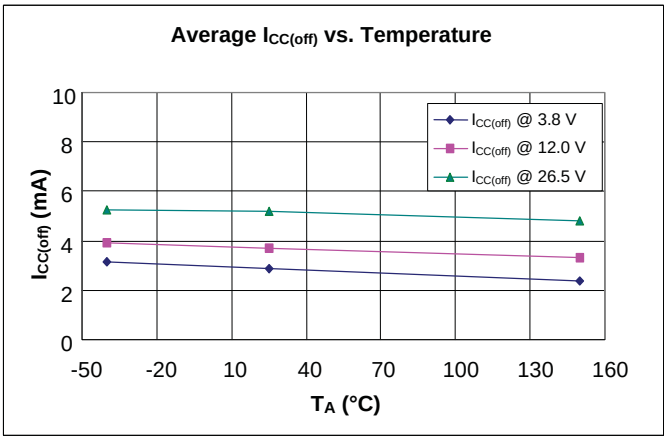


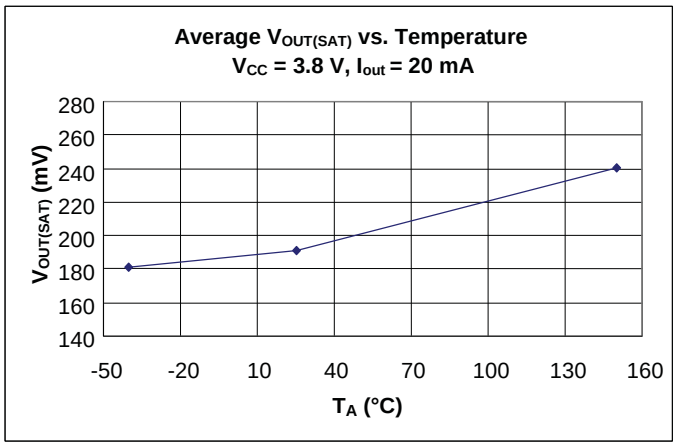


Typical Characterization Data

All data are taken with A3250 devices, the average of 3 lots, 30 pieces per lot

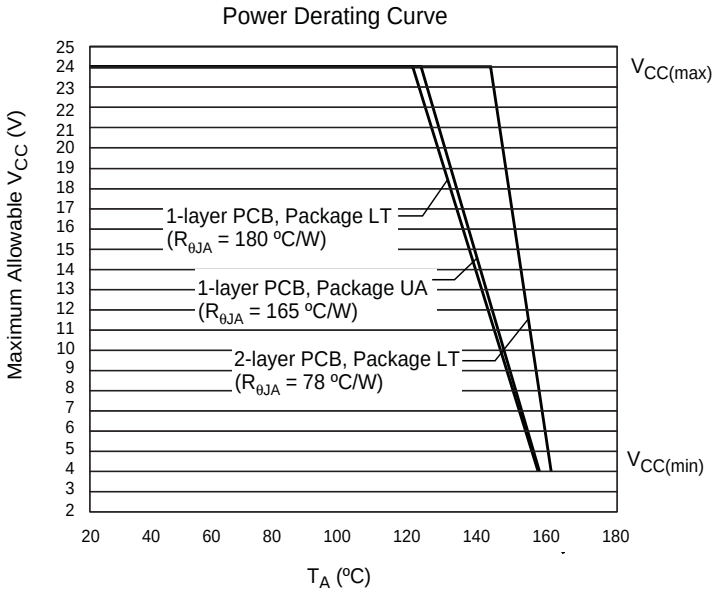


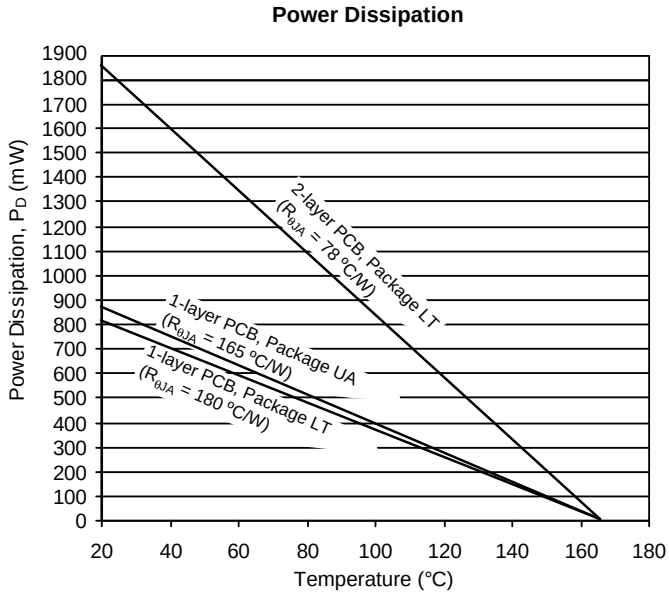




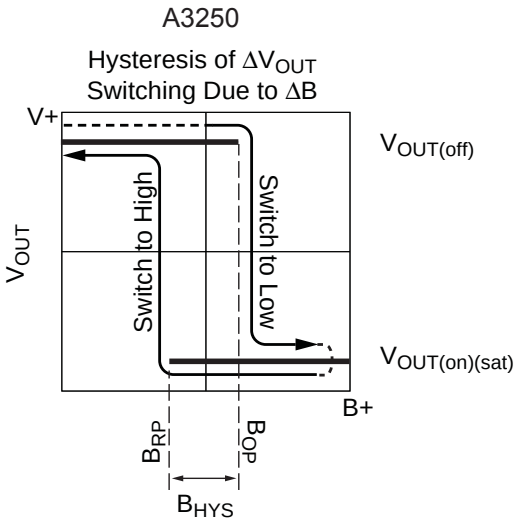
THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

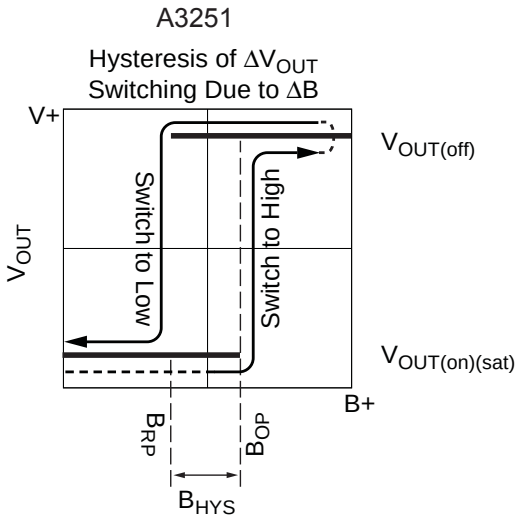
Characteristic	Symbol	Test Conditions	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W
		Package LT, 1-layer PCB with copper limited to solder pads	180	ºC/W
		Package LT, 2-layer PCB with 0.94 in^2 copper each side	78	ºC/W





Hysteresis Curves





Output voltage in relation to impinging magnetic flux density in a south polarity magnetic field of sufficient strength. Transition through B_{OP} must precede transition through B_{RP}.

Functional Description

Chopper-Stabilized Technique

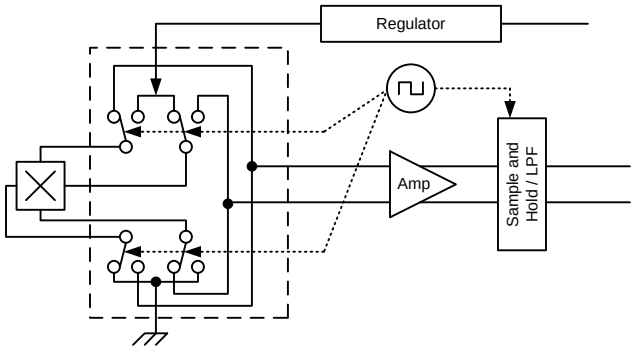
The Hall circuit is based on a Hall element, a small sheet of semiconductor material in which a constant bias current flows when a constant voltage source is applied. The output takes the form of a voltage measured across the width of the Hall element, and has negligible value in the absence of a magnetic field. When a magnetic field is applied with flux lines at right angles to the current in the Hall element, a small signal voltage directly proportional to the strength of the magnetic field occurs at the output of the Hall element.

This small signal voltage is disproportionally small relative to the offset produced at the input of the device. This makes it very difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Therefore, it is important to reduce any distortion of the signal that could be amplified when the signal is processed.

Chopper stabilization is a unique approach used to minimize input offset on the Hall IC. This technique removes a key source of output drift due to temperature and mechanical stress, and produces a 3X reduction in offset in comparison to other, conventional methods.

This offset reduction chopping technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetically-induced signal in the frequency domain. The offset (and any low-frequency noise) component of the signal can be seen as signal distortion added after the signal modulation process has taken place. Therefore, the DC offset is not modulated and remains a low-frequency component. Consequently, the signal demodulation process acts as a modulation process for the offset, causing the magnetically-induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, the signal passes using a low-pass filter, while the modulated DC offset is suppressed.

The advantage of this approach is significant offset reduction, which desensitizes the Hall IC against the effects of temperature and mechanical stress. The disadvantage is that this technique features a demodulator that uses a sample-and-hold block to store and recover the signal. This sampling process can slightly degrade the SNR (signal-to-noise ratio) by producing replicas of the noise spectrum at the baseband. This degradation is a function of the ratio between the white noise spectrum and the sampling frequency. The effect of the degradation of the SNR is higher jitter, also known as signal repeatability. However, the jitter in a continuous-time device can be 5X that of the A3250/A3251.



Chopper stabilization circuit (dynamic quadrature offset cancellation)

Programming Protocol

The operate switchpoint, B_{OP}, can be field-programmed. To do so, a coded series of voltage pulses through the VCC pin is used to set bitfields in onboard registers. The effect on the device output can be monitored, and the registers can be cleared and set repeatedly until the required B_{OP} is achieved. To make the setting permanent, bitfield-level solid state fuses are blown, and finally, a device-level fuse is blown, blocking any further coding. It is not necessary to program the release switchpoint, B_{RP}, because the difference between B_{OP} and B_{RP}, referred to as the hysteresis, B_{HYS}, is fixed.

The range of values between $B_{OP(min)}$ and $B_{OP(max)}$ is scaled to 64 increments. The actual change in magnetic flux (G) represented by each increment is indicated by B_{RES} (see the Operating Characteristics table; however, testing is the only method for verifying the resulting B_{OP}). For programming, the 64 increments are individually identified using 6 data bits, which are physically represented by 6 bitfields in the onboard registers. By setting these bitfields, the corresponding calibration value is programmed into the device.

Three voltage levels are used in programming the device: a low voltage, V_{PL}, a minimum required to sustain register settings; a mid-level voltage, V_{PM}, used to increment the address counter in the device; and a high voltage, V_{PH}, used to separate sets of V_{PM} pulses (when short in duration) and to blow fuses (when long in duration). A fourth voltage level, essentially 0 V, is used to clear the registers between pulse sequences. The pulse values are shown in the Programming Protocol Characteristics table and in figure 1.

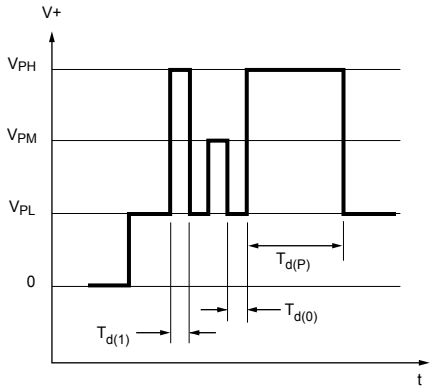


Figure 1. Pulse amplitudes and durations

Additional information on device programming and programming products is available on www. allegromicro.com. Programming hardware is available for purchase, and programming software is available free of charge.

Code Programming. Each bitfield must be individually set. To do so, a pulse sequence must be transmitted for each bitfield that is being set to 1. If more than one bitfield is being set to 1, all pulse sequences must be sent, one after the other, without allowing V_{CC} to fall to zero (which clears the registers).

The same pulse sequence is used to provisionally set bitfields as is used to permanently set bitfield-level fuses. The only difference is that when provisionally setting bitfields, no fuse-blowing pulse is sent at the end of the pulse sequence.

PROGRAMMING PROTOCOL CHARACTERISTICS, T_A = 25ºC, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Programming Voltage[1]	V_{PL}	Minimum voltage range during programming	4.5	5.0	5.5	V
	V_{PM}		10	11	12	V
	V_{PH}		23	25	26	V
Programming Current[2]	I_{PP}	Maximum supply current during programming	–	500	–	mA
Pulse Width	$t_{d(0)}$	OFF time between programming bits	20	–	–	µs
	$t_{d(1)}$	Pulse duration (ON time) for enable, address, fuse blowing or lock bits	20	–	–	µs
	$t_{d(P)}$	Pulse duration (ON time) for fuse blowing	100	300	–	µs
Pulse Rise Time	t_r	V_{PL} to V_{PM}; V_{PL} to V_{PH}	11	–	–	µs
Pulse Fall Time	t_f	V_{PM} to V_{PL}; V_{PH} to V_{PL}	5	–	–	µs

[1]Programming voltages are measured at the VCC pin.
[2]A bypass capacitor with a minimum capacitance of 0.1 µF must be connected from VCC to the GND pin of the device in order to provide the current necessary to blow the fuse.

The pulse sequences consist of the following groups of pulses:

1. An enable sequence.
2. A bitfield address sequence.
3. When permanently setting the bitfield, a long V_{PH} fuse-blowing pulse. (Note: Blown bit fuses cannot be reset.)
4. When permanently setting the bitfield, the level of V_{CC} must be allowed to drop to zero between each pulse sequence, in order to clear all registers. However, when provisionally setting bitfields, V_{CC} must be maintained at V_{PL} between pulse sequences, in order to maintain the prior bitfield settings while preparing to set additional bitfields.

Bitfields that are not set are evaluated as zeros. The bitfield-level fuses for 0 value bitfields are never blown. This prevents inadvertently setting the bitfield to 1. Instead, blowing the device-level fuse protects the 0 bitfields from being accidentally set in the future.

When provisionally trying the calibration value, one pulse sequence is used, using decimal values. The sequence for setting the value 5_{10} is shown in figure 2.

When permanently setting values, the bitfields must be set individually, and 5_{10} must be programmed as binary 101. Bit 3 is set to 1 (000100_2, which is 4_{10}), then bit 1 is set to 1 (000001_2, which is 1_{10}). Bit 2 is ignored, and so remains 0.Two pulse sequences for permanently setting the calibration value 5 are shown in figure 3. The final V_{PH} pulse is maintained for a longer period, enough to blow the corresponding bitfield-level fuse.

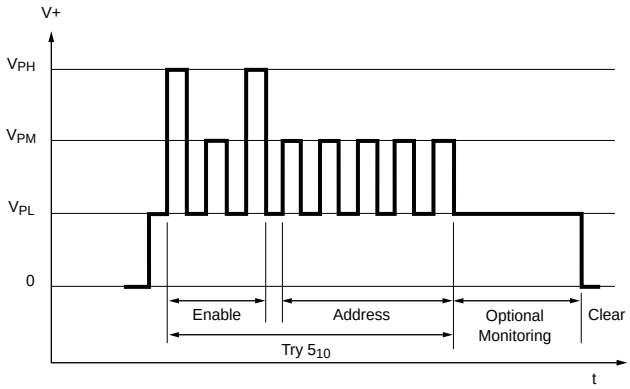


Figure 2. Pulse sequence to provisionally try calibration value 5.

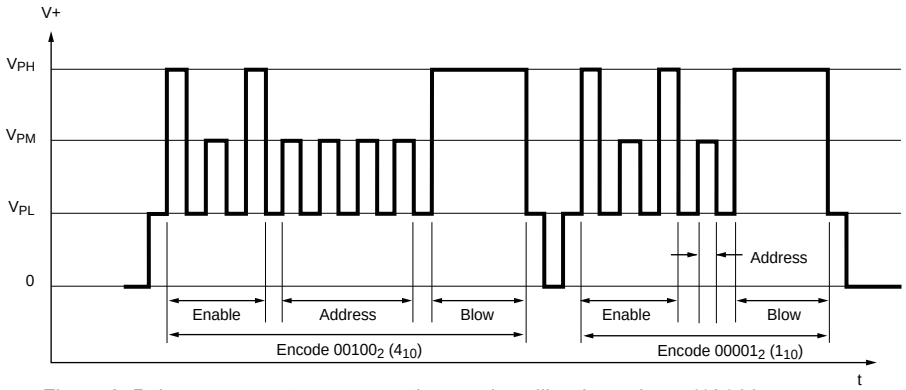


Figure 3. Pulse sequence to permanently encode calibration value 5 (101 binary, or bitfield address 3 and bitfield address 1).

Enabling Addressing Mode. The first segment of code is a keying sequence used to enable the bitfield addressing mode. As shown in figure 4, this segment consists of one short V_{PH} pulse, seven or more V_{PM} pulses, and one short V_{PH} pulse, with no supply interruptions. This sequence is designed to prevent the device from being programmed accidentally, such as by noise on the supply line.

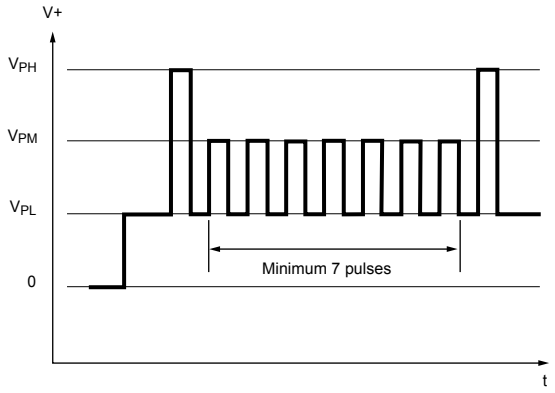


Figure 4. Addressing mode enable pulse sequence

Address Selection. After addressing mode is enabled, the target bitfield address, is indicated by a series of VPM pulses, as shown in figure 3. When provisionally trying a value, this sequence is followed by a short V_{PH} pulse, which serves to delimit the address and set the corresponding bitfield. When permanently setting a bitfield, the V_{PH} pulse is continued for a longer period of time, suffienct to not only set the bitfield to 1, but also to blow the bitfield fuse.

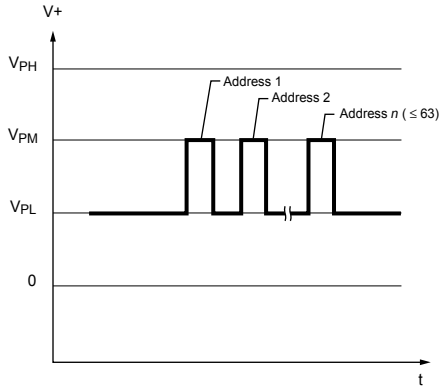


Figure 5. Pulse sequence to select addresses

Lock Bit Programming. After the desired B_{OP} calibration value is programmed, and all of the corresponding bitfield-level fuses are blown, the device-level fuse should be blown. To do so, the lock bit (bitfield address 65) should be encoded as 1 and have its fuse blown. This is done in the same manner as permanently setting the other bitfields, as shown in figure 6.

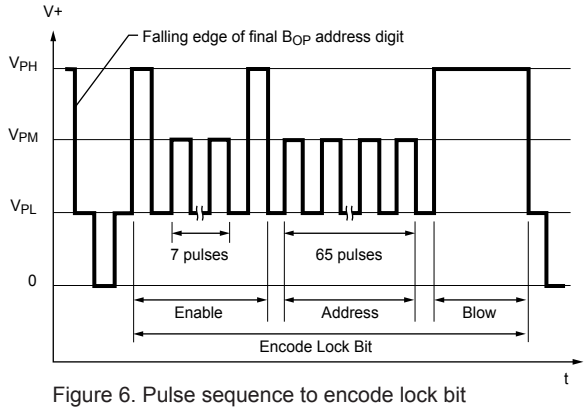


Figure 6. Pulse sequence to encode lock bit

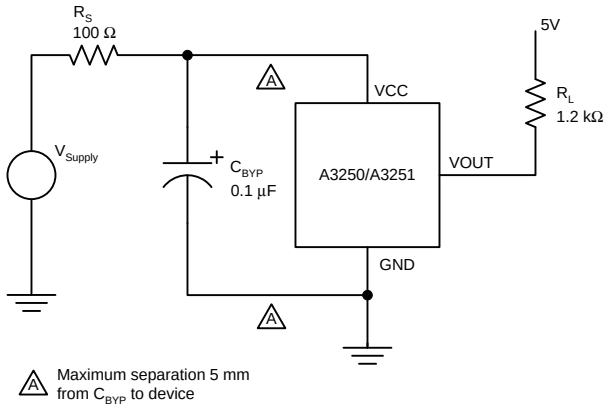
Application Information

For additional general application information, visit the Allegro MicroSystems Web site at www. allegromicro.com.

Typical Application Circuit

It is strongly recommended that an external ceramic bypass capacitor, C_{BYP}, in the range of 0.01 µF to 0.1 µF be connected between the VCC pin and the supply and GND pin to reduce both external noise and noise generated by the chopper-stabilization technique. (The diagram at the right shows C_{BYP} at 0.1 µF.) C_{BYP} should be installed so that the traces that connect it to the A3250/A3251 are no greater than 5 mm in length. (For programming the device, the capacitor may be further away from the device, including mounting on the board used for programming the device.)

The series resistor R_S, in combination with C_{BYP} creates a filter for EMI pulses. (Additional information on EMC is provided on the Allegro MicroSystems Web site.) R_S will have a drop of approximately 800 mV. This must be taken into consideration when determining the minimum VCC requirement for the A3250/A3251. The pull-up resistor, R_L, should be chosen to limit the current through the output transistor; do not exceed the maximum continuous output current of the device.



Typical application circuit

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \qquad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \qquad (2)$$

$$T_J = T_A + \Delta T \qquad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4 mA, and $R_{\theta JA}$ = 165 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 165\ °C/W = 8°C$$

$$T_J = T_A + \Delta T = 25°C + 8°C = 33°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UA, using minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=165°C/W, $T_{J(max)}$=165°C, $V_{CC(max)}$= 24 V, and $I_{CC(max)}$ = 10 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165\ °C/W = 91\ mW$$

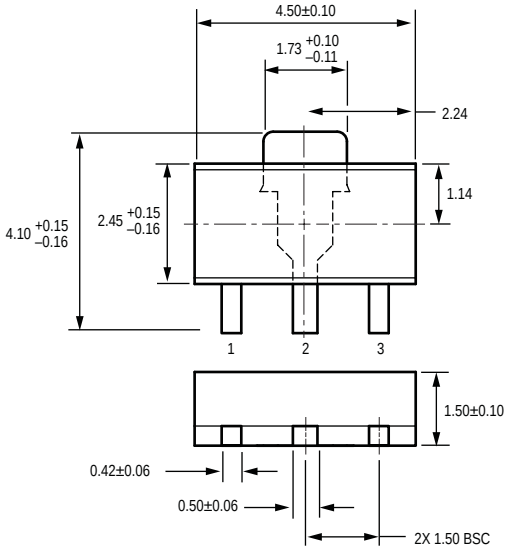
Finally, invert equation 1 with respect to voltage:

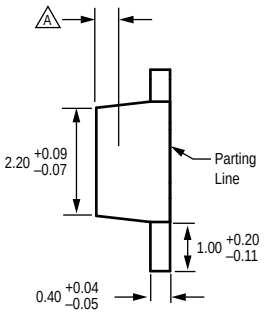
$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 91\ mW \div 10\ mA = 9\ V$$

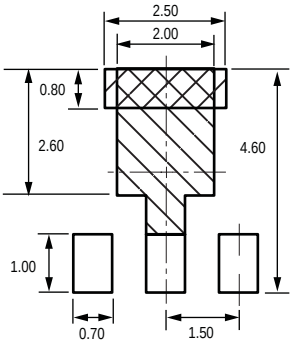
The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

Package LT, 3-Pin SOT89







B PCB Layout Reference View

Basic pads for low-stress, not self-aligning
Additional pad for low-stress, self-aligning
Additional area for IPC reference layout

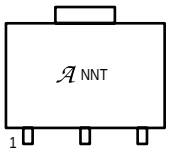
For Reference Only; not for tooling use (reference JEDEC. TO-243AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Active Area Depth, 0.78 mm REF

B Reference land pattern layout (reference IPC7351 SOT89N);
All pads a minimum of 0.20 mm from all adjacent pads;
adjust as necessary to meet application process
requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

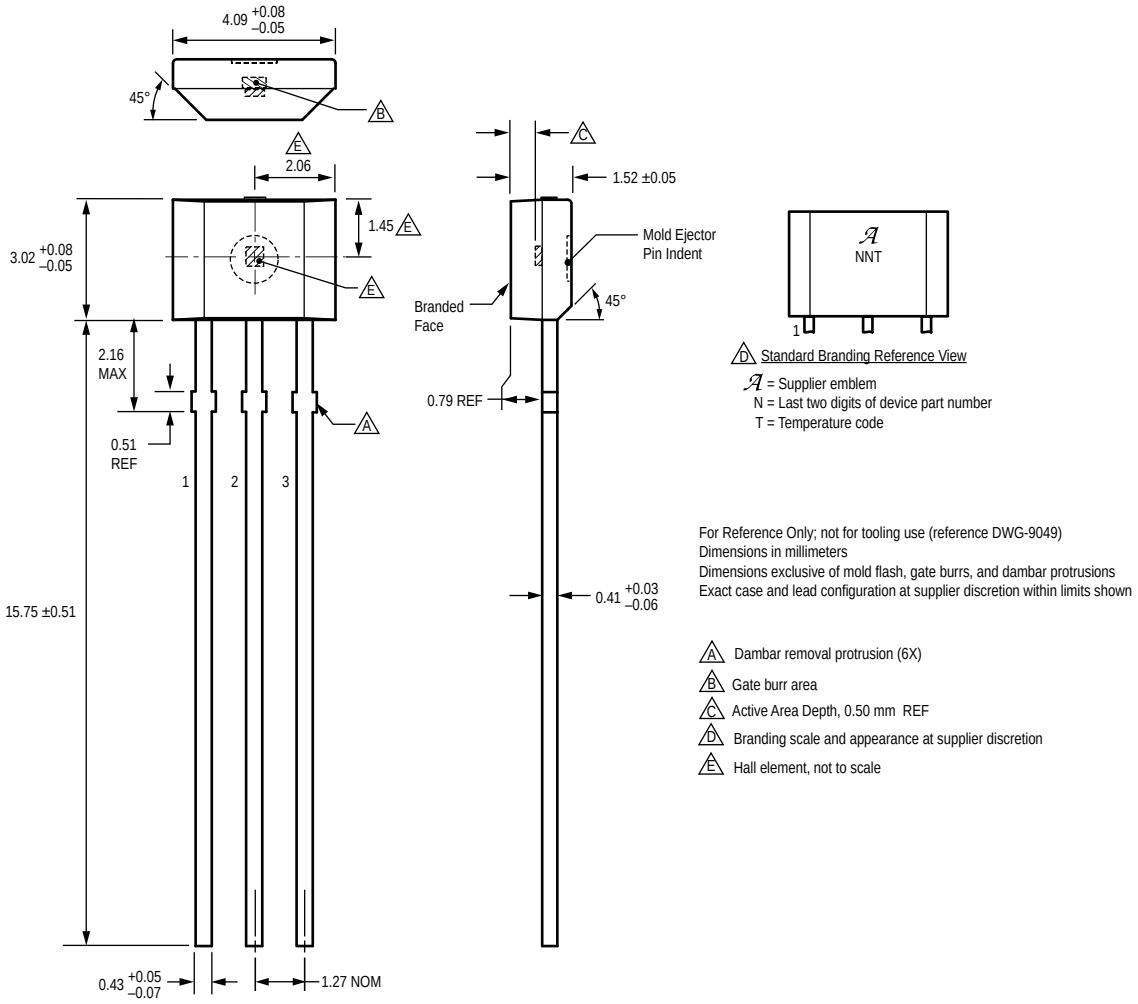
D Hall element, not to scale



C Standard Branding Reference View

A = Supplier emblem
N = Last two digits of device part number
T = Temperature code

Package UA, 3-Pin SIP



For the latest version of this document, visit our website:
www.allegromicro.com