

# XS1-G02B-FB144 Datasheet

---

Document Number: 1100C

**Not for New Designs**

Publication Date: 2011/05/16

Copyright © 2010 XMOS Limited, All Rights Reserved.



## Table of Contents

1	Features	2
2	Pin Configuration	3
3	Signal Description	4
4	Block Diagram	7
5	Product Overview	8
6	DC and Switching Characteristics	15
7	Package Information	19
8	Ordering Information	20
9	Development Tools	20
10	Addendum: XMOS USB Interface	20
11	Associated Design Documentation	21
12	Related Documentation	22
13	Revision History	23

### TO OUR VALUED CUSTOMERS

It is our intention to provide you with accurate and comprehensive documentation for the hardware and software components used in this product. To subscribe to receive updates, visit <http://www.xmos.com/>.

XMOS Ltd. is the owner or licensee of the information in this document and is providing it to you “AS IS” with no warranty of any kind, express or implied and shall have no liability in relation to its use. XMOS Ltd. makes no representation that the information, or any particular implementation thereof, is or will be free from any claims of infringement and again, shall have no liability in relation to any such claims.

XMOS and the XMOS logo are registered trademarks of XMOS Ltd in the United Kingdom and other countries, and may not be used without written permission. Company and product names mentioned in this document are the trademarks or registered trademarks of their respective owners.

## 1 Features

- ▶ **Dual-Core Device with Advanced Multi-Threaded RISC Architecture**
  - Up to 800 MIPS shared between up to 16 real-time threads
  - Each thread has:
    - Guaranteed throughput of between  $\frac{1}{4}$  and  $\frac{1}{8}$  of core MIPS
    - 16x32bit dedicated registers
  - 159 high-density 16/32-bit instructions
    - All have single clock-cycle execution (except for divide)
    - High-performance DSP (32x32→64-bit MAC) and cryptographic instructions
- ▶ **Programmable I/O**
  - 88 general-purpose I/O pins, configurable as input, output or bi-directional ports
  - Port sampling rates of up to 60 MHz with respect to an external clock
  - 64 channel ends for communication with other threads, on or off-chip
- ▶ **Non-Volatile Memory**
  - 128KB internal single-cycle SRAM (max 64KB per core) for code and data storage
  - 32KB internal OTP (max 8KB per core) for application boot code
- ▶ **JTAG Module for On-Chip Debug**
- ▶ **Security Features**
  - Programming lock disables debug and prevents read-back of memory contents
  - AES bootloader ensures secrecy of IP held on external flash memory
- ▶ **Ambient Temperature Range**
  - Commercial qualification: 0 °C to 70 °C
  - Industrial qualification: -40 °C to 85 °C
- ▶ **Speed Grade**
  - 400 MHz part: 400 MIPS
- ▶ **144-pin FBGA package 0.8 mm pitch**

## 2 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12
A	IO VDD	X0D34	X0D35	X0D36	X0D37	X0D38	X0D39	X0D40	X0D41	X0D42	X0D43	VSS
B	X0D33	VSS	X0D18	X0D19	X0D20	IO VDD	VSS	X0D21	X0D22	X0D23	IO VDD	X2D24
C	X0D32	X0D17	VDD	X0D06	X0D07	X0D08	X0D09	X0D10	X0D11	VDD	X2D12	X2D25
D	X0D31	X0D16	X0D05	SS_PLL_BYPASS	SS_RESET	VDD	SS_OTP_VPP	SS_XC0_BS[0]	SS_XC_CFG[0]	X2D00	X2D13	X2D26
E	X0D30	X0D15	X0D04	SS_CLK	VSS	VSS	VSS	VSS	DEBUG_N	X2D01	X2D14	X2D27
F	X0D29	IO VDD	X0D03	SS_PLL_AGND	VSS	VSS	VSS	VSS	VDD	X2D02	VSS	X2D28
G	X0D28	VSS	X0D02	VDD	VSS	VSS	VSS	VSS	SS_TEST_ENA	X2D03	IO VDD	X2D29
H	X0D27	X0D14	X0D01	SS_PLL_AVDD	VSS	VSS	VSS	VSS	SS_TCK	X2D04	X2D15	X2D30
J	X0D26	X0D13	X0D00	SS_PLL_LOCK	SS_TMS	SS_TDO	VDD	SS_TDI	SS_TRST	X2D05	X2D16	X2D31
K	X0D25	X0D12	VDD	X2D11	X2D10	X2D09	X2D08	X2D07	X2D06	VDD	X2D17	X2D32
L	X0D24	IO VDD	X2D23	X2D22	X2D21	VSS	IO VDD	X2D20	X2D19	X2D18	VSS	X2D33
M	VSS	X2D43	X2D42	X2D41	X2D40	X2D39	X2D38	X2D37	X2D36	X2D35	X2D34	IO VDD

### 3 Signal Description

Module	Signal	Function	Type	Active	Properties
PU=Pull Up, PD=Pull Down, ST=Schmitt Trigger, OT=Output Tristate, S=Switchable R <sub>S</sub> =Required for SPI boot (§5.8), R <sub>U</sub> =Required for USB-enabled devices (§10)					
Power	VSS	Digital ground	GND	—	
	VDD	Digital core power	PWR	—	
	IO VDD	Digital I/O power	PWR	—	
	SS_PLL_AGND	Analog ground for PLL	GND	—	
	SS_PLL_AVDD	Analog PLL power	PWR	—	
	SS_OTP_VPP	OTP programming voltage	PWR	—	
	SS_RESET	Global reset input	Input	—	PU, ST
PLL	SS_CLK	PLL reference clock	Input	—	PD, ST
	SS_PLL_BYPASS	PLL bypass	Input	—	PD
	SS_XCO_BS[0:0]	Boot status (core 0)	I/O	—	PU
JTAG	SS_TDI	Test data input	Input	—	PU, ST
	SS_TDO	Test data output	Output	—	PD
	SS_TMS	Test mode select	Input	—	PU, ST
	SS_TRST	Test reset input	Input	—	PU, ST
	SS_TCK	Test clock	Input	—	PU
	DEBUG_N	Multi-chip debug	I/O	Low	PU
XCore 0 I/O	X0D00	P1A <sup>0</sup>	I/O	—	R <sub>S</sub>
	X0D01	X0LA <sub>5b</sub> <sup>4i</sup> P1B <sup>0</sup>	I/O	—	R <sub>S</sub>
	X0D02	X0LA <sub>5b</sub> <sup>3i</sup> P4A <sup>0</sup> P8A <sup>0</sup> P16A <sup>0</sup> P32A <sup>20</sup>	I/O	—	R <sub>U</sub>
	X0D03	X0LA <sub>5b</sub> <sup>2i</sup> P4A <sup>1</sup> P8A <sup>1</sup> P16A <sup>1</sup> P32A <sup>21</sup>	I/O	—	R <sub>U</sub>
	X0D04	X0LA <sub>5b</sub> <sup>1i</sup> P4B <sup>0</sup> P8A <sup>2</sup> P16A <sup>2</sup> P32A <sup>22</sup>	I/O	—	R <sub>U</sub>
	X0D05	X0LA <sub>5b</sub> <sup>0i</sup> P4B <sup>1</sup> P8A <sup>3</sup> P16A <sup>3</sup> P32A <sup>23</sup>	I/O	—	R <sub>U</sub>
	X0D06	X0LA <sub>5b</sub> <sup>0o</sup> P4B <sup>2</sup> P8A <sup>4</sup> P16A <sup>4</sup> P32A <sup>24</sup>	I/O	—	R <sub>U</sub>
	X0D07	X0LA <sub>5b</sub> <sup>1o</sup> P4B <sup>3</sup> P8A <sup>5</sup> P16A <sup>5</sup> P32A <sup>25</sup>	I/O	—	R <sub>U</sub>
	X0D08	X0LA <sub>5b</sub> <sup>2o</sup> P4A <sup>2</sup> P8A <sup>6</sup> P16A <sup>6</sup> P32A <sup>26</sup>	I/O	—	R <sub>U</sub>
	X0D09	X0LA <sub>5b</sub> <sup>3o</sup> P4A <sup>3</sup> P8A <sup>7</sup> P16A <sup>7</sup> P32A <sup>27</sup>	I/O	—	R <sub>U</sub>
	X0D10	X0LA <sub>5b</sub> <sup>4o</sup> P1C <sup>0</sup>	I/O	—	R <sub>S</sub>
	X0D11	P1D <sup>0</sup>	I/O	—	R <sub>S</sub>
	X0D12	P1E <sup>0</sup>	I/O	—	R <sub>U</sub>
	X0D13	X0LB <sub>5b</sub> <sup>4i</sup> P1F <sup>0</sup>	I/O	—	R <sub>U</sub>
	X0D14	X0LB <sub>5b</sub> <sup>3i</sup> P4C <sup>0</sup> P8B <sup>0</sup> P16A <sup>8</sup> P32A <sup>28</sup>	I/O	—	R <sub>U</sub>
	X0D15	X0LB <sub>5b</sub> <sup>2i</sup> P4C <sup>1</sup> P8B <sup>1</sup> P16A <sup>9</sup> P32A <sup>29</sup>	I/O	—	R <sub>U</sub>
	X0D16	X0LB <sub>5b</sub> <sup>1i</sup> P4D <sup>0</sup> P8B <sup>2</sup> P16A <sup>10</sup>	I/O	—	R <sub>U</sub>
	X0D17	X0LB <sub>5b</sub> <sup>0i</sup> P4D <sup>1</sup> P8B <sup>3</sup> P16A <sup>11</sup>	I/O	—	R <sub>U</sub>
	X0D18	X0LB <sub>5b</sub> <sup>0o</sup> P4D <sup>2</sup> P8B <sup>4</sup> P16A <sup>12</sup>	I/O	—	R <sub>U</sub>
	X0D19	X0LB <sub>5b</sub> <sup>1o</sup> P4D <sup>3</sup> P8B <sup>5</sup> P16A <sup>13</sup>	I/O	—	R <sub>U</sub>
	X0D20	X0LB <sub>5b</sub> <sup>2o</sup> P4C <sup>2</sup> P8B <sup>6</sup> P16A <sup>14</sup> P32A <sup>30</sup>	I/O	—	R <sub>U</sub>
X0D21	X0LB <sub>5b</sub> <sup>3o</sup> P4C <sup>3</sup> P8B <sup>7</sup> P16A <sup>15</sup> P32A <sup>31</sup>	I/O	—	R <sub>U</sub>	

(continued)

Module	Name	Function	Type	Active	Properties
XCore 0 I/O	X0D22	X0LB <sup>4</sup> <sub>5b</sub> P1G <sup>0</sup>	I/O	—	RU
	X0D23	P1H <sup>0</sup>	I/O	—	RU
	X0D24	P1I <sup>0</sup>	I/O	—	
	X0D25	P1J <sup>0</sup>	I/O	—	
	X0D26	P4E <sup>0</sup> P8C <sup>0</sup> P16B <sup>0</sup>	I/O	—	RU
	X0D27	P4E <sup>1</sup> P8C <sup>1</sup> P16B <sup>1</sup>	I/O	—	RU
	X0D28	P4F <sup>0</sup> P8C <sup>2</sup> P16B <sup>2</sup>	I/O	—	RU
	X0D29	P4F <sup>1</sup> P8C <sup>3</sup> P16B <sup>3</sup>	I/O	—	RU
	X0D30	P4F <sup>2</sup> P8C <sup>4</sup> P16B <sup>4</sup>	I/O	—	RU
	X0D31	P4F <sup>3</sup> P8C <sup>5</sup> P16B <sup>5</sup>	I/O	—	RU
	X0D32	P4E <sup>2</sup> P8C <sup>6</sup> P16B <sup>6</sup>	I/O	—	RU
	X0D33	P4E <sup>3</sup> P8C <sup>7</sup> P16B <sup>7</sup>	I/O	—	RU
	X0D34	P1K <sup>0</sup>	I/O	—	
	X0D35	P1L <sup>0</sup>	I/O	—	
	X0D36	P1M <sup>0</sup> P8D <sup>0</sup> P16B <sup>8</sup>	I/O	—	
	X0D37	P1N <sup>0</sup> P8D <sup>1</sup> P16B <sup>9</sup>	I/O	—	RU
	X0D38	P1O <sup>0</sup> P8D <sup>2</sup> P16B <sup>10</sup>	I/O	—	RU
	X0D39	P1P <sup>0</sup> P8D <sup>3</sup> P16B <sup>11</sup>	I/O	—	RU
	X0D40	P8D <sup>4</sup> P16B <sup>12</sup>	I/O	—	RU
	X0D41	P8D <sup>5</sup> P16B <sup>13</sup>	I/O	—	RU
X0D42	P8D <sup>6</sup> P16B <sup>14</sup>	I/O	—	RU	
X0D43	P8D <sup>7</sup> P16B <sup>15</sup>	I/O	—	RU	
XCore 2 I/O	X2D00	P1A <sup>0</sup>	I/O	—	
	X2D01	X2LA <sup>4</sup> <sub>5b</sub> P1B <sup>0</sup>	I/O	—	
	X2D02	X2LA <sup>3</sup> <sub>5b</sub> P4A <sup>0</sup> P8A <sup>0</sup> P16A <sup>0</sup> P32A <sup>20</sup>	I/O	—	RU
	X2D03	X2LA <sup>2</sup> <sub>5b</sub> P4A <sup>1</sup> P8A <sup>1</sup> P16A <sup>1</sup> P32A <sup>21</sup>	I/O	—	RU
	X2D04	X2LA <sup>1</sup> <sub>2b/5b</sub> P4B <sup>0</sup> P8A <sup>2</sup> P16A <sup>2</sup> P32A <sup>22</sup>	I/O	—	RU
	X2D05	X2LA <sup>0</sup> <sub>2b/5b</sub> P4B <sup>1</sup> P8A <sup>3</sup> P16A <sup>3</sup> P32A <sup>23</sup>	I/O	—	RU
	X2D06	X2LA <sup>0</sup> <sub>2b/5b</sub> P4B <sup>2</sup> P8A <sup>4</sup> P16A <sup>4</sup> P32A <sup>24</sup>	I/O	—	RU
	X2D07	X2LA <sup>1</sup> <sub>2b/5b</sub> P4B <sup>3</sup> P8A <sup>5</sup> P16A <sup>5</sup> P32A <sup>25</sup>	I/O	—	RU
	X2D08	X2LA <sup>2</sup> <sub>5b</sub> P4A <sup>2</sup> P8A <sup>6</sup> P16A <sup>6</sup> P32A <sup>26</sup>	I/O	—	RU
	X2D09	X2LA <sup>3</sup> <sub>5b</sub> P4A <sup>3</sup> P8A <sup>7</sup> P16A <sup>7</sup> P32A <sup>27</sup>	I/O	—	RU
	X2D10	X2LA <sup>4</sup> <sub>5b</sub> P1C <sup>0</sup>	I/O	—	
	X2D11	P1D <sup>0</sup>	I/O	—	
	X2D12	P1E <sup>0</sup>	I/O	—	RU
	X2D13	X2LB <sup>4</sup> <sub>5b</sub> P1F <sup>0</sup>	I/O	—	RU
	X2D14	X2LB <sup>3</sup> <sub>5b</sub> P4C <sup>0</sup> P8B <sup>0</sup> P16A <sup>8</sup> P32A <sup>28</sup>	I/O	—	RU
	X2D15	X2LB <sup>2</sup> <sub>5b</sub> P4C <sup>1</sup> P8B <sup>1</sup> P16A <sup>9</sup> P32A <sup>29</sup>	I/O	—	RU
	X2D16	X2LB <sup>1</sup> <sub>2b/5b</sub> P4D <sup>0</sup> P8B <sup>2</sup> P16A <sup>10</sup>	I/O	—	RU
	X2D17	X2LB <sup>0</sup> <sub>2b/5b</sub> P4D <sup>1</sup> P8B <sup>3</sup> P16A <sup>11</sup>	I/O	—	RU
	X2D18	X2LB <sup>0</sup> <sub>2b/5b</sub> P4D <sup>2</sup> P8B <sup>4</sup> P16A <sup>12</sup>	I/O	—	RU
	X2D19	X2LB <sup>1</sup> <sub>2b/5b</sub> P4D <sup>3</sup> P8B <sup>5</sup> P16A <sup>13</sup>	I/O	—	RU
X2D20	X2LB <sup>2</sup> <sub>5b</sub> P4C <sup>2</sup> P8B <sup>6</sup> P16A <sup>14</sup> P32A <sup>30</sup>	I/O	—	RU	

(continued)

Module	Name	Function	Type	Active	Properties
XCore 2 I/O	X2D21	X2LB <sub>5b</sub> <sup>3o</sup> P4C <sup>3</sup> P8B <sup>7</sup> P16A <sup>15</sup> P32A <sup>31</sup>	I/O	—	R <sub>U</sub>
	X2D22	X2LB <sub>5b</sub> <sup>4o</sup> P1G <sup>0</sup>	I/O	—	R <sub>U</sub>
	X2D23	P1H <sup>0</sup>	I/O	—	R <sub>U</sub>
	X2D24	P1I <sup>0</sup>	I/O	—	
	X2D25	P1J <sup>0</sup>	I/O	—	
	X2D26	P4E <sup>0</sup> P8C <sup>0</sup> P16B <sup>0</sup>	I/O	—	R <sub>U</sub>
	X2D27	P4E <sup>1</sup> P8C <sup>1</sup> P16B <sup>1</sup>	I/O	—	R <sub>U</sub>
	X2D28	P4F <sup>0</sup> P8C <sup>2</sup> P16B <sup>2</sup>	I/O	—	R <sub>U</sub>
	X2D29	P4F <sup>1</sup> P8C <sup>3</sup> P16B <sup>3</sup>	I/O	—	R <sub>U</sub>
	X2D30	P4F <sup>2</sup> P8C <sup>4</sup> P16B <sup>4</sup>	I/O	—	R <sub>U</sub>
	X2D31	P4F <sup>3</sup> P8C <sup>5</sup> P16B <sup>5</sup>	I/O	—	R <sub>U</sub>
	X2D32	P4E <sup>2</sup> P8C <sup>6</sup> P16B <sup>6</sup>	I/O	—	R <sub>U</sub>
	X2D33	P4E <sup>3</sup> P8C <sup>7</sup> P16B <sup>7</sup>	I/O	—	R <sub>U</sub>
	X2D34	P1K <sup>0</sup>	I/O	—	
	X2D35	P1L <sup>0</sup>	I/O	—	
	X2D36	P1M <sup>0</sup> P8D <sup>0</sup> P16B <sup>8</sup>	I/O	—	
	X2D37	P1N <sup>0</sup> P8D <sup>1</sup> P16B <sup>9</sup>	I/O	—	R <sub>U</sub>
	X2D38	P1O <sup>0</sup> P8D <sup>2</sup> P16B <sup>10</sup>	I/O	—	R <sub>U</sub>
	X2D39	P1P <sup>0</sup> P8D <sup>3</sup> P16B <sup>11</sup>	I/O	—	R <sub>U</sub>
	X2D40	P8D <sup>4</sup> P16B <sup>12</sup>	I/O	—	R <sub>U</sub>
X2D41	P8D <sup>5</sup> P16B <sup>13</sup>	I/O	—	R <sub>U</sub>	
X2D42	P8D <sup>6</sup> P16B <sup>14</sup>	I/O	—	R <sub>U</sub>	
X2D43	P8D <sup>7</sup> P16B <sup>15</sup>	I/O	—	R <sub>U</sub>	
Reserved	SS_PLL_LOCK	Reserved (do not connect)	Output	—	PD
	SS_TEST_ENA	Reserved (tie to VSS)	Input	—	PD
	SS_XC_CFG[0:0]	Reserved (tie to IO VDD)	Input	—	PD

## 4 Block Diagram





## 5 Product Overview

The XMOS XS1-G02B-FB144 is a powerful device that provides a simple design process and highly-flexible solution to many applications. The device consists of two XCores, each comprising an event-driven processor with tightly integrated I/O and on-chip memory. The processors run multiple tasks simultaneously using hardware threads, each of which is guaranteed a slice of processing power and can execute computational code, control software and I/O interfaces. Threads use channels to exchange data within a core or across cores. The cores are connected via an integrated switch network, which uses a proprietary physical layer protocol, and which can also be used to add additional resources to a design. The I/O pins are driven using intelligent ports that can serialize data, interpret strobe signals and wait for scheduled times or events, making the device ideal for real-time control applications.

The device can be configured using a set of software components that are rapidly customized and composed. XMOS provides source code libraries for many standard components. The device can be programmed using high-level languages such as C/C++ and the XMOS-originated XC language. XC provides extensions to C that simplify the control over concurrency, I/O and time.

The XMOS toolchain includes compilers, a simulator, debugger and static timing analyzer. The combination of real-time software, a compiler and timing analyzer enables the programmer to close timings on components of the design without a detailed understanding of the hardware characteristics.

### 5.1 Threads, Synchronizers and Locks

Each XCore has up to eight active threads, which issue instructions down a shared four-stage pipeline. Instructions from the active threads are issued round-robin. If up to four threads are active, each thread is allocated a quarter of the processing cycles. If more than four threads are active, each thread is allocated at least  $1/n$  cycles (for  $n$  threads). Figure 1 shows the guaranteed thread performance depending on the number of threads used.

**Figure 1:**  
Thread  
performance

Speed Grade	Minimum MIPS per thread (for $n$ threads)							
	1	2	3	4	5	6	7	8
400 MHz	100	100	100	100	80	67	57	50

There is no way that the performance of a thread can be reduced below these predicted levels. Because threads may be delayed on I/O, however, their unused processor cycles can be taken by other threads. This means that for more than four threads, the performance of each thread is often higher than the predicted minimum.

## 5.2 Channel Ends, Links and Switch

Threads communicate using point-to-point connections formed between two channel ends. Between cores, channel communications are implemented over XMOS Links and routed through switches. The links operate in either 2bit/direction or 5bit/direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between XCores (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two cores. All packet communications can be multiplexed onto a single link. A total of eight 5bit links are available between both cores.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-G Link Performance and Design Guides, document number [X2215](#).

## 5.3 Ports and Clock Blocks

Ports provide an interface between the threads and I/O pins. The operation of each port is synchronized to a clock block. A clock block can be connected to an external clock input, or it can be run from the divided reference clock. A clock block can also output its signal to a pin. On reset, each port is connected to clock block 0, which runs from the reference clock.

The ports and links are multiplexed, allowing the pins to be configured for use by ports of different widths or links. If an XMOS Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

## 5.4 Timers

Timers are 32-bit counters that are relative to the reference clock. A timer is defined to tick every 10 ns. This value is derived from the reference clock, which is configured to tick at 100 MHz by default.

## 5.5 SRAM

Each XCore integrates a single 64 KB SRAM bank for both instructions and data. All internal memory is 32 bits wide, and instructions are either 16-bit or 32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one core clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

## 5.6 OTP

Each XCore integrates 8KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in 2k rows x 32-bit configuration which can be used to implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up.

### 5.6.1 Security Register

The security register enables the following security features:

- **Secure Boot:** The XCore is forced to boot from address 0 of the OTP, allowing the XCore boot ROM to be bypassed (see §5.8). This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.
- **Disable JTAG:** The JTAG interface is disabled, making it impossible for the processor state or memory content to be accessed via the JTAG interface.
- **Disable Link access:** Other processors are forbidden access to the processor state via the system switch.  
Disabling both JTAG and Link access transforms a core into a “secure island” with other cores free for non-secure user application code.
- **Disable Global Debug access:** Disables access to the SS\_DEBUG pin.
- **OTP Master and Sector Lock:** Further access to the OTP is prevented by setting the master lock. Locks can also be applied to each of the four OTP sectors individually.

These security features provide a strong level of protection and are sufficient for providing strong IP security.

## 5.7 PLL

The PLL is used to generate all on-chip clocks. SS\_CLK is the reference clock input. It should be supplied with a clock with monotonic rising edges and should be stable before SS\_RESET is taken high.

Many standard clock frequencies can be used with appropriate settings configured into the PLL. At boot time, before the PLL can be reconfigured, the PLL multiplier is set using the pins specified in the table in Figure 2. The PLL increases the clock frequency to the core frequency used to run the processor data path and the switch.

**Figure 2:**  
PLL boot modes

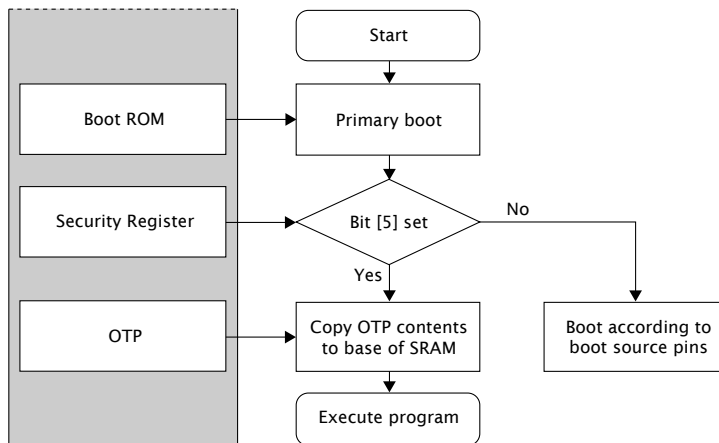
SS_PLL_BYPASS	PLL Multiplier	SS_CLK Input (MHz)	Boot Frequency (MHz)
0	20	12.5-20	250-400
1	0.5	<100	<50

Further details on configuring the clock can be found in the XS1-G Clock Frequency Control document, document number [X140](#).

### 5.8 Boot ROM

The boot procedure is illustrated in Figure 3. If bit 5 of the security register is set (see §5.6.1), the device boots from OTP. Otherwise, SS\_XC0\_BS[0] controls the boot source.

**Figure 3:**  
Boot procedure



SS\_XC0\_BS[0] operates as an input prior to the de-assertion of SS\_RESET. The device latches the value driven onto these pins on the rising edge (de-assertion) of SS\_RESET. The value driven should be static and configured using a pullup or pulldown resistor, as the device drives the boot status on this pin after reset. The value configured on this pin defines the boot mode, as described in Figure 4.

After reset is complete, SS\_XC0\_BS[0] becomes an output and indicates the boot mode, as described in Figure 5.

### 5.9 JTAG

The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory.

The JTAG chain structure is illustrated in Figure 6. Directly after reset, two TAP controllers are present in the JTAG chain for each XCore: the boundary scan TAP

**Figure 4:**  
Boot source pins

SS_XC0_BS[0]	Boot Mode		
0	Boot from SPI		
	Pin <sup>A</sup>	Signal	Description
	X0D00	MISO	Master In Slave Out
	X0D01	SS	Slave Select
	X0D10	SCLK	Clock
	X0D11	MOSI	Master Out Slave In
1	None: Device waits to be booted from JTAG		

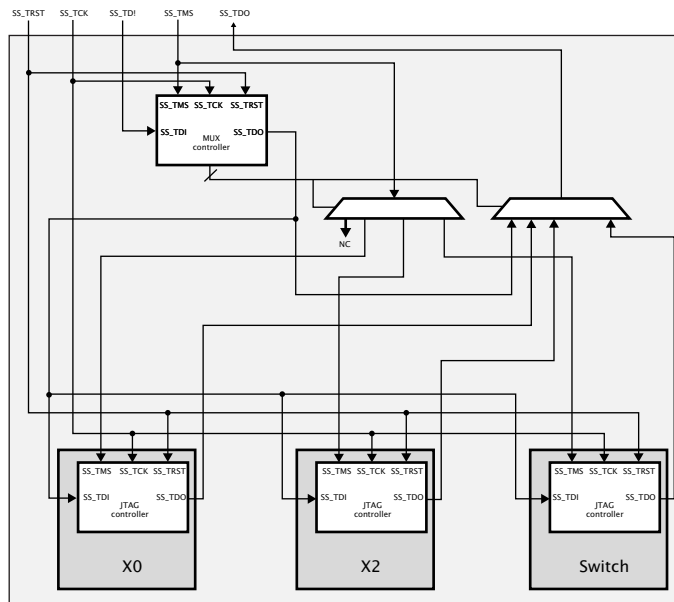
A The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. An SPI boot program can be burned into OTP and used at any time.

**Figure 5:**  
Boot mode indication pins

SS_XC0_BS[0]	Boot Confirmation
0	Booted from SPI
1	Booted from OTP or JTAG

and the chip TAP. The boundary scan TAP is a standard 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. The chip TAP provides access into the XCore, switch and OTP for loading code and debugging.

**Figure 6:**  
JTAG chain structure



The SS\_TRST pin must be asserted low during and after power up for 100 ns. If JTAG is not required, the SS\_TRST pin can be tied to ground with a 1k resistor to hold the JTAG module in reset.

The SS\_DEBUG pin is used to synchronize the debugging of multiple XCores. This pin can operate in both output and input mode. In output mode and when configured to do so, SS\_DEBUG is driven low by the device when the XCore processor hits a debug break point. Prior to this point the pin will be tri-stated. In input mode and when configured to do so, driving this pin low will put the XCore into debug mode. Software can set the behavior of the XCore based on this pin. This pin should have an external pull up of 4K7-47KΩ or left not connected in single core applications.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified in Figure 7.

**Figure 7:**  
IDCODE return value

Bit31		Device Identification Register																												Bit0						
Version				Part Number												Manufacturer Identity												1								
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	1
0				0				1				0				4				6				3				3								

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in Figure 8. The OTP User ID field is read from bits [22:31] of the security register on XCore 0 (all zero on unprogrammed devices).

**Figure 8:**  
USERCODE return value

Bit31		Usercode Register																												Bit0								
OTP User ID								Unused				Silicon Revision																										
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0								0				2				8								0								0						

### 5.10 Power Supplies

The device has the following types of power supply pins:

- VDD pins for the chip core
- IO VDD pins for the I/O lines
- SS\_PLL\_AVDD pins for the PLL
- SS\_OTP\_VPP pins for faster programming the OTP (optional)

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDD supply must ramp from 0V to its final value within 10ms to ensure correct startup.

The IO VDD supply must ramp to its final value before VDD reaches 0.4V.

The SS\_PLL\_AVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for

example, a  $4.7\Omega$  resistor and  $1\mu\text{F}$  multi-layer ceramic capacitor) is recommended on this pin.

The SS\_OTP\_VPP supply can be optionally provided for faster OTP programming times, otherwise an internal charge pump is used.

The following ground pins are provided:

- PLL\_AGND for PLL\_AVDD
- GND for all other supplies

All ground pins must be connected directly to the board ground.

The VDD and IO VDD supplies should be decoupled close to the chip by several  $100\text{ nF}$  low inductance multi-layer ceramic capacitors between the supplies and GND (for example,  $4 \times 100\text{ nF}$  0402 low inductance MLCCs per supply rail). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least  $10\mu\text{F}$  should be placed on each of these supplies.

SS\_RESET is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (see §5.8). SS\_RESET and must be asserted low during and after power up for  $100\text{ ns}$ .

## 6 DC and Switching Characteristics

### 6.1 Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD	Core DC supply voltage	0.95	1.00	1.05	V	
VDDIO	I/O DC supply voltage	3.00	3.30	3.60	V	
PLL_AVDD	PLL analog supply	0.95	1.00	1.05	V	
OTP_VPP	OTP external programming voltage (optional program only)	6.18	6.50	6.83	V	
CI	XCore I/O load capacitance			25	pF	
Ta	Ambient operating temperature (Commercial)	0		70	°C	
	Ambient operating temperature (Industrial)	-40		85	°C	
Tj	Junction temperature			125	°C	
Tstg	Storage temperature	-65		150	°C	

**Figure 9:**  
Operating conditions

### 6.2 DC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Input high voltage	2.00		5.50	V	A, B
V(IL)	Input low voltage	-0.30		0.80	V	A, B
V(OH)	Output high voltage	2.40			V	A, B
V(OL)	Output low voltage			0.40	V	A, B
R(PU)	Pull-up resistance		100K		Ω	A, C

**Figure 10:**  
DC characteristics

- A All pins except power supply pins.
- B Internal pull-up resistors are fitter to general-purpose I/O pins.
- C Use for unused I/O only. The internal pull-up resistor is not recommended as a substitute for an external pull-up resistor.

### 6.3 ESD Stress Voltage

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
HBM	Human body model	-2.00		2.00	KV	
MM	Machine model	-200		200	V	

**Figure 11:**  
ESD stress voltage



### 6.4 Reset Timing

**Figure 12:**  
Reset timing

Symbol	Parameters	MIN	TYP	MAX	UNITS	Notes
T(RST)	Reset pulse width	100			ns	
T(PLLLOCK)	PLL lock			1	ms	
T(INIT)	Initialization time			<100	µs	A

A Shows the time taken to start booting after SS\_RESET has gone high.

### 6.5 Quiescent Current

**Figure 13:**  
Quiescent current

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD current		120		mA	
I(PLLQ)	Quiescent PLL current		4		mA	

### 6.6 Power Consumption

**Figure 14:**  
Core currents

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
PD	Core power dissipation (Commercial)		0.86		Watts	A, B, C, D
	Core power dissipation (Industrial)		0.80		Watts	A, B, C, D

A Use for budgetary purposes only.

B Assumes typical core and I/O voltages operating at 400 MHz with nominal activity on all cores.

C PD(TYP) value is the usage power consumption under typical operating conditions.

D PD(TYP) value includes quiescent current.



The core power consumption of the device is highly application dependent and should be used for budgetary purposes only. More detailed power analysis can be found in the XS1-G Power Consumption document, document number [X1423](#).

### 6.7 Clock

**Figure 15:**  
Clock

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f	Frequency	12.5	20	20	MHz	
SR	Slew rate	1		2	ns	
f(MAX)	System clock frequency			400	MHz	

Further details can be found in the XS1-G Clock Frequency Control document, document number [X140](#).

### 6.8 XCore I/O AC Characteristics

**Figure 16:**  
I/O AC characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOVALID)	Input data valid window	8			ns	
T(XOINVALID)	Output data invalid window	9			ns	
T(XIFMAX)	Rate at which data can be sampled with respect to an external clock			60	MHz	

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, document number [X9122](#).

### 6.9 XMOS Link Performance

**Figure 17:**  
Link performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blinkP)	2b link bandwidth (packetized)			87	MBit/s	A, B
B(5blinkP)	5b link bandwidth (packetized)			217	MBit/s	A, B
B(2blinkS)	2b link bandwidth (streaming)			100	MBit/s	B
B(5blinkS)	5b link bandwidth (streaming)			250	MBit/s	B

A Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.

B 7.5 ns symbol time.

The asynchronous nature of links means that the relative phasing of SS\_CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

### 6.10 JTAG Timing

**Figure 18:**  
JTAG timing

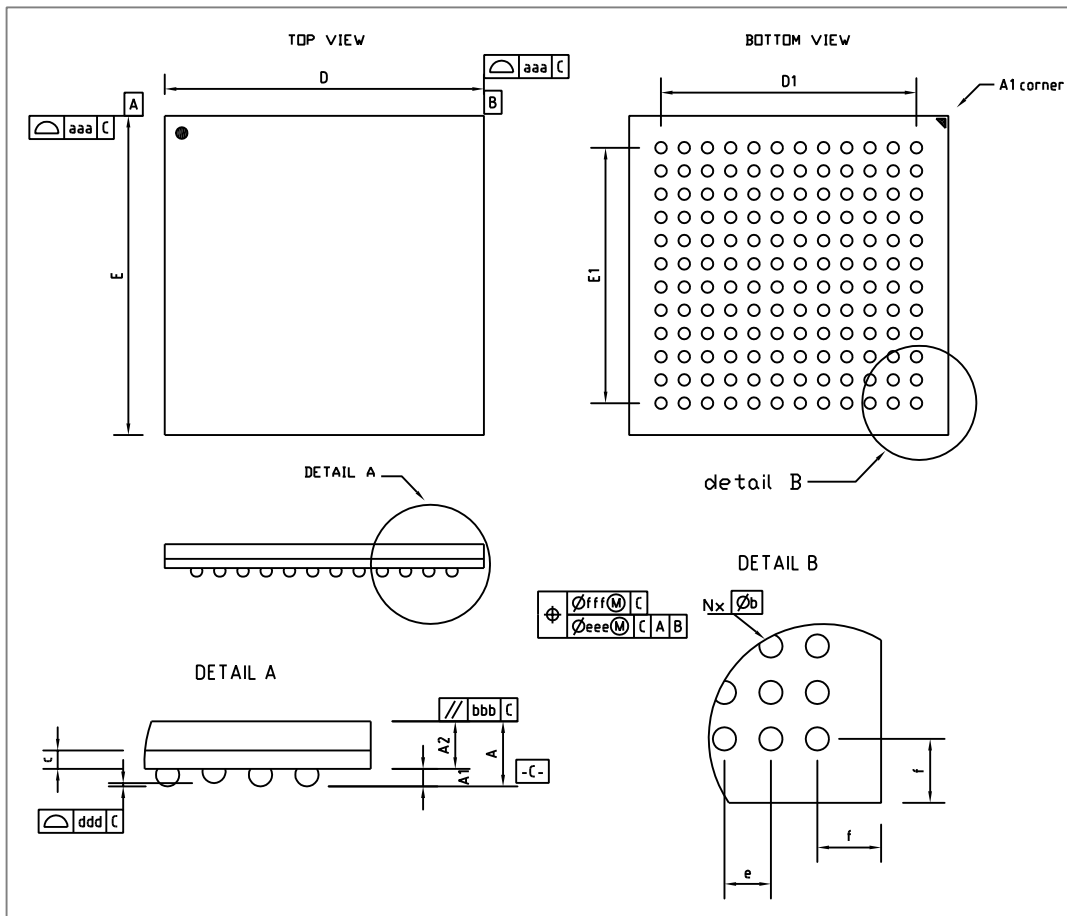
Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(TCK)	TCK period	30			ns	
T(SETUP)	TDO to TCK setup time	5			ns	A
T(HOLD)	TDO to TCK hold time			10	ns	A
T(DELAY)	TCK to output delay			15	ns	B

A Timing applies to SS\_TMS, SS\_TRST and SS\_TDI inputs.

B Timing applies to SS\_TDO output.

All JTAG operations are synchronous to SS\_TCK apart from the global asynchronous reset SS\_TRST.

### 7 Package Information



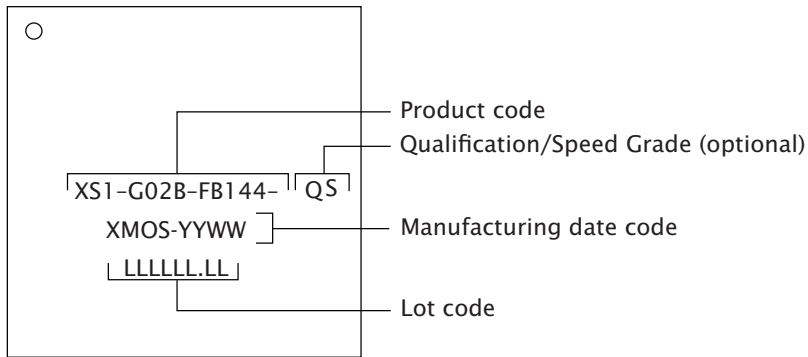
Dimensional Ref.			
REF	Min.	Nom.	Max.
A			1.7
A1	0.21		
A2		1.06	
D		11.0	
D1		8.8	
E		11.0	
E1		8.8	
b		0.4	
c	0.32	0.36	0.40
e		0.8	
f		1.1	
m		12	
n		14.4	

Dimensional Tol.	
aaa	0.15
bbb	0.20
ddd	0.10
eee	0.15
fff	0.08

**Notes**

- All dimensions in MM
- 'e' represents the basic solder ball pitch
- 'm' represents the basic solder ball matrix. And 'n' is the number of attached solder balls
- 'b' is measurable at the maximum solder ball diameter parallel the the primary datum -C-
- Dimension 'aaa' is measured parallel to primary datum -C-
- Primary datum -C- and the seating plane are defined by the spherical crowns of the solder balls
- The package surface shall be matte finish charmiltes 24 to 27
- The over package thickness 'A' already considers collapse balls
- Reference Jeduc Design Guide 4.5 and M0-275

### 7.1 Part Marking



**Figure 19:**  
Part marking scheme

## 8 Ordering Information

**Figure 20:**  
Orderable part numbers

Product Code	Qualification	Speed Grade
XS1-G02B-FB144-C4	Commercial	400 MHz
XS1-G02B-FB144-I4	Industrial	400 MHz

## 9 Development Tools

XMOS provides a comprehensive suite of development tools. Source files, timing scripts and a board design file are input to the compiler toolchain which produces a binary executable. This executable file can be simulated, loaded onto the device and debugged over JTAG, programmed into flash memory on the board or written to OTP memory on the device. The tools can also encrypt the flash image and write the decryption key securely to OTP memory.

The tools can be driven from either a graphical development environment or the command line and are supported on Windows, Linux and MacOS X. The tools are available at no cost from [xmos.com/tools](http://xmos.com/tools). Information on using the tools is provided in a separate user guide, document number [X1066](#).

## 10 Addendum: XMOS USB Interface

XMOS provides a low-level USB interface for connecting the device to a USB transceiver using the UTMI+ Low Pin Interface (ULPI). The ULPI signals must be connected to the pins named in [Figure 21](#). Note also that some ports on the same

core are used internally and are not available for use when the USB driver is active (they are available otherwise).

Pin	Signal	Pin	Signal	Pin	Signal
XnD02	Unavailable	XnD16	ULPI_DATA[2]	XnD30	Unavailable
XnD03		XnD17	ULPI_DATA[3]	XnD31	
XnD04		XnD18	ULPI_DATA[4]	XnD32	
XnD05		XnD19	ULPI_DATA[5]	XnD33	
XnD06		XnD20	ULPI_DATA[6]	XnD37	
XnD07		XnD21	ULPI_DATA[7]	XnD38	
XnD08		XnD22	ULPI_DIR	XnD39	
XnD09		XnD23	ULPI_CLK	XnD40	
XnD12		ULPI_STP	XnD26	Unavailable	
XnD13	ULPI_NXT	XnD27	XnD42		
XnD14	ULPI_DATA[0]	XnD28	XnD43		
XnD15	ULPI_DATA[1]	XnD29			

**Figure 21:**  
ULPI signals provided by the XMOS USB driver

## 11 Associated Design Documentation

Document Title	Information	Document Number
XS1-G Hardware Design Checklist	Board design checklist	<a href="#">X0124</a>
Device Package User Guide	Land pattern, solder paste, ground recommendations	<a href="#">X4979</a>
Estimating Power Consumption For XS1-G Devices	Power consumption	<a href="#">X1423</a>
Programming XC on XMOS Devices	Timers, ports, clocks, threads and channels	<a href="#">X1066</a>
XMOS Tools User Guide	Compilers, assembler and linker/mapper Timing analyzer and debugger Flash and OTP programming utilities	<a href="#">X1089</a>

- ▶ Example schematic diagrams detailing minimal system configurations are available from <http://www.xmos.com/support/silicon>.

## 12 Related Documentation

Document Title	Information	Document Number
The XMOS XS1 Architecture	ISA manual	<a href="#">X0102</a>
XS1 Port I/O Timing	Port timings	<a href="#">X9122</a>
XS1-G System Specification	Link, switch and system information	<a href="#">X2725</a>
XS1-G Link Performance and Design Guidelines	Link timings	<a href="#">X2215</a>
XS1-G Clock Frequency Control	Advanced clock control	<a href="#">X1340</a>

## 13 Revision History

The page numbers in this section refer to this document.

### Rev. 1100C-05/11

1. Revised format.
2. Standard XMOS Link format XnLn on page 4.

### Rev. 1100B-01/11

1. Replaced “Port Pin Table” with “Signal Description” on page 4.
2. Updated “ULPI” on page 20 with set of disabled signals.
3. Removed “Device Configuration”.
4. Added “Associated Design Documentation” on page 21.
5. Not recommended for new designs.
6. Clock frequencies of between 20 MHz and 25 MHz are **not** supported.
7. Removed documentation of numerous JTAG commands, which were incorrect.
8. Updated Figure 10 in “DC Characteristics” on page 15 by removing rows for I(OH) and I(OL).
9. Updated Figure 17 in “XMOS Link Performance” on page 17 by removing rows for B(2link) and B(5link), and adding rows for B(2linkP), B(5linkP), B(2linkS) and B(5linkS).
10. Renamed IO VSS signals to VSS.
11. Renamed DEBUG to DEBUG\_N.

### Rev. 1100A-06/10

1. Revised format.
2. Updated “Power Consumption” on page 16.



Copyright © 2010 XMOS Limited, All Rights Reserved.

---

XMOS Limited is the owner or licensee of this design, code, or Information (collectively, the “Information”) and is providing it to you “AS IS” with no warranty of any kind, express or implied and shall have no liability in relation to its use. XMOS Limited makes no representation that the Information, or any particular implementation thereof, is or will be free from any claims of infringement and again, shall have no liability in relation to any such claims.

XMOS and the XMOS logo are registered trademarks of XMOS Limited in the United Kingdom and other countries, and may not be used without written permission. All other trademarks are property of their respective owners. Where those designations appear in this book, and XMOS was aware of a trademark claim, the designations have been printed with initial capital letters or in all capitals.

---