



Device Overview

The IDT 89HP0504PB (P0504PB) is a 5Gbps PCIe® Repeater device featuring IDT EyeBoost™ technology that compensates for cable and board trace attenuations and ISI jitter, thereby extending connection reach. The device is optimized for PCIe Gen1 and Gen2 high speed serial data streams and contains four data channels, each able to process 5Gbps transmission rates. Each channel consists of an input equalizer and amplifier, signal detection with glitch filter, as well as programmable output swing and de-emphasis. Allowing for application specific optimization, the P0504PB, with its configurable receiver and transmitter features, is ideal for PCIe applications using a wide combination of cables and board trace materials.

All modes of active data transfer are designed with minimized power consumption. In full shutdown mode, the part consumes less than 40mW in worst case environmental conditions.

Applications

- ◆ Blade servers, rack servers
- ◆ PCIe instrumentation
- ◆ Storage systems
- ◆ Cabled PCIe devices

Features

- ◆ Compensates for cable and PCB trace attenuation and ISI jitter
- ◆ Programmable receiver equalization up to 24db
- ◆ Programmable transmitter swing and de-emphasis
- ◆ Recovers data stream even when the differential signal eye is completely closed due to trace attenuation and ISI jitter
- ◆ Full PCIe protocol support
- ◆ Configurable via external pins
- ◆ Leading edge power minimization in active and shutdown modes
- ◆ No external bias resistors or reference clocks required
- ◆ Channel mux mode, demux mode, 1 to 2 channels multicast, and Z-switch function mode
- ◆ Available in a 36-pin QFN package (4.0 x 7.5mm with 0.5mm pitch)

Benefits

- ◆ Extends maximum cable length to over 8 meters and trace length over 48 inches in PCIe applications
- ◆ Minimizes BER

Typical Application

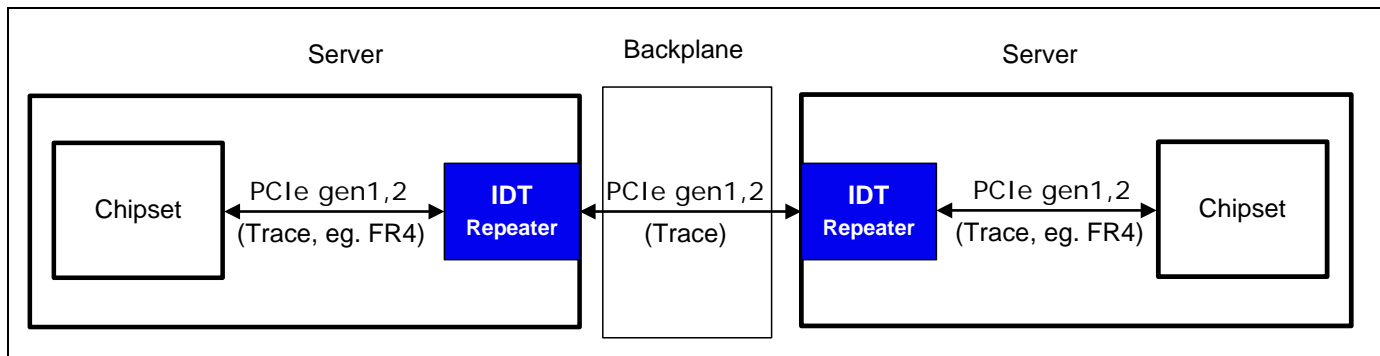


Figure 1 IDT Repeaters in Blade Servers

PCIe Compliance

The device was designed to provide end users with features needed to comply with PCIe system application requirements:

- Receiver Detection Support, PCIe Beacon Support
- Receiver supports high impedance mode for PCIe
- Jitter, eye opening, and all other key AC and DC specifications.

Block Diagram

The P0504PB contains four high speed channels as shown in Figure 2. Each channel can be routed to different outputs. Depending on user configuration via mode selections, input traffic can be muxed or demuxed. Powerdown (PDB) and Receiver Detection Reset (RSTB) are provided for state and channel control.

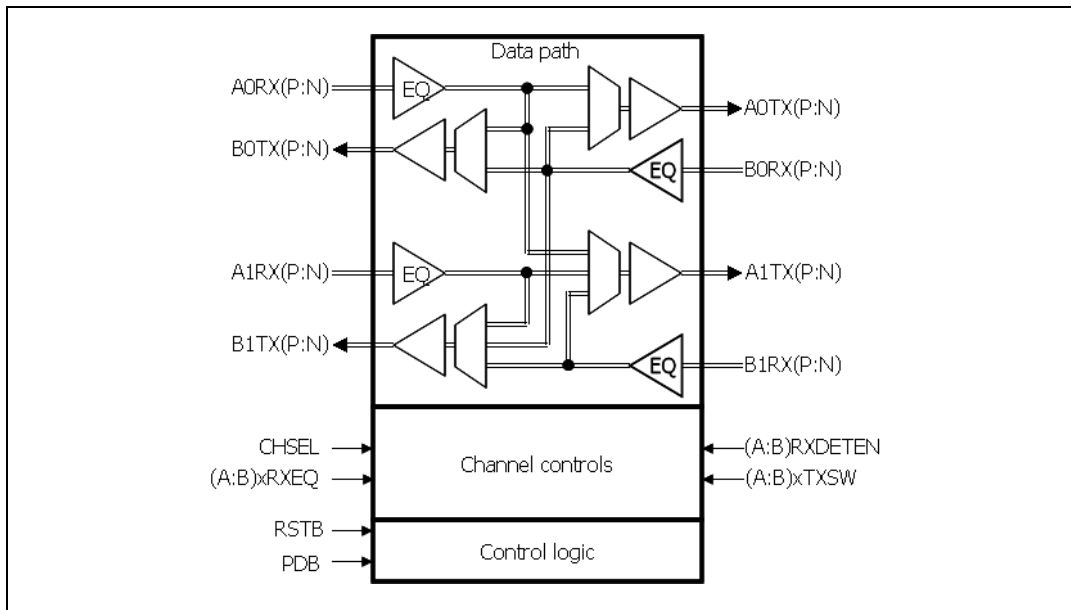


Figure 2 Block Diagram

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Functional Description

The P0504PB has 4 channels, each with the individually programmable features listed below. Figure 3 diagrams the channel and Table 1 summarizes key configuration options.

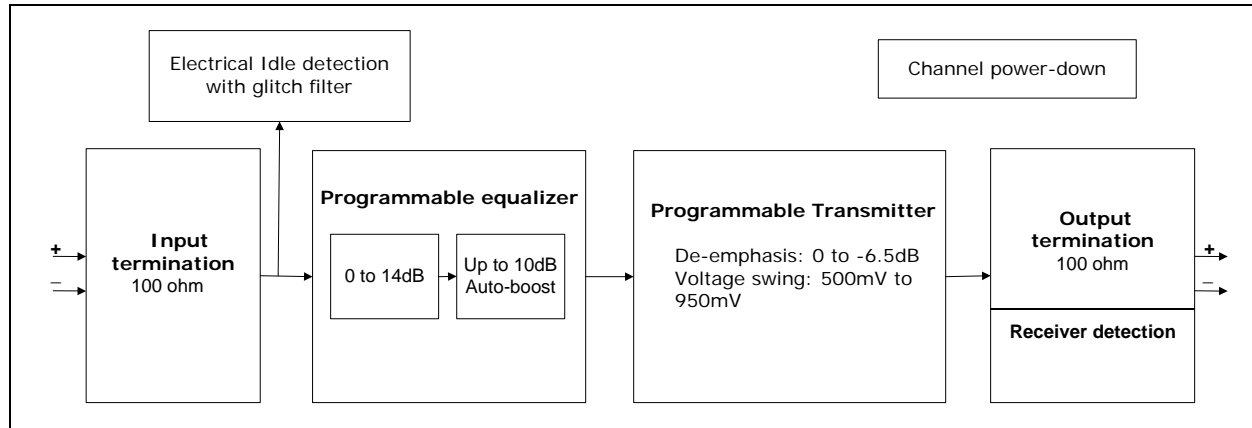


Figure 3 Channel Block Diagram with Channel Features

- ◆ Per-channel programmable features used at the Receive side.
 - Input equalization with 3 levels: 2 to 14dB compensation for high frequency signal attenuation due to cables and board traces. Additionally, up to 10dB boost is added automatically by the equalizer for applications using long cables. The total equalization range is between 2dB and 24dB.
 - Input high impedance control via channel enable: disabled (active mode) and hi-Z (power-down).
- ◆ Per-channel programmable features used at the Transmit side.
 - Output de-emphasis with 8 levels: 0 to -6.5dB. The de-emphasis boosts the magnitude of higher frequencies sent by the transmitter to compensate for high frequency losses travelling through output side cable or output side board traces. This ensures that the final received signal has a wider eye opening.
 - Output differential swing with 3 levels: 0.5V to 0.95V (peak-to-peak).
 - Receiver detection: enable or disable. This function is activated following an RSTB pulse.
 - With receiver detection enabled, if A0 and A1 channels do not detect at least one receiver, then the P0504PB on-chip Rx termination on A0 and A1 is set to hi-Z as shown in Table 2.
 - With receiver detection enabled, if B0 and B1 channels do not detect at least one receiver, then the P0504PB on-chip Rx termination on B0 and B1 is set to hi-Z as shown in Table 2.
 - Electrical idle detection: When the incoming differential peak-peak amplitude falls below 110mV, the device enters electrical idle mode and the corresponding transmitter stops toggling, maintains its common mode voltage level, and meets all electrical idle specifications described in the AC Specifications section of this data sheet.

In addition, the device contains global configuration of the data path:

- Transfer modes: direct connect, cross-connect, multicast.

Power-Up

After the power supplies reach their minimum required levels, the P0504PB powers up by setting all input and output pins to known states:

- ◆ All the device's input configuration pins are set internally to VSS or VDD for 2-level pins and to VDD/2 for 3-level pins.
- ◆ High speed differential input and output pins depend on various conditions described below:
 - High speed differential input and output pins are in high impedance if any of the following conditions is true:
 - Powerdown is set (PDB pin = 0V) or
 - No receiver termination was detected at TX outputs

In all other cases, high speed differential input and output pins are set to 50 ohms per pin, with 100 ohms differential impedance. Also refer to Table 4, Power Reducing Modes, Table 2, Receiver Impedance, and Table 3, Transmitter Impedance.

The power ramp up time for the P0504PB should be less than 1ms.

Power Sequencing

There are no power sequencing constraints for the P0504PB.

IDT EyeBoost™ Technology

IDT EyeBoost™ technology is a method of data stream recovery even when the differential signal eye is completely closed due to cable or trace attenuation and ISI jitter. With IDT EyeBoost™, the system designer can both recover the incoming data and retransmit it to target device with a maximized eye width and amplitude. An example of IDT EyeBoost™ technology usage in a system application and eye diagram results are shown in Figure 4. In this figure, the (a) diagram shows incoming differential signal (closed eye) after 62 inch FR4 connection from signal source and the (b) diagram shows differential signal at the output of repeater maximized eye opening with IDT EyeBoost™ technology.

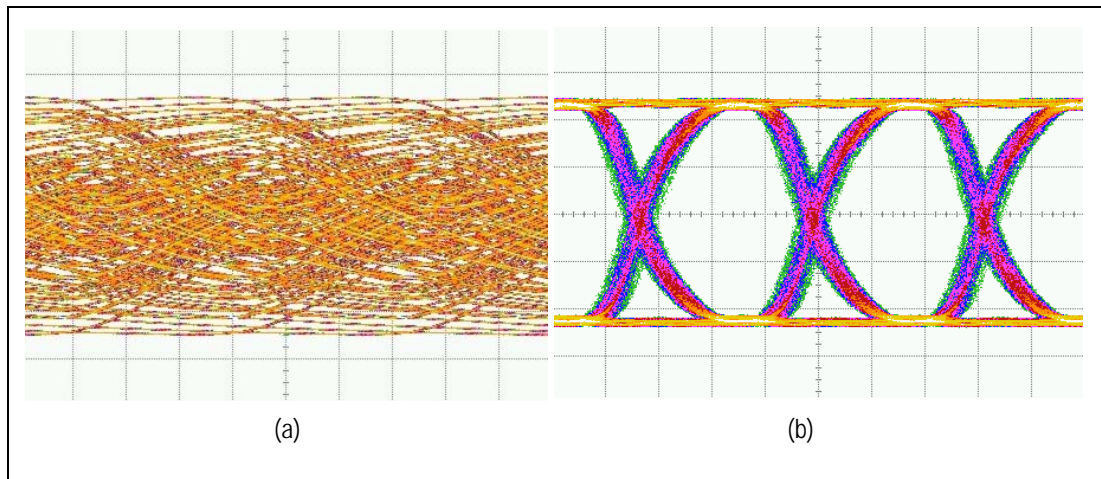


Figure 4 Eye Diagram

Eye Diagram Parameters

| Feature | Feature Type | Parameter Names for Programming via Pins |
|--|-----------------------|---|
| Input equalization | Main eye optimization | A0RXEQ, A1RXEQ, B0RXEQ, B1RXEQ Range: 0dB to 14dB (plus additional auto-boost up to 10dB for long connections) |
| Output differential signal swing (peak-to-peak) and output de-emphasis | Main eye optimization | A0TXSW, A1TXSW, B0TXSW, B1TXSW Range: 0.5V to 0.95V for swing Range: 0 to -6.5dB for de-emphasis |

Table 1 Quick Reference: Parameters Used for Eye Optimization

Receiver Impedance

The table below shows how the receiver impedance changes based on input and output pin states.

| Mode | Control Inputs | | | Rx Terminations | Description |
|--------------------|----------------|--------------|------|-----------------|---|
| | PDB | [A,B]RXDETEN | RSTB | | |
| Full IC Power-down | 0 | X | X | Hi-Z | Receiver terminations placed in Hi-Z. |
| Channel Enabled | 1 | 0 | 1 | 50Ω | Receiver detect disabled. Receiver terminations set to 50Ω. |
| Channel Enabled | 1 | 1 | 1 | 50Ω | Receiver detect enabled. Valid receiver detected. Receiver terminations set to 50Ω. |

Table 2 Receiver Impedance

Transmitter Impedance

The table below shows how the transmitter impedance changes based on input and output pin states.

| Mode | Control Inputs | | Tx Terminations | Description |
|--------------------|----------------|------|-----------------|--|
| | [A,B]RXDETEN | RSTB | | |
| Full IC Power-down | X | X | 1kΩ | Receiver terminations placed in Hi-Z. |
| Channel Enabled | 0 | 1 | 50Ω | Rx signal not detected. Receiver detect disabled. Receiver terminations set to Hi-Z. |

Table 3 Transmitter Impedance (Part 1 of 2)

| Mode | Control Inputs | | Tx Terminations | Description |
|------------------------------|----------------|------|-----------------|---|
| | [A,B]RXDETEN | RSTB | | |
| Channel Enabled | 0 | 1 | 50Ω | Rx signal detected. Receiver detect disabled. Receiver terminations set to 50Ω. |
| Channel Enabled but inactive | 1 | 1 | 50Ω | TX output is squelched. A valid receiver was detected. Receiver terminations set to 50Ω. Output common-mode is held at its active value. |
| Channel Enabled and active | 1 | 1 | 50Ω | TX output is active. A valid receiver was detected. Receiver terminations set to 50Ω. |

Table 3 Transmitter Impedance (Part 2 of 2)

PCIe Receiver Detection Support

The P0504PB transmitter fully supports PCIe Receiver Detection requirements. Receiver detection is enabled for channels A0 and A1 by asserting pin ARXDETEN and for channels B0 and B1 by asserting pin BRXDETEN. For receiver detection to occur, a low pulse (minimum 200ns) must be applied at pin RSTB. The rising edge of the RSTB signal starts the receiver detection procedure. Neither ARXDETEN nor BRXDETEN can be toggled during the receiver detection procedure, i.e., they must be kept high for at least 200ns before the RSTB rising edge and they cannot go to low sooner than 2ms from the time the RSTB goes high. The receiver detection takes place once per RSTB pulse.

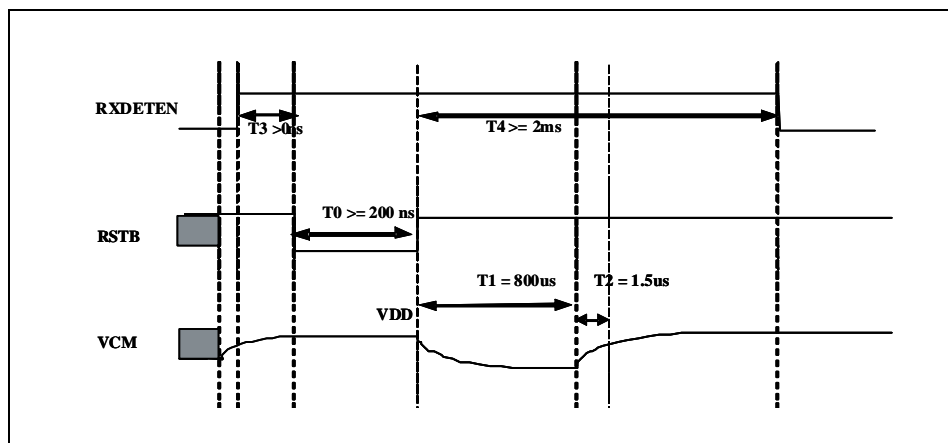


Figure 5 Receiver Detection Timing

Modes of Operation

The device supports several data transfer modes, electrical idle mode, and several power reducing modes.

Electrical Idle Mode

In electrical idle mode, the transmitter stops toggling and maintains its common-mode voltage level. The device enters electrical idle mode when the envelope of the incoming signal on a given channel has fallen below a programmable threshold level.

Power Reducing Modes

The Repeater supports five power-down states and one active state as shown in Table 4. The user can choose between full chip power-down, channel based power-down, and electrical idle modes. Power reducing modes can be selected via PDB and RSTB.

| Power Reducing Mode | Required Signal Values | | State Description |
|---|------------------------|-----------------------|---|
| | Power-Down Control | Receiver Detect Start | |
| | PDB | RSTB | |
| Full IC power-down | 0 | X | All channels are powered-down Receiver detect reset Rx termination is set to Hi-Z Tx termination is set to 1k Ω Tx common-mode is at VDD |
| Receiver Detect reset | 1 | 0 | Receiver detect state machine Receiver terminations placed in Hi-Z Tx termination is set to 1k Ω Tx common-mode is at VDD |
| Channel enabled but inactive (electrical idle). Rx and Tx set to hi-Z | 1 | 1 | Tx output is squelched No receiver was Detected Receiver terminations placed in Hi-Z Tx termination is set to 1k Ω Tx common-mode is at VDD |
| Channel enabled but inactive (electrical idle). Rx and Tx set to 50 Ohms | 1 | 1 | Tx output is squelched A valid receiver was detected Receiver terminations set to 50 Ω Output common-mode is held at its active value Tx termination is set to 50 Ω |
| Channel enabled and active. No power-down | 1 | 1 | Tx output is active A valid receiver was detected Receiver terminations set to 50 Ω Transmitter terminations set to 50 Ω |

Table 4 Power Reducing Modes

Channel Muxing

The P0504PB repeater permits a variety of muxing, demuxing, and switching configurations, and it can mux/de-mux 1 or 2 bi-directional PCIe lanes (4 PCIe channels) into 2 target devices. These configurations require the selection of specific pins for input and output ports. In the following sections, each configuration is described in terms of pin connectivity to external upstream and downstream devices. The configurations shown are those often used in system designs:

- Uni-directional 2:1 Mux (1 or 2 instances)
- Uni-directional 1:2 De-Mux (1 or 2 instances)
- Bi-directional 2:1 Mux/De-Mux
- Bi-directional Z-function (also called Partial Cross Function)

The P0504PB supports channel muxing in both upstream and downstream channel directions via the CHSEL pin, as shown below. Figure 6 shows the channel/reference muxing modes and Table 5 shows how CHSEL (Channel transfer selection) pin allows for various modes of data transfers: Multicast mode, Direct-connect, and Cross-connect. Both Direct-connect, and Cross-connect modes are used to build uni-directional and bi-directional 2:1 mux and Z-switch functions.

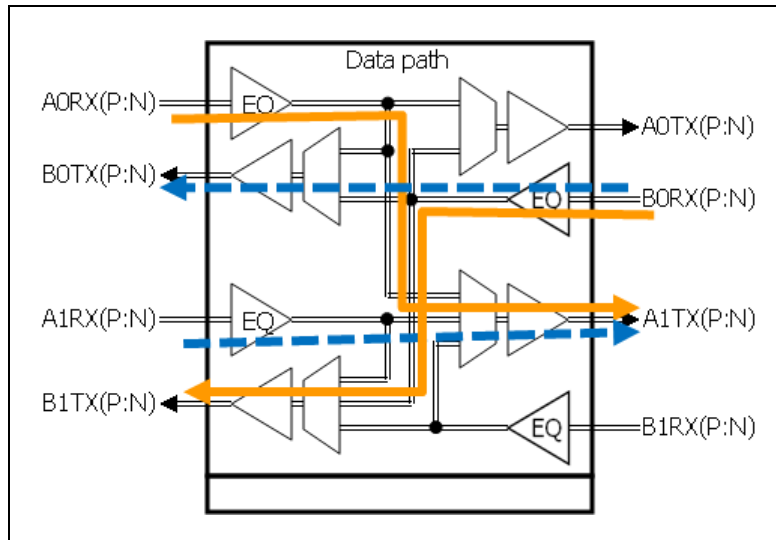


Figure 6 Diagram of Channel/Reference Muxing Modes

| Input Pins | | | | | Output Pins | | | |
|-------------------------------------|-----------|-----------|-----------|-----------|-------------|-----------|-----------|-----------|
| CHSEL | A0RX[P,N] | A1RX[P,N] | B0RX[P,N] | B1RX[P,N] | A0TX[P,N] | A1TX[P,N] | B0TX[P,N] | B1TX[P,N] |
| CHSEL=VSS (Multicast Mode) | A0 DATA | X | B0 DATA | X | A0 DATA | A0 DATA | B0 DATA | B0 DATA |
| CHSEL=Open (Direct-Connect Mode) | A0 DATA | A1 DATA | B0 DATA | B1 DATA | A0 DATA | A1 DATA | B0 DATA | B1 DATA |
| CHSEL=VDD (Cross-Connect Mode) | A0 DATA | X | B0 DATA | X | Squelched | A0 DATA | Squelched | B0 DATA |

Table 5 Description of Channel Muxing/De-Muxing Functionality

Uni-directional 2:1 Mux or Two Instances of Unidirectional 2:1 Mux

This function can be achieved by using the CHSEL pin as a mux control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 7.

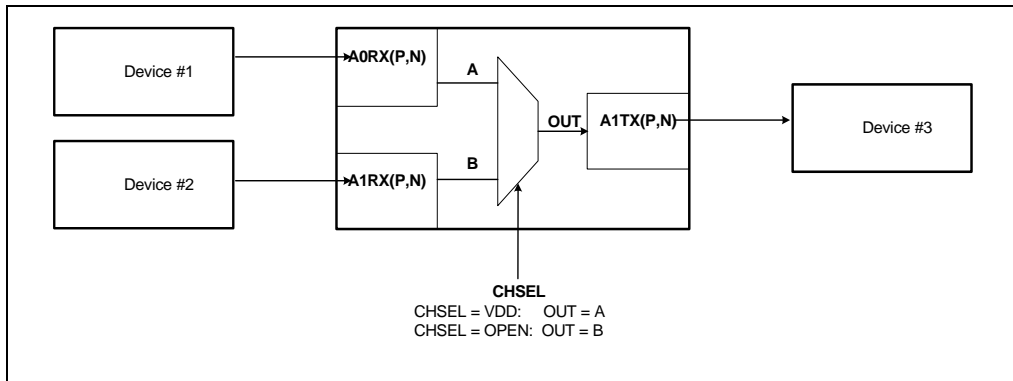


Figure 7 Implementation of Unidirectional 2:1 Mux

As an alternative, different chip channels can also be selected as shown in Figure 8. This solution can be combined with the previous one to obtain two instances of Uni-directional 2:1 Mux.

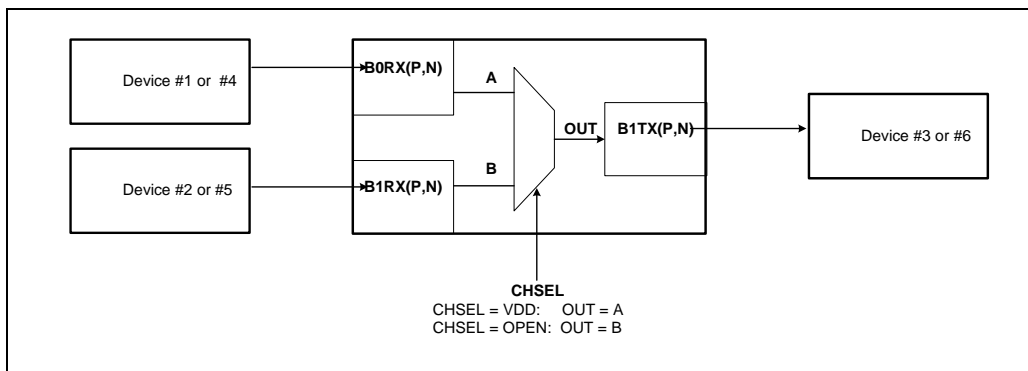


Figure 8 Implementation of Second Instance of Unidirectional 2:1 Mux

Uni-directional 1:2 De-Mux or Two Instances of Unidirectional 1:2 De-Mux

This function can be achieved by using CHSEL pin as a de-mux control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 9.

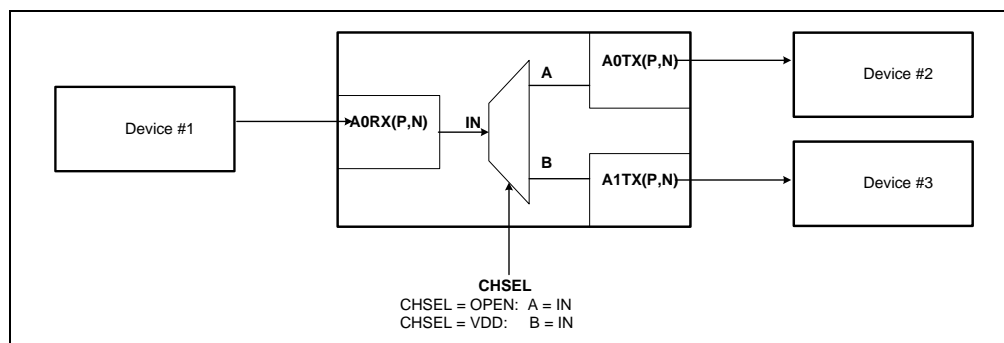


Figure 9 Implementation of Unidirectional 1:2 De-Mux

As an alternative, different chip channels can also be selected as shown in Figure 10. This solution can be combined with the previous one to obtain two instances of Uni-directional 1:2 De-Mux.

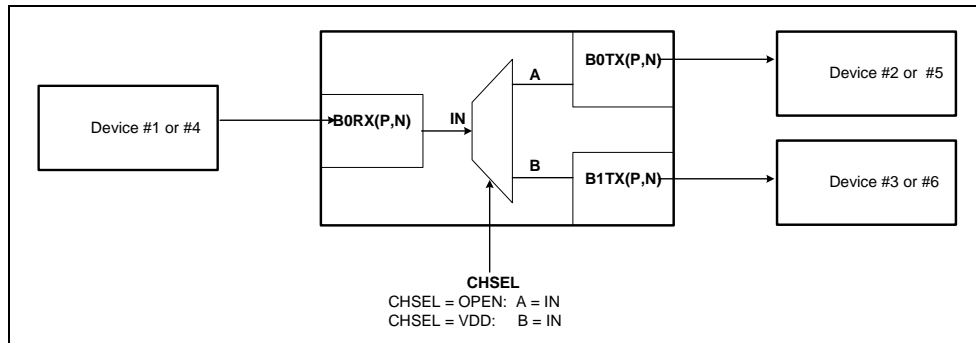


Figure 10 Implementation of Second Instance of Unidirectional 1:2 De-Mux

Bi-directional 2:1 Mux/De-Mux

The bi-directional Mux and De-Mux function can also be achieved by using the CHSEL pin as a mux control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 11.

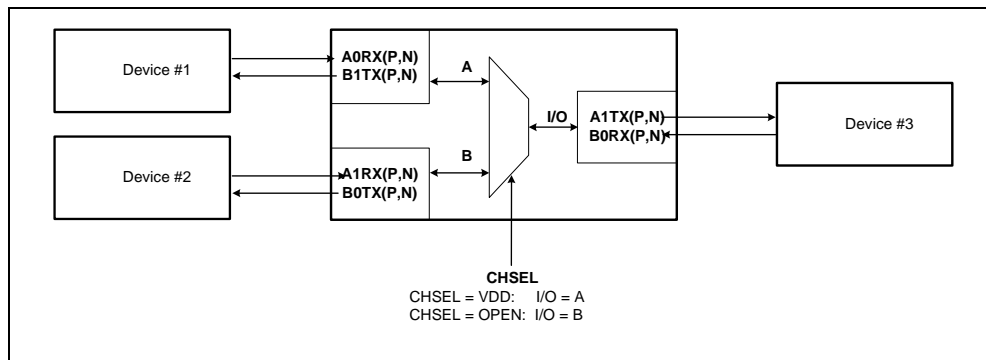


Figure 11 Implementation of Bi-directional 2:1 Mux/De-Mux

Bi-directional Z-function (also called Partial Cross Function)

This function can also be achieved by using the CHSEL pin as a flow control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 12.

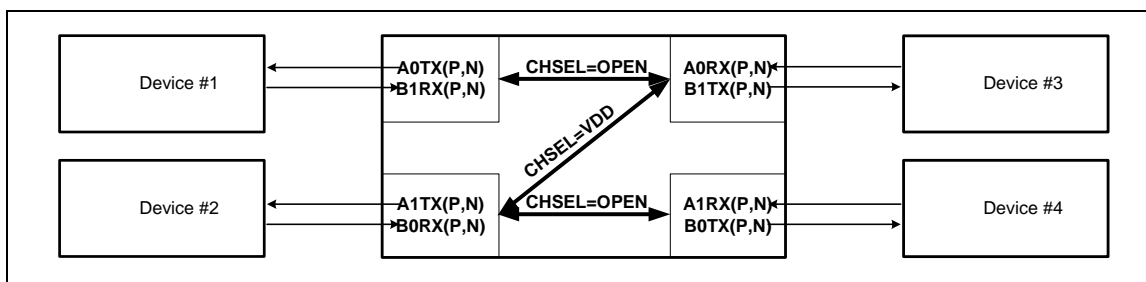


Figure 12 Implementation of Z-function

Electrical Specifications

Absolute Maximum Ratings

Note: All voltage values, except differential voltages, are measured with respect to ground pins.

| Parameter | Value | Unit |
|---|-------------------|------|
| Supply voltage range VDD | -0.5 to 1.35 | V |
| Voltage range Differential I/O | -0.5 to VDD +0.5 | V |
| Control I/O | -0.5 to VDD + 0.5 | V |
| ESD requirements: Electrostatic discharge Human body model | ±2000 | V |
| ESD requirements: Charged-Device Model (CDM) | ±500 | V |
| ESD requirements: Machine model | ±125 | V |
| Storage ambient temperature | -55 to 150 | °C |

Table 6 Absolute Maximum Ratings

Warning: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

| Parameter | Notes | Min | Typical | Max | Unit |
|--------------------------------------|--|------|---------|------|------|
| Power Supply Pin Requirements | | | | | |
| VDD | 1.2V DC analog supply voltage (specified at bump pins) | 1.14 | 1.2 | 1.26 | V |
| Temperature Requirements | | | | | |
| TA | Ambient operating temperature - Commercial | 0 | — | 70 | °C |
| | Ambient operating temperature - Industrial | -40 | — | 85 | °C |
| TJUNCTION | Junction operating temperature | 0 | — | 125 | °C |

Table 7 Operating Conditions

Power Consumption

Table 8 below lists power consumption values under typical and maximum operating conditions.

| Parameter | Notes | Min | Typical | Max | Unit |
|---------------------|--------------------------------|-----|---------|-----|------|
| Active Mode | | | | | |
| I_{VDD} | Current into VDD supply | — | 330 | 500 | mA |
| P_D | Full chip power ¹ | | 400 | 600 | mW |
| P_{D-ch} | Power per channel ¹ | | 100 | 150 | mW |
| Standby Mode | | | 30 | 40 | mW |

Table 8 Power Consumption

¹ Maximum power under all conditions. Power is reduced by selecting smaller de-emphasis settings (closer or equal to 0dB).

Package Thermal Considerations

The data in Table 9 below contains information that is relevant to the thermal performance of the 36-pin QFN package.

| Parameter | Description | Value | Conditions | Units |
|--------------------------|---|-------|---------------------------------------|-------|
| $T_{J(max)}$ | Junction Temperature | 125 | Maximum | °C |
| $T_{A(max)}$ | Ambient Temperature | 70 | Maximum for commercial-rated products | °C |
| | | 85 | Maximum for industrial-rated products | °C |
| $\theta_{JA(effective)}$ | Effective Thermal Resistance, Junction-to-Ambient | 41.8 | Zero air flow | °C/W |
| | | 36.1 | 1 m/S air flow | °C/W |
| | | 35.3 | 2 m/S air flow | °C/W |
| | | 34.3 | 3 m/S air flow | °C/W |
| | | 33.7 | 4 m/S air flow | °C/W |
| | | 33.2 | 5 m/S air flow | °C/W |
| θ_{JB} | Thermal Resistance, Junction-to-Board | 14.5 | NA | °C/W |
| θ_{JC} | Thermal Resistance, Junction-to-Case | 37.2 | NA | °C/W |

Table 9 Thermal Specifications for P0504PB, 4.0x7.5mm 36-QFN Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 9. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 9), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board).

DC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|--------------------|---|---------------------------|-----|---------------------------|---------|
| V_{IL} | Digital Input Signal Voltage Low Level ¹ | -0.3 | — | $0.25 \cdot V_{DD} - 0.1$ | V |
| V_{IM} | Digital Input Signal Voltage Mid Level ² | $0.25 \cdot V_{DD} + 0.1$ | | $0.75 \cdot V_{DD} - 0.1$ | V |
| V_{IH} | Digital Input Signal Voltage High Level ¹ | $0.75 \cdot V_{DD} + 0.1$ | | $V_{DD} + 0.3$ | V |
| V_{HYS} | Hysteresis of Schmitt Trigger Input | 0.1 | | — | V |
| I_{IL} | Input Current ³ | — | | 100 | μA |
| I_{IH} | Input Current ⁴ | — | | 100 | μA |
| I_{IL1} | Input Current ² | — | | 180 | μA |
| I_{IH1} | Input Current ² | — | | 180 | μA |
| $R_{WEAK_PD_2L}$ | Internal weak pull-down resistor at 2-level input pads ⁴ | 11 | | — | K ohm |
| $R_{WEAK_PU_2L}$ | Internal weak pull-up resistor at 2-level input pads ³ | 11 | | — | K ohm |
| $R_{WEAK_PD_3L}$ | Internal weak pull-down resistor at all 3-level input pads | 6.3 | | — | K ohm |
| $R_{WEAK_PU_3L}$ | Internal weak pull-up resistor at all 3-level input pads | 6.3 | | — | K ohm |

Table 10 DC Specification

¹ Applies to all input pins.

² Applies to all 3-level input pins.

³ Applies only to 2-level input pins with default values set to VDD in the Pin Description table (Table 14).

⁴ Applies only to 2-level input pins with default values set to VSS in the Pin Description table (Table 14).

AC Specifications

Latency Specification

| Parameter | Description | Min | Typical | Max | Unit |
|-----------|---|-----|---------|-----|------|
| Latency | Input to output signal propagation device | — | 300 | — | ps |

Table 11 Latency Specification

Receiver Specifications

| Parameter | Description | Min | Typical | Max | Unit |
|---|---|------|---------|------|------|
| Receiver Input Jitter Specifications | | | | | |
| T _{RX-DDJ} | Receive Input Signal Data Dependent Jitter (Inter-Symbol Interference). | — | — | >1 | UI |
| T _{RX-TJ} | Receive Input Signal Total Jitter | — | — | >1 | UI |
| T _{RX-EYE} | Receiver eye time opening (can recover from closed eye due to trace attenuation and ISI jitter) | 0 | — | — | UI |
| Receiver Input Eye Specification | | | | | |
| V _{RX-DIFF-PP-DC} | Receiver Differential Peak-Peak Voltage ¹ | 0 | — | 2000 | mV |
| V _{RX-CM-DC} | Receiver DC Common Mode Voltage | — | 0 | — | mV |
| V _{RX-CM-AC-P} | Receiver AC Common Mode Voltage | — | — | 150 | mV |
| Receiver Return Loss | | | | | |
| RL _{RX-DIFF-F1} | Receiver Differential Return Loss (0 - 1.25GHz) | — | — | -10 | dB |
| RL _{RX-DIFF-F2} | Receiver Differential Return Loss (1.25 - 2.5GHz) | — | — | -8 | dB |
| RL _{RX-CM} | Receiver Common-Mode DC Return Loss | — | — | -6 | dB |
| Receiver DC Impedance | | | | | |
| Z _{RX-DC} | Receive Impedance (singled-ended) | 40 | 50 | 60 | Ohm |
| Z _{RX-DIFF-DC} | DC differential impedance | 80 | 100 | 120 | Ohm |
| Z _{RX-HIGH-IMP-DC-POS} | DC Input Common-Mode Receive High Impedance for Input Voltage from 0V to 200mV | 50k | — | — | Ohm |
| Z _{RX-HIGH-IMP-DC-NEG} | DC Input Common-Mode Receive High Impedance for Input Voltage from 0V to -200mV | 1k | — | — | Ohm |
| Z _{DIFF-HIZ-POS} | Differential Receive High Impedance for Input Voltage from 0V to 200mV | 200k | — | — | Ohm |
| Z _{DIFF-HIZ-NEG} | Differential Receive High Impedance for Input Voltage from 0V to -200mV | 4k | — | — | Ohm |
| Receiver Signal Detection | | | | | |
| V _{RX-IDLE-DET-DIFF-p-p} | Electrical Idle Signal Detect Threshold | 70 | 110 | 150 | mV |
| T _{RX-IDLE-DET-DIFF-ENTER-TIME} | Unexpected Electrical Idle Enter Detect Threshold Integration Time | — | — | 10 | ms |
| T _{SIGDET-ATTACK} | Signal Detect Valid Signal Attack Time (Turn-on time) | — | — | 15 | ns |
| T _{SIGDET-DECAY} | Signal Detect Valid Signal Decay Time (Turn-off time) | — | — | 15 | ns |
| T _{SIGDET-ATT-DECAY-MIS} | Signal Detect Attack / Decay Time Mismatch | — | — | 5 | ns |

Table 12 Receiver Electrical Specifications

¹: The minimum value of 0 mV represents the case when Eye is completely closed.

Transmitter Specifications

| Parameter | Description | Min | Typical | Max | Unit |
|--|---|------------|------------|-------------|------|
| Output Eye and Common Voltage Specification | | | | | |
| $V_{TX-DIFF-PP}$ | Differential Transmitter swing [A:B]xTXSW=1 [A:B]xTXSW=open | 800 700 | 950 800 | 1100 950 | mV |
| $V_{TX-DIFF-PP-LOW}$ | Low power differential p-p Transmitter swing [A:B]xTXSW=0 | 400 | 500 | 650 | mV |
| $D_{TX-DEEMP}$ | Output De-emphasis. Defined as $20\log(V_{TX-DE-EMP} / V_{TX-DIFF})$ [dB] | -6.5 | — | 0 | dB |
| $V_{TX-DE-RATIO-3.5dB}$ | Tx de-emphasis level ratio [A:B]xTXSW=open | -4.0 | — | -3.0 | dB |
| $V_{TX-DE-RATIO-6dB}$ | Tx de-emphasis level [A:B]xTXSW=1 | -6.5 | — | -5.5 | dB |
| $T_{TX-RISE-FALL}$ | Rise/Fall Time | 0.125 | — | — | UI |
| $T_{RF-MISMATCH}$ | Tx rise/fall mismatch | — | — | 0.1 | UI |
| $T_{RES-DJ-5GBPS-1}$ | Residual Deterministic Jitter at output pins (1 inch FR4 trace before receiver input pins, 5Gbps) ¹ | — | — | <0.1 | UI |
| $T_{RES-DJ-5GBPS-2}$ | Residual Deterministic Jitter at output pins (40 inch FR4 trace before receiver input pins, 5Gbps) ¹ | — | 0.15 | 0.2 | UI |
| $V_{TX-CM-AC-PP}$ | Pk-Pk AC Common Mode Voltage Variation | — | — | 50 | mV |
| $V_{TX-CM-AC-P}$ | Tx AC common mode voltage (2.5 GT/s) | — | — | 20 | mV |
| $V_{TX-CM-RMS-AC}$ | RMS AC Common Mode Voltage Variation | — | — | 20 | mV |
| $V_{TX-DC-CM}$ | Transmitter DC common-mode voltage | 0 | — | VDD | V |
| $V_{TX-CM-DC-LINEDELTA}$ | Absolute Delta of DC Common Mode Voltage between P and N | 0 | — | 25 | mV |
| C_{TX} | AC Coupling Capacitor | 75 | — | 200 | nF |
| Transmitter DC Impedance | | | | | |
| $Z_{TX-DIFF-DC}$ | Transmitter Output Differential DC Impedance ² | 80 | 100 | 120 | Ohm |
| $I_{TX-SHORT}$ | Transmitter short-circuit current limit | — | — | 90 | mA |
| Transmitter Return Loss | | | | | |
| $RL_{TX-DIFF-F1}$ | Transmitter Differential Return Loss (0 - 1.25GHz) | — | — | -10 | dB |
| $RL_{TX-DIFF-F2}$ | Transmitter Differential Return Loss (1.25 - 2.5GHz) | — | — | -8 | dB |
| RL_{TX-CM} | Transmitter Common-Mode DC Return Loss | — | — | -6 | dB |
| Electrical Idle | | | | | |
| $V_{TX-IDLE}$ | Idle Output Voltage | — | — | 20 | mV |
| $V_{CM-DELTA-SQUELCH}$ | Maximum Common-Mode Step Entering/Exiting Electrical Idle Mode | — | — | 50 | mV |

Table 13 Transmitter Electrical Requirements (Part 1 of 2)

| Parameter | Description | Min | Typical | Max | Unit |
|---------------------------------|---|-----|---------|-----|---------|
| $V_{TX-CM-DC-ACTIVEIDLE-DELTA}$ | Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle. | 0 | — | 100 | mV |
| $V_{TX-IDLE-DIFF-AC-p}$ | Electrical Idle Differential Peak Output Voltage | 0 | — | 20 | mV |
| $V_{TX-IDLE-DIFF-DC}$ | DC Electrical Idle Differential Output Voltage | 0 | — | 5 | mV |
| Lane Skew | | | | | |
| $L_{TX-SKEW}$ | Lane-to-Lane Output Skew | — | 5 | 10 | ps |
| Receiver Detect | | | | | |
| $V_{TX-RCV-DETECT}$ | Voltage change allowed during receiver detection | — | — | 600 | mV |
| T0 | RSTB negative pulse width | 200 | — | — | ns |
| T1 | VCM pulsing (ramp up) | — | 800 | — | μ s |
| T2 | VCM pulsing (ramp down) | — | 1.5 | — | μ s |
| T3 | Time from RXDETEN high to RSTB pulse | 0 | — | — | ns |

Table 13 Transmitter Electrical Requirements (Part 2 of 2)

¹ Refer to Figure 13.

² When TERM_CTL bit is set to 100 Ω .

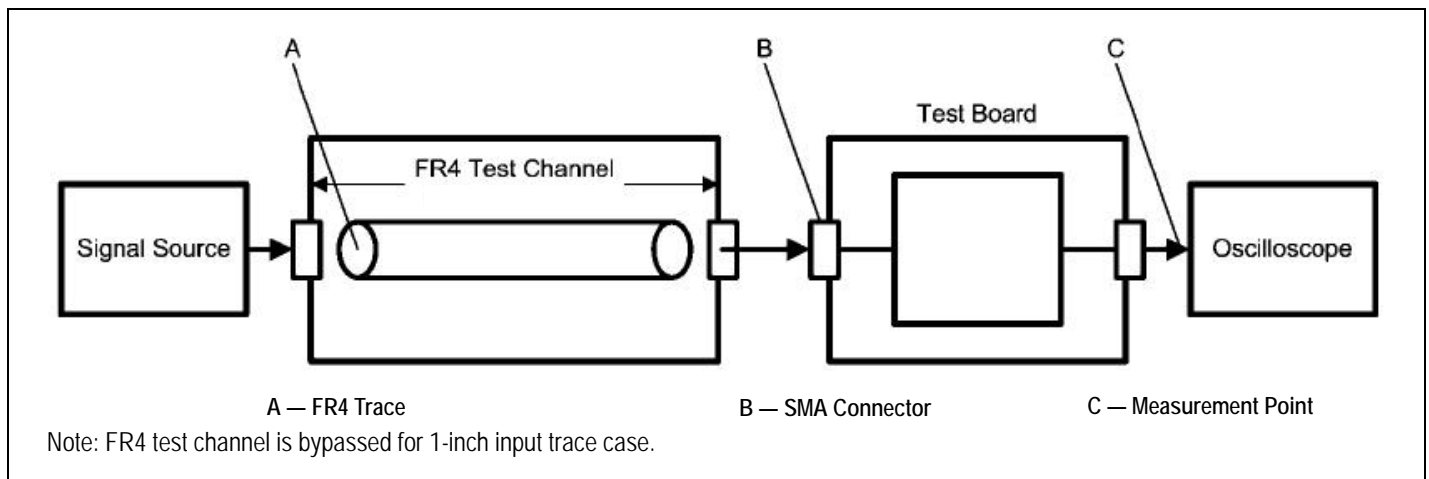


Figure 13 Residual Jitter Characterization Test Setup

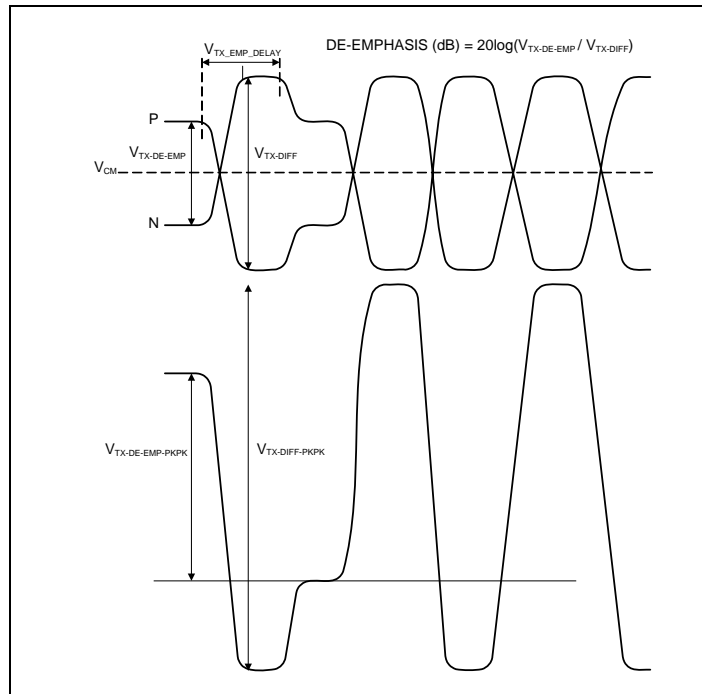


Figure 14 Transmitter Swing Levels With and Without De-emphasis

Note: $V_{TX-DIFF-PKPK}$ Peak to Peak voltage is twice as large as voltage difference between P pins and N pins of differential pairs. For example, if the P pin swings from 0.8V to 1.4V while the N pin swings from 1.4V to 0.8V, then: $V_{TX-DIFF-PKPK} = 2*(1.4-0.8)=1.2V$.

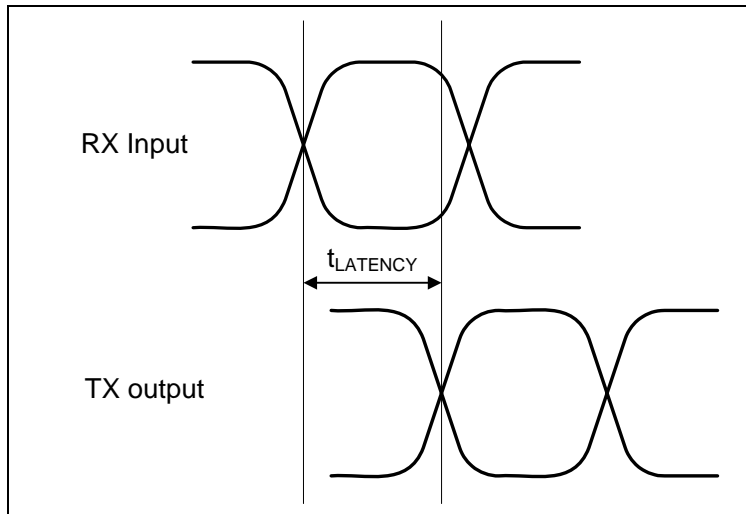


Figure 15 Definition of Latency Timing

Pin Description

Note: Unused pins can be left floating.

| Pin Name | Pin # | Description | Input/ Output/ Power 2 or 3 Level |
|--|----------------------|---|---|
| Power | | | |
| VDD | 5, 8, 11, 21, 24, 27 | 1.2V (typ) Power supply for Repeater high speed channels and internal logic. Each VDD pin should be connected to the VDD plane through a low inductance path, with a via located as close as possible to the landing pad of VDD pins. It is recommended to have a 0.01 μ F or 0.1 μ F, X7R, size-0402 bypass capacitor from each VDD pin to ground plane. | Power |
| VSS | Center Pad | VSS reference. VSS should be connected to the ground plane through a low inductance path, with a via located as close as possible to the landing pad. | Power |
| Data Signals | | | |
| AORXN AORXP | 4 3 | Channel A0 Receive Data Ports | Input |
| AOTXN AOTXP | 28 29 | Channel A0 Transmit Data Ports | Output |
| BORXN BORXP | 25 26 | Channel B0 Receive Data Ports | Input |
| BOTXN BOTXP | 7 6 | Channel B0 Transmit Data Ports | Output |
| A1RXN A1RXP | 10 9 | Channel A1 Receive Data Ports | Input |
| A1TXN A1TXP | 22 23 | Channel A1 Transmit Data Ports | Output |
| B1RXN B1RXP | 19 20 | Channel B1 Receive Data Ports | Input |
| B1TXN B1TXP | 13 12 | Channel B1 Transmit Data Ports | Output |
| Channel Control and Status | | | |
| A0RXEQ (Channel A0) B0RXEQ (Channel B0) A1RXEQ (Channel A1) B1RXEQ (Channel B1) | 15 17 36 33 | Receiver Equalization. Programming of channel A0 via pins is shown below. To program other channels, use pins for those channels. <u>A0RXEQ</u> <u>Setting</u> VSS 2dB Open 6dB (Default) VDD 14dB | Input - 3 level |

Table 14 Pin Description (Part 1 of 2)

| Pin Name | Pin # | Description | Input/ Output/ Power 2 or 3 Level |
|--|---------------------|--|---|
| A0TXSW (Channel A0) B0TXSW (Channel B0) A1TXSW (Channel A1) B1TXSW (Channel B1) | 1 32 14 18 | Transmitter Voltage Swing (pk-pk). Programming of channel A0 via pins is shown below. To program other channels, use pins for those channels. <u>A0TXSW</u> <u>Swing</u> <u>De-Emphasis</u> VSS 0.5Vdiff-pkpk 0dB Open 0.8Vdiff-pkpk (Default) -3.5dB VDD 0.95Vdiff-pkpk -6.5dB | Input - 3 level |
| Other Control Signals | | | |
| PDB | 35 | Power-down Enable. <u>PDB</u> <u>Setting</u> VSS Powerdown IC. RX terminations are in Hi-Z, TX is disabled VDD Normal operation (internal 11K ohm minimum pull-up applied) | Input - 2 level |
| RSTB | 34 | Receiver Detection Start. <u>RSTB</u> <u>Setting</u> VSS Resets Channel Receiver Detection State Machine VDD Normal operation (internal 11K ohm minimum pull-up applied) Note: the rising edge of RSTB will start the receiver detection. | Input - 2 level |
| ARXDETEN BRXDETEN | 16 31 | Output Channel Receiver Detect Enable Input. Programming of channel ARXDETEN via pins is shown below. To program BRXDETEN, use pins for that channel. <u>ARXDETEN</u> <u>Setting</u> VSS Receiver Detection is disabled for A0 and A1 channels (internal 11K ohm minimum pull-down applied) VDD Receiver Detection is enabled for A0 and A1 channels | Input - 2 level |
| CHSEL | 30 | Channel Transfer Mode. <u>CHSEL</u> <u>Setting</u> VSS Multi-cast mode Open Direct-connect mode (default) VDD Cross-connect mode | Input - 3 level |
| RSVD | 2 | Reserved. Do not connect. | |

Table 14 Pin Description (Part 2 of 2)

Package Pinout — 36-QFN Signal Pinout

Table 15 lists the pin numbers and signal names for the P0504PB device.

| Function | Pin | Function | Pin | Function | Pin |
|----------|-----|----------|-----|----------|-----|
| A0RXEQ | 15 | ARXDETEN | 16 | B1TXSW | 18 |
| A0RXN | 4 | B0RXEQ | 17 | BRXDETEN | 31 |
| A0RXP | 3 | B0RXN | 25 | CHSEL | 30 |
| A0TXN | 28 | B0RXP | 26 | PDB | 35 |
| A0TXP | 29 | B0TXN | 7 | RSTB | 34 |
| A0TXSW | 1 | B0TXP | 6 | RSVD | 2 |
| A1RXEQ | 36 | B0TXSW | 32 | VDD | 5 |
| A1RXN | 10 | B1RXEQ | 33 | VDD | 8 |
| A1RXP | 9 | B1RXN | 19 | VDD | 11 |
| A1TXN | 22 | B1RXP | 20 | VDD | 21 |
| A1TXP | 23 | B1TXN | 13 | VDD | 24 |
| A1TXSW | 14 | B1TXP | 12 | VDD | 27 |

Table 15 Alphabetical Pin List

Pin Diagram

The following figure lists the pin numbers and the signal names for the 36-QFN package.

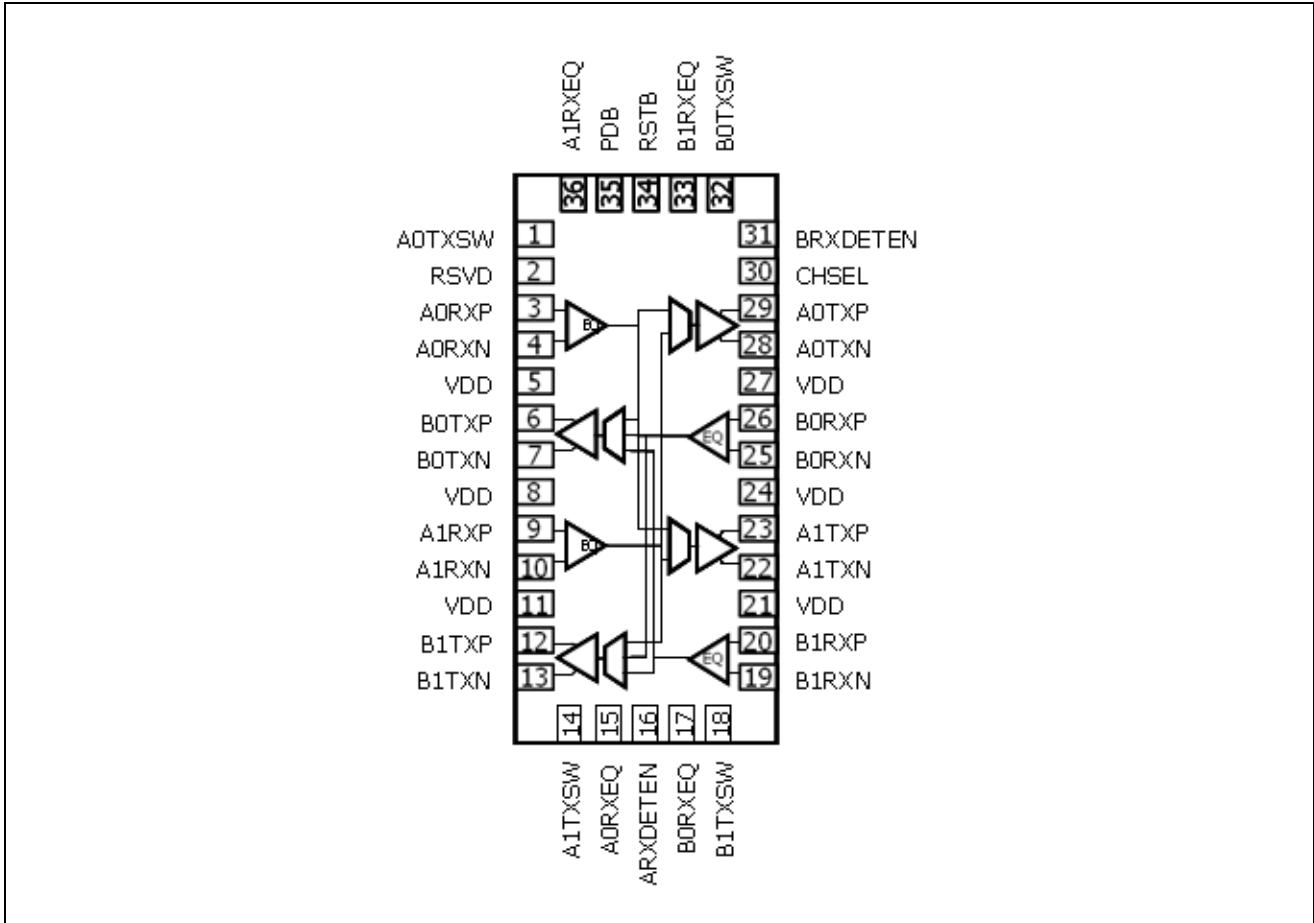
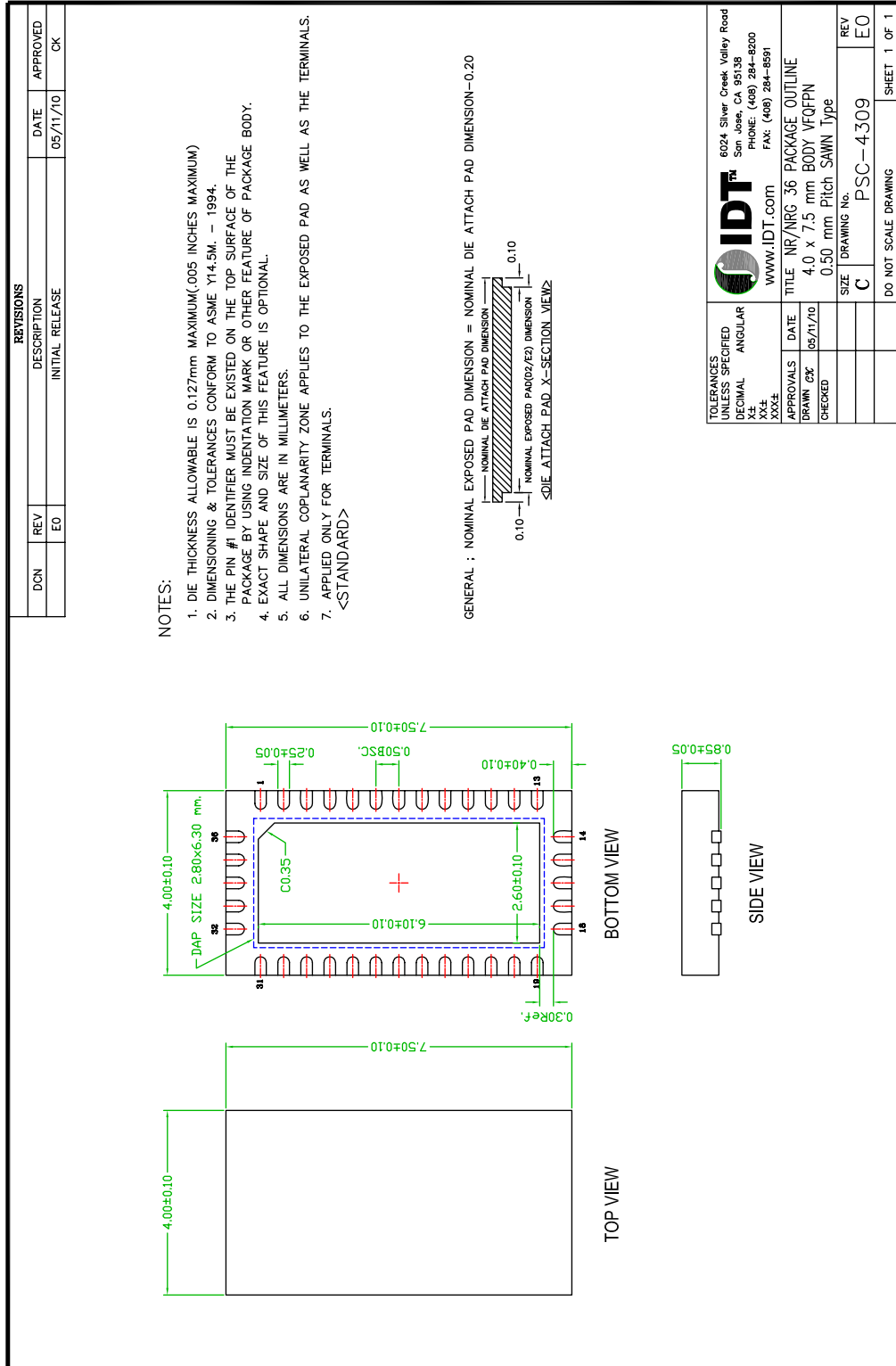


Figure 16 Pin Diagram — Top View

QFN Package Dimension



TOLERANCES UNLESS SPECIFIED

| | |
|---------|---------|
| DECIMAL | ANGULAR |
| XXX± | XXX± |
| XXXX± | XXXX± |

APPROVALS **DATE**

DRAWN CFC 05/11/10

CHECKED

TITLE NR/NRG_36 PACKAGE OUTLINE

SIZE 4.0 x 7.5 mm BODY VFQFPN

REV 0.50 mm Pitch SAWN Type

DRAWING No. PSC-4309

REV E0

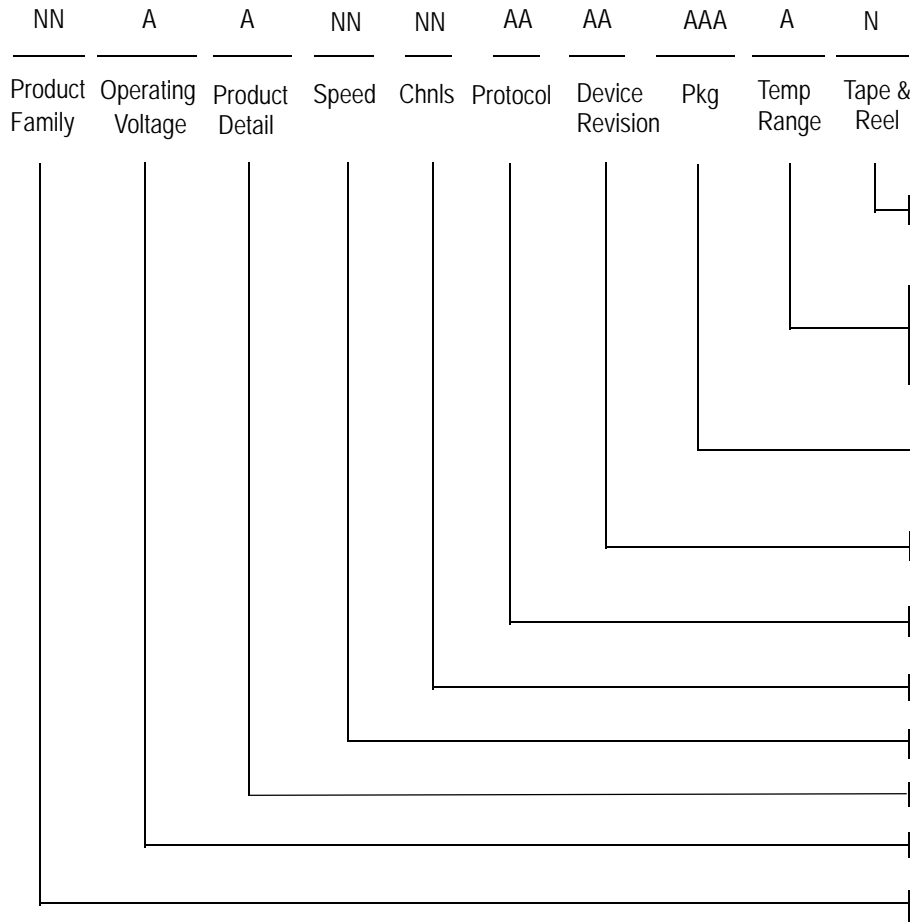
DO NOT SCALE DRAWING SHEET 1 OF 1

Revision History

November 2, 2010: Initial publication of final datasheet.

February 8, 2011: Removed black packaging options from Order page.

Ordering Information



Legend

A = Alpha Character
 N = Numeric Character

- 8 Tape & Reel
- Blank Commercial Temperature (0°C to +70°C Ambient)
- I Industrial Temperature (-40° C to +85° C Ambient)
- NRG NRG36 36-pin QFN, Green
- ZB ZB revision
- PB PCIe Interface, "B" version
- 04 4 Channels
- 05 5Gbps
- P rePeater
- H 1.2V +/- 5%
- 89 Signal Integrity Product

Valid Combinations

- 89HP0504PBZBNRG / 89HP0504PBZBNRG8 36-pin Green QFN package, Commercial Temperature
- 89HP0504PBZBNRGI / 89HP0504PBZBNRGI8 36-pin Green QFN package, Industrial Temperature



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