FAIRCHILD
SEMICONDUCTOR TM

May 1998

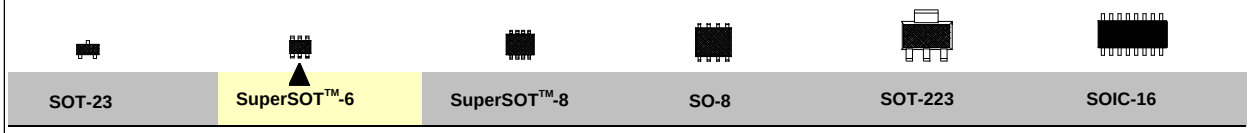
# FDC636P
# P-Channel Logic Level Enhancement Mode Field Effect Transistor

## General Description

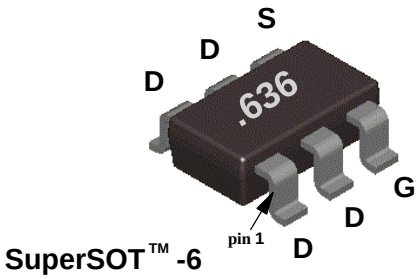
These P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

## Features

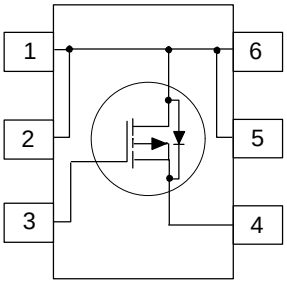
- -2.8 A, -20 V. $R_{DS(ON)}$ = 0.130 Ω @ $V_{GS}$ = -4.5 V
  $R_{DS(ON)}$ = 0.180 Ω @ $V_{GS}$ = -2.5 V.
- SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16




SuperSOT™ -6




**Absolute Maximum Ratings** $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | FDC636P | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | -20 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±8 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | -2.8 | A |
| | - Pulsed | | -11 | |
| $P_D$ | Maximum Power Dissipation | (Note 1a) | 1.6 | W |
| | | (Note 1b) | 0.8 | |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | | -55 to 150 | °C |
| **THERMAL CHARACTERISTICS** | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 78 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 30 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = -250 µA | -20 | | | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D$ = -250 µA, Referenced to 25 °C | | -22 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -16 V, $V_{GS}$ = 0 V | | | -1 | µA |
| | | $T_J$ = 55°C | | | -10 | µA |
| $I_{GSSF}$ | Gate - Body Leakage, Forward | $V_{GS}$ = 8 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate - Body Leakage, Reverse | $V_{GS}$ = -8 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 µA | -0.4 | -0.6 | -1 | V |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold VoltageTemp.Coefficient | $I_D$ = -250 µA, Referenced to 25 °C | | 2 | | mV/°C |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = -4.5 V, $I_D$ = -2.8 A | | 0.11 | 0.13 | Ω |
| | | $T_J$ = 125°C | | 0.17 | 0.21 | |
| | | $V_{GS}$ = -2.5 V, $I_D$ = -2.2 A | | 0.146 | 0.18 | |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = -4.5 V, $V_{DS}$ = -5 V | -11 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = -5 V, $I_D$ = -2.8 A | | 4 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = -10 V, $V_{GS}$ = 0 V, | | 390 | | pF |
| $C_{oss}$ | Output Capacitance | f = 1.0 MHz | | 170 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 45 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DD}$ = -10 V, $I_D$ = -1 A, | | 30 | 48 | ns |
| $t_r$ | Turn - On Rise Time | $V_{GS}$ = -4.5 V, $R_{GEN}$ = 6 Ω | | 26 | 42 | ns |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 8 | 16 | ns |
| $t_f$ | Turn - Off Fall Time | | | 15 | 27 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = -5 V, $I_D$ = -2.8 A, | | 6 | 8.5 | nC |
| $Q_{gs}$ | Gate-Source Charge | $V_{GS}$ = -4.5 V | | 0.9 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 1 | | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $I_S$ | Continuous Source Diode Current | | | | -1.3 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = -1.3 A (Note 2) | | -0.77 | -1.2 | V |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

   a. 78°C/W when mounted on a 1 $in^2$ pad of 2oz Cu on FR-4 board.

   b. 156°C/W when mounted on a minimum pad of 2oz Cu on FR-4 board.

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

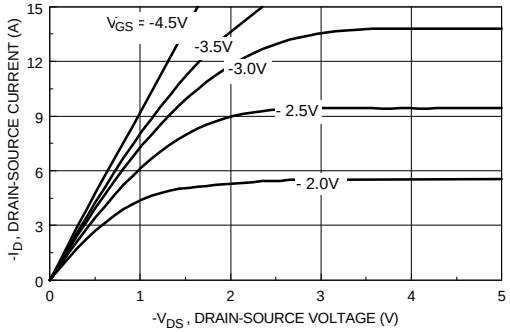



**Figure 1. On-Region Characteristics.**

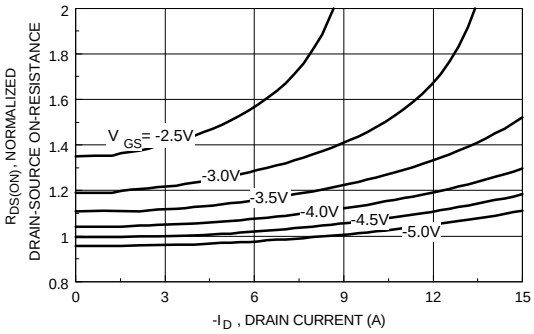



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

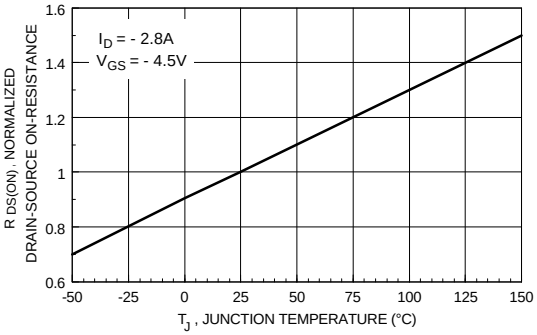



**Figure 3. On-Resistance Variation with Temperature.**

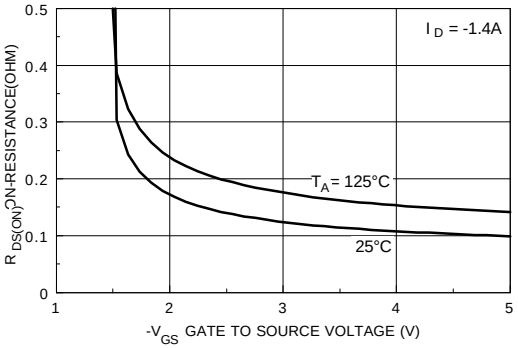



**Figure 4. On-Resistance Variation with Gate-To-Source Voltage.**

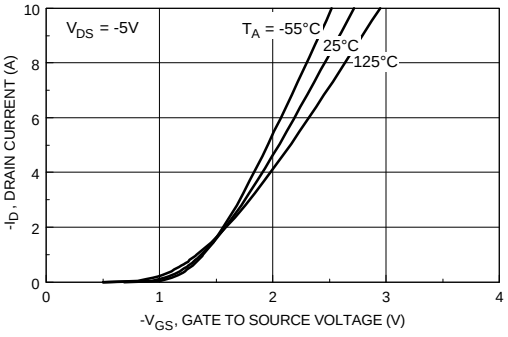



**Figure 5. Transfer Characteristics.**

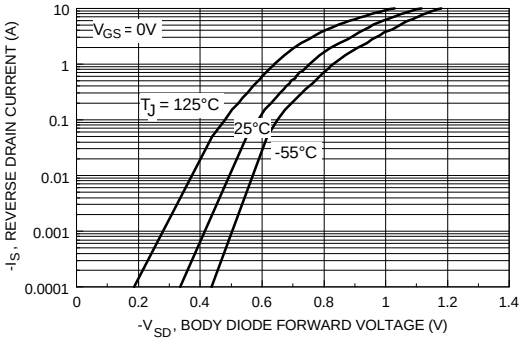



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Electrical Characteristics (continued)

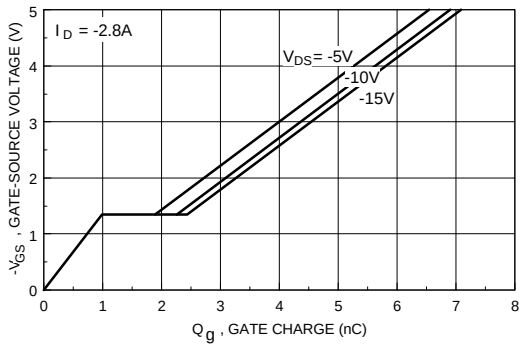



**Figure 7. Gate Charge Characteristics.**

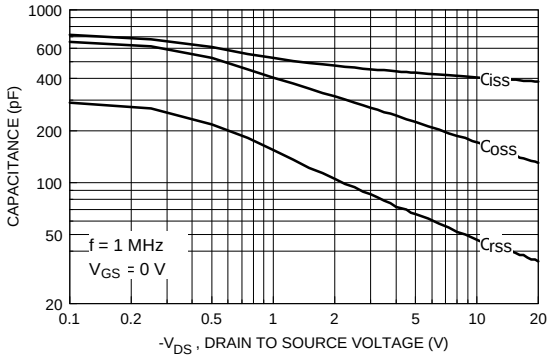



**Figure 8. Capacitance Characteristics.**

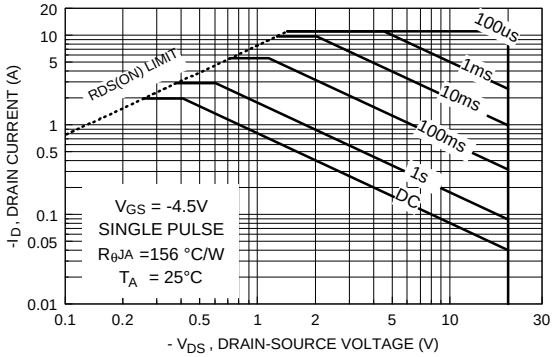



**Figure 9. Maximum Safe Operating Area.**

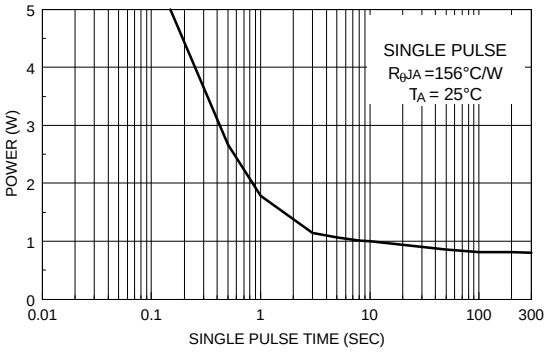



**Figure 10. Single Pulse Maximum Power Dissipation.**

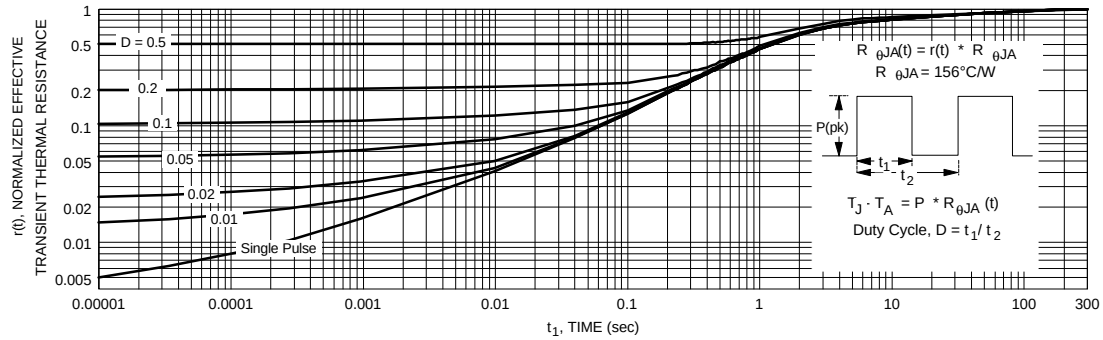



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in note 1b.
Transient thermal response will change depending on the circuit board design.