i.MX23 EVK Hardware

User's Guide

Document Number: 924-76384
Rev. 1.1
05/2010

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About This Book

This document explains how to connect and operate Revision B of the i.MX23 EVK.

Audience

This document is intended for software, hardware, and system engineers who are planning to use the product and for anyone who wants to understand more about the product.

Organization

This document contains the following chapters.

Chapter 1 Introduces the features and functionality of the EVK.

Chapter 2 Provides configuration and setup information.

Chapter 3 Provides functional operations and memory mapping.

Chapter 4 Provides connector pin information.

Conventions

This document uses the following conventions:

`Courier`	Is used to identify commands, explicit command parameters, code examples, expressions, data types, and directives.
Italic	Is used for emphasis, to identify new terms, and for replaceable command parameters.

Definitions, Acronyms, and Abbreviations

The following list defines the abbreviations used in this document.

AUART	Application Universal Asynchronous Receiver/Transmitter
CD	Compact Disk
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Custom Programmed Logic Devices
CPU	Central Processing Unit
DCE	Data Communications Equipment
DDR	Double Data Rate
DIP	Dual In-line Package
DMA	Direct Memory Access
DTE	Data Terminal Equipment
DUART	Debug Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory

GPIO	General Purpose Input/Output
GPO	General Purpose Output
I2C	Inter-Integrated Circuit
ICE	In-Circuit Emulator
I/O	Input/Output
IrDA	Infrared Data Association
ISA	Instrumentation, System, and Automation Society
JTAG	Joint Test Access Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MB	Megabyte
MCU	Microcontroller Unit
MMC	Multi-media Card
MCP	Multi-chip product
MS	Memory Stick
NVRAM	Non-volatile Random Access Memory
OTG	On the Go
PC	Personal Computer
PCMCIA	Personal Computer Memory Card International Association
PCB	Printed Circuit Board
PHY	Physical interface
POR	Power on Reset
PSRAM	Pseudo Random Access Memory
PWM	Pulse Width Modulation
QVGA	Quarter Video Graphics Array
RAM	Random Access Memory
SD	Secure Digital (Smart Media)
SDRAM	Synchronous Dynamic Random Access Memory
SI	System International (international system of units and measures)
SIMM	Single In-Line Memory Module
SPI	Serial Peripheral Interface
SPST	Single Pole Single Throw
SSI2	Synchronous Serial Interface
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WQVGA	Wide Quarter Video Graphics Array

Chapter 1
Introduction

The i.MX23 EVK helps you to develop multimedia communication applications using the i.MX23 ARM-9 CPU.

The EVK is a stand alone board that supports application software development, target board debugging, and optional circuit cards. A 4.3 inch LCD touch screen display panel is an optional accessory for use with the EVK.

Figure 1-1 shows the EVK with the optional LCD Daughter Card.

Figure1-1 EVK System with optional LCD

1.1 Features

The i.MX23 EVK provides in a reduced size form factor with the most common functions expected to be used by customers. Some features can be enabled by populating the EVK with additional components. Because the i.MX23 is a highly capable IC, not all features can be provided in a compact design. If there are required features not available on the i.MX23 EVK platform, contact your Freescale customer representative for other options.

The i.MX23 EVK platform includes the following features.

- 128 MB DDR1 SDRAM (with optional power saving mode)
- 1 GB NAND Flash (Can support 4 chip enable 48-TSOP NAND and ONFI packages)
- SD/MMC Card Socket
- Micro USB connector (OTG Host capability optional)
- 3.5mm stereo line-in and Headphone out jacks
- Ethernet Connector
- Debug UART
- 2 Application UARTs (one populated by default, one optional)
- LCD Connector
- 6 User Interface buttons, 3 Functional buttons
- 3-Axis Accelerometer
- JTAG connector with integrated parallel-to-serial converter
- Power supply jack to provide simulated battery power and power to support functions.
- Connectors for Li-ION Battery attachment.
- On-board microphone
- External Speaker connector pins
- Expansion Port Connector (optional)
- SPI Flash and EEPROM (optional)
- Composite Video Out (optional)
- Ability to select different Boot Mode options
- Near form-factor layout.
- Solid reference schematics that closely resemble final products to aid customers' designs.
- Utilizes reliable high-density connector to interface between boards.

Figure 1-2 illustrates the general locations of the EVK functionality.

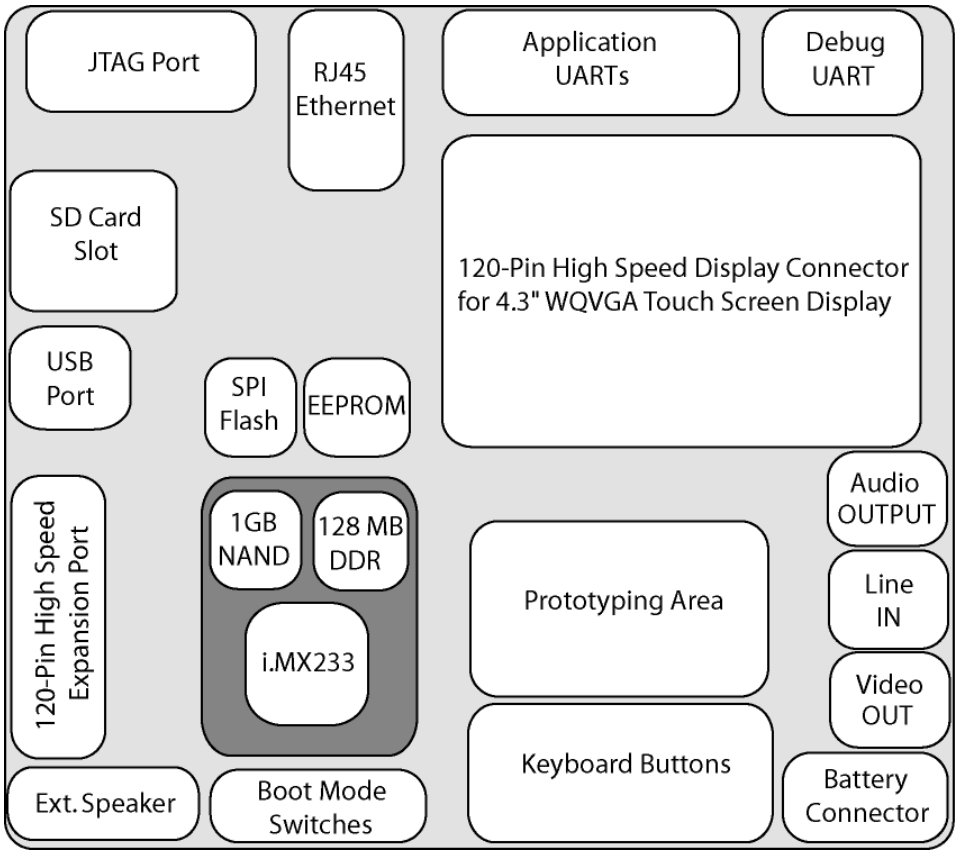

Figure1-2 EVK Functionality

1.2 Components

Table 1.1 describes the i.MX23 EVK board components.

Table 1.1 Board Components

Item	Description
DDR1 memory	128MB of 16 bit DDR memory from two chips.
Debug support	Proprietary Parallel-to-Serial JTAG converter, supports commercially available JTAG software up to 1MHz operations.
Flash memory, NAND	1 GB of MLC NAND Flash Memory
Jacks and speaker terminals	Headphone jack, line in jack, and external mono speaker terminals.
Microphone	Omni-Directional Condenser Microphone
Network connector	Ethernet network connector driven by external SPI Ethernet IC. Shares data lines with SD/MMC card connector through a buffer.

Power supply	+5.0 VDC, 3 A universal power supply
Reset	Push button reset forces i.MX23 CPU to shutdown. Must be restarted manually.
SD/MMC card connector	Card sense functionality.
USB Connector	One USB fast-speed Micro-AB connector. Host Mode (OTG) option requires stuffing additional components
WQVGA LCD Connector	4.3 inch WVGA display panel connector with touch panel as optional LCD (not included)

1.3 System and User Requirements

You will need a PC that includes:

- Windows 98™, ME™, 2000™, XP™, or NT ™ (version 4.0) operating system
- One +5VDC, 3.0A power supply with a female (inside positive) power connector (included)

CAUTION

Never supply more than +5.5 V power to the i.MX23 EVK. Doing so can damage board components, and possibly an attached USB device if operating in optional USB OTG Host mode.

1.3.1 System Operating Specifications

Table 1.2 identifies the clock, environmental conditions, and dimensions of the i.MX23 EVK system.

Table 1.2 System Operating Specifications

Item	Specifications
Clock	Master Clock 24 MHz Real Time Clock, Watch Dog Timer 32.768KHz
Temperature: Operating Storage	 -10 °C to + 50 °C -40 °C to +85 °C
Relative Humidity	0 to 90% (noncondensing)
Power Requirements	4.5V to 5.5 V DC @3 A
Dimensions	178 mm x 123 mm

Chapter 2
Configuration and Connections

This section contains configuration information, connection descriptions, and other operational information that may be useful during the development process.

2.1 EVK Top Switches and Connectors

Figure 2-1 identifies the switches and connectors located on the top of the EVK board.

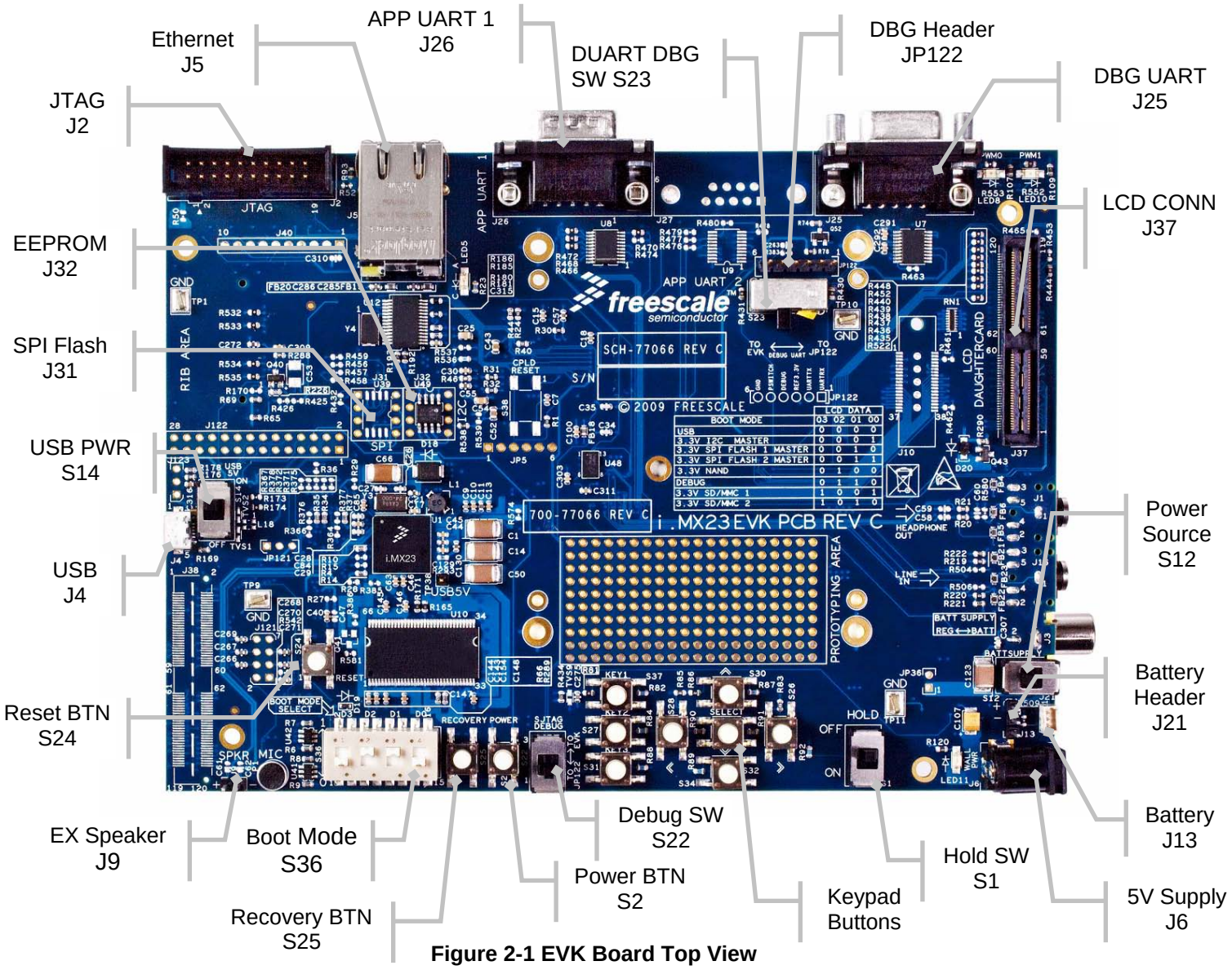

Figure 2-1 EVK Board Top View

Table 2.1 describes the switches and connectors

Table 2.1 EVK Board, Top Components

Identifier	Component	Description
S1	Hold Switch	Connected to the end of a resistive tree network of resistors and UI buttons, the switch creates a specific voltage level sensed by LRADC0 which causes the i.MX23 IC to ignore other changes until the sense voltage returns to the hold OFF voltage level.
S2	Power Button	Connected to the PSwitch input pin of i.MX23 IC, momentarily pressing the button, causes the chip to begin its boot up process. Holding the button down for more than 100 msec at start up will have the same effect as pressing the Recovery Button.
S12	Power Source Select Switch	When switched to the left (REG), simulated 4.2V Battery Power is supplied to the i.MX23 device to allow battery powered operations. When switched to the right (BATT), a Li-ION Battery attached to either J13 or J21 supplies power to the i.MX23 IC. When no Battery is attached, this switch can be used to remove power to the i.MX23 IC. This is a break before make switch.
S14	USB Power Select Switch	This double-pole, double-throw switch can remove USB 5V power supplied by a host to the i.MX23 IC by moving the switch to the OFF (down) position. Normal operation is when the switch is ON (up). This switch is allows the user to effectively remove USB without having to pull the cable.
S22	SJTAG Debug Switch	When in the UP position, this double-pole, double-throw switch connects the output of the CPLD Serialized JTAG signal to the Debug pin of the i.MX23 IC and also connect the output reset signal from the CPLD to the PSWITCH pin of the i.MX23 IC. When in the DOWN position, both circuits are disconnected from the i.MX23 IC, and are instead routed to header JP122 for use in debugging customer prototype boards.
S23	DEBUG UART Switch	When in the LEFT Hand position, this switch connects the DUART_RX (PWM0) and the DUART_TX (PWM1) pins of the i.MX23 IC to the DUART connector. When in the RIGHT Hand position, the DUART signals from the i.MX23 IC on the EVK are disconnected from the DUART connector, and instead, RX and TX signals from a customer prototype board are routed from header JP122 to the UART driver IC and 9- DSUB connector.
S24	Reset Button	Resets the EVK by shorting the Y3 crystal to ground, effectively turning off the internal DC-DC converters. If the USB 5V rail is connected to a 5V source, the EVK will restart. If not connected to a 5V source, the EVK requires the Power Button to be pressed to restart the board.
S25	Recovery Button	Connected to the PSwitch input of the i.MX23 IC, the Recovery Button will provide an elevated voltage level which will override the Boot Mode Switch settings and force the i.MX23 IC to boot in USB Recovery Mode when connected to a USB host.
S26	Right Navigation Button	Connected to the resistive tree network of resistors and provides a specific voltage level sensed by LRADC0. Button definition is user configurable by making software changes.
S27	User Definable Key2 Button	Connected to the resistive tree network of resistors and provides a specific voltage level sensed by LRADC0. Button definition is user configurable by making software changes.

S28	Left Navigation Button	Connected to the resistive tree network of resistors and provides a specific voltage level sensed by LRADC0. Button definition is user configurable by making software changes.
S30	Up Navigation Button	Connected to the resistive tree network of resistors and provides a specific voltage level sensed by LRADC0. Button definition is user configurable by making software changes.
S31	User Definable Key3 Button	Connected to the resistive tree network of resistors and provides a specific voltage level sensed by LRADC0. Button definition is user configurable by making software changes.
S32	Down Navigation Button	Connected to the resistive tree network of resistors and provides a specific voltage level sensed by LRADC0. Button definition is user configurable by making software changes.
S34	Select Navigation Button	Connected to the resistive tree network of resistors and provides a specific voltage level sensed by LRADC0. Button definition is user configurable by making software changes.
S36	Boot Mode Select Switch	Connected to the first 4 data lines of the LCD module, the i.MX23 IC will read the voltage levels on these pins when the i.MX23 IC is initially powered on to determine what mode the IC should boot into. Table 2.2 lists the various Boot Mode options.
S37	User Definable Key1 Button	Connected to the resistive tree network of resistors and provides a specific voltage level sensed by LRADC0. Button definition is user configurable by making software changes.
S38	CPLD Reset (Optional)	Optional Button connected to the CPLD which will force the CPLD to reset and resume operations. This button can be populated when software JTAG reset functionality is not present or insufficient for the users need.
J2	JTAG Connector	20-Pin standard JTAG connector connects to on board CPLD pre-programmed to convert parallel JATG data into a proprietary serialized data stream. Reset commands are separated from the stream and formatted to correctly stop and restart the i.MX23 IC.
J4	USB Micro AB Connector	USB connector conforms to new USB standard micro connector requirements. The AB format allows using the EVK as a USB Host when additional components are populated. D+ and D- traces are connected directly to the I.MX23 IC. The USB_5V power rail goes through a switch to allow for manual removal of 5V power to the IC.
J5	Ethernet RJ45 Connector	Standard RJ45 Jack connects to a SPI Ethernet IC through an isolation transformer. Ethernet IC communicates with i.MX23 via the SPI port also used by the SD/MMC card. A buffer IC disconnects the Ethernet IC from the CPU when an SD/MMC card is inserted and reconnects the Ethernet hardware when the SD/MMC card is removed.
J6	Power connector	5.0V DC power connector. Provides power to a linear regulator which outputs simulated 4.2V battery power for use by the i.MX23 CPU. The external 5V rail also supplies power to two Linear Regulators which independently supply power to the CPLD, Ethernet IC, and UART line drivers. When the EVK is used in USB Host mode, 5V power is also supplied directly from the 5.0V DC Power Supply.
J9	External Speaker Posts	Directly connected to the two External Speaker pins of the i.MX23 IC, these pins can drive an attached external speakers, typically 4 Ohms.

J10	Optional Mictor Connector	Provides support for Super JTAG trace mode. Connects to CPLD to convert JTAG data to proprietary serial data for use by the i.MX23 IC. Additional data is sent over LCD Data lines. When in use, RGB-LCD operations is prohibited
J13	Battery Connector Socket	Three pin connector allows for the attachment of Li-ION batteries with a
J21	Battery Connection Header	3 x 1 pin header version of Battery Connector socket. Allows for the use of generic Li-ION Batteries or an external power supply.
J25	Debug UART	D-SUB9 Connector is driven by a MAX3222 UART Driver IC to provide a Serial Debug Communications port. i.MX23 IC provides debug data over PWM0 and PWM1 pins to the Driver IC. There are no hardware flow control operations on the Debug UART.
J26	Application UART1	D-SUB9 Connector is driven by a MAX3222 UART Driver IC to provide an Application Serial Communications Port. i.MX23 IC provides debug data over UART1: TX, RX, CTS, RTS pins to the Driver IC.
J27	Application UART2 (optional)	Optional D-SUB9 Connector is driven by a MAX3222 UART Driver IC to provide a second Application Serial Communications Port if desired. i.MX23 IC provides debug data over GPMI: D14, D15 for receive and transmit. ROTARY: A, B can supply flow control if necessary.
J31	8-Pin DIP Socket SPI Flash Header	Optional 8-pin DIP Socket can be added to allow EVK user to plug in various SPI Flash ICs, in lieu of soldering SPI Flash directly down on the EVK board.. SPI Flash uses same SPI Header as SD/MMC card and Ethernet. When SPI Flash is inserted, SD/MMC card can not be inserted and Ethernet communications must be disabled. Additional resistors and capacitors must be added to support SPI Flash operations.
J32	8-Pin DIP Socket EEPROM Header	Optional 8-pin DIP Socket can be added to allow EVK user to plug in various I2C EEPROM ICs, in lieu of soldering an EEPROM directly down on the EVK board. Socket connects directly to I2C header of i.MX23 IC, which is shared by various other ICs.
J37	LCD Connector	120-Pin high speed, high density connector designed to fit optional 4.3” WQVGA touch screen display panel. Other panels may become available for use by the EVK over the lifecycle of the i.MX23 IC.
J38	Optional Expansion Port Connector	120-Pin high speed, high density connector designed to fit optional expansion boards which may become available over the lifecycle of the i.MX23 IC.
J40	Optional Remote Interface Header	Used for internal Freescale, large quantity, automated testing.
J121	Optional LRADC Header	Connected to the LRADC pins of the i.MX23 IC, this optional header allows the user access to connect LRADC inputs to the CPU for uses other than those normally used by the EVK.
J122	Optional Remote Interface Header	Used for internal Freescale, large quantity, automated testing.
JP5	CPLD Program Header	Connected to Xilinx CPLD programming pins to allow in-situ programming of the CPLD.
JP36	Optional Battery Power Current Measurement Header	User can cut the traces between the two pins, install a 2 x 1 Header and attach a current probe between the pins to readily measure current drawn from the battery.

JP121	Optional USB 5V Current Measurement Header	User can cut the traces between the two pins, install a 2 x 1 Header pins and attach a current probe between the pins to readily measure current drawn through the USB_5V header.
JP122	OFFBOARD DEBUG Header	This header allows customers to connect wires from customer designed prototype boards to enable the EVK to act as the communication path for JTAG and UART Debug signals. The Prototype board PWM0 signal connects to Pin 1. The Prototype board PWM1 signal connects to Pin 2. The Prototype board DEBUG signal connects to Pin 4. The Prototype board PSWITCH signal connects to Pin 5. The ground connection between the two boards is made through Pin 6. Pin 3 is an optional 3.3V reference pin that can be used as a 3.3V source by the prototype board, or can indicate to the prototype board that the Debug system is powered on. Signal to and from this header are enabled by switches S22 (DOWN) and S23 (RIGHT).
JP123	Optional 5V Source Header	User can cut the traces between the pins 1 - 2, install a 3 x 1 Header and use the header to select the source of 5V power to the i.MX23 IC. The two available choices are through the USB Micro AB connector or from the attached 5.0V DC Power Supply.
LED5	CPLD Activity LED	Indicates when JTAG traffic is being passed to the i.MX23 IC. When off, JTAG communications are idle. When solid on, a JTAG communications link has not been established between the external JTAG IC and the i.MX23 IC.
LED8	PWM0 Activity LED	Indicates when i.MX23 is receiving traffic over the Debug Serial Communications Port. When the receive line is idle and i.MX23 is powered up, this LED is normally solid ON.
LED10	PWM1 Activity LED	Indicates when i.MX23 is transmitting traffic over the Debug Serial Communications Port. When the i.MX23 IC is powered up but not transmitting data, this LED is normally solid ON.
LED11	Power Available LED	LED turns on when External 5.0V DC Power Supply is attached.

2.1.1 Boot Mode Switches

The i.MX23 EVK is normally set to Boot according to the selection made on S36. It is possible to force the EVK to ignore the settings of S36 and boot from the mode programmed into the i.MX23 chip itself by moving Resistor R10 to the R15 pads. Table 2.2 shows the valid combinations of the switches.

Table 2.2 Boot Mode Settings

Boot Mode Device	LCD_D03	LCD_D02	LCD_D01	LCD_D00
USB (Recovery)	0	0	0	0
3.3V I2C Master	0	0	0	1
3.3V SPI Flash 1 Master	0	0	1	0
3.3V NAND	0	1	0	0
DEBUG	0	1	1	0
3.3V SD/MMC	1	0	0	1

2.1.2 EVK Bottom Connectors

Figure 2-2 identifies the switches and connectors located on the bottom of the EVK board. Table 2.3 describes the switches and connectors.

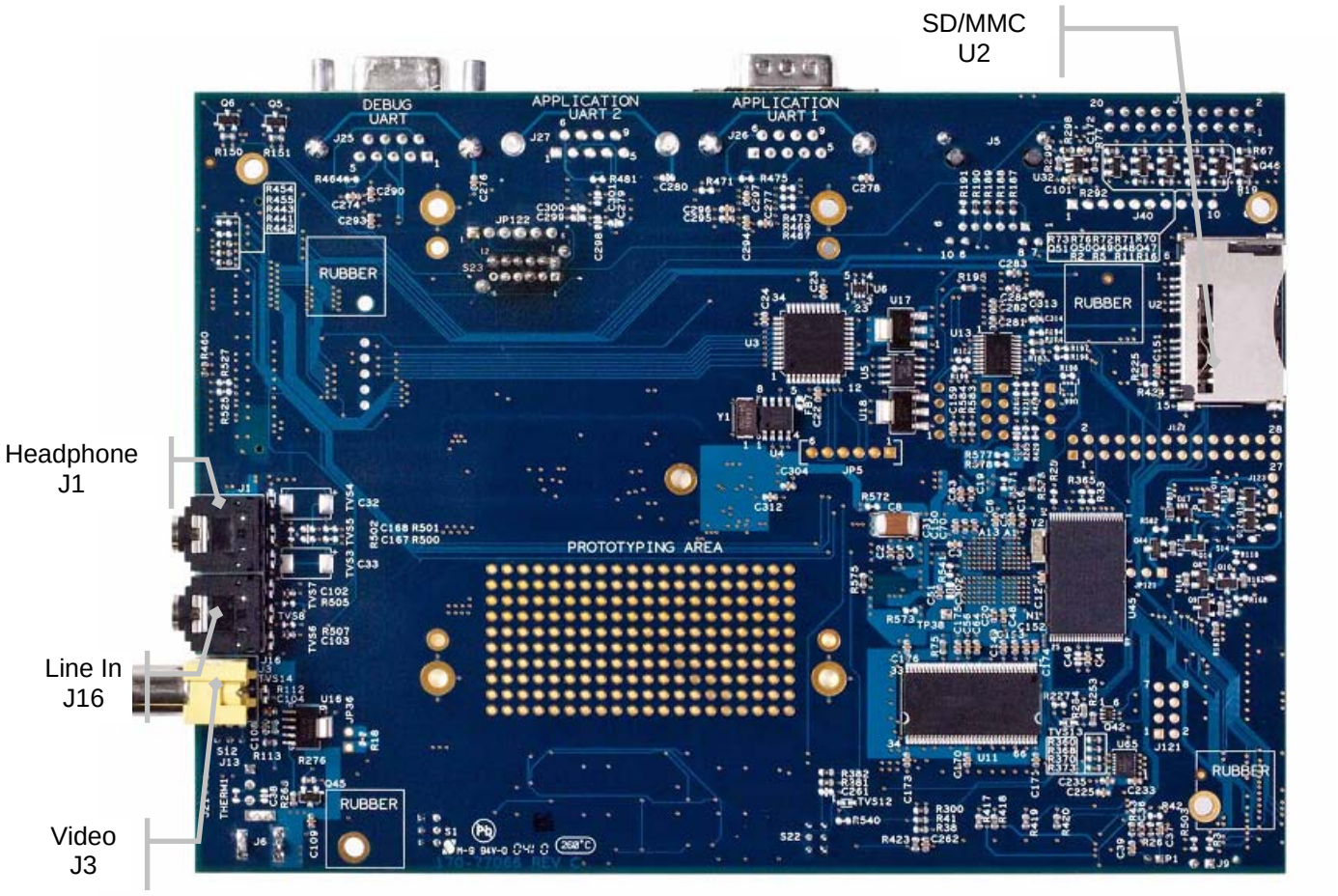

Figure2-2 EVK Board, bottom view

Table 2.3 Debug Board, Top Components

Identifier	Component	Description
J1	Headphone Jack	Standard 3.5mm diameter stereo jack connects with the Head Phone Output pins of the i.MX23 device. Circuit is normally in Direct drive Mode. AC Coupled mode can be optionally installed.
J3	Composite Video	RCA jack connects to VDAC pin of the i.MX23 device
J16	Line In Jack	Standard 3.5mm diameter stereo jack connects with the Line In pins for the i.MX23 device.

U2	SD/MMC Card Connector	Standard SD/MMC card connector connects to the i.MX23 device via the SSP1 module. This module also shares with Ethernet operations and an optional SPI Flash. 3.3V power is only supplied to the connector when an SD/MMC Card is physically inserted into the slot and the i.MX23 recognizes the presence of the card and turns on power to the card. When SD/MMC power is turned on, Ethernet operations are disconnected through a buffer chip.

2.2 Setting Up the EVK for Normal Operations

2.2.1 Set the EVK Board Switches

To set the EVK board switches for normal operations, use these steps:

1. Attach the 5.0V DC Power Supply to Jack J6 and plug the AC end into an electrical source.
2. Slide USB 5V Switch (S14) to the ON position (up).
3. Slide Debug Switch (S22) to the OFF position (down).
4. Slide the Hold Switch (S1) to the OFF position (up).
5. Set the Boot Mode Selector Switch (S36) to the desired mode per Table 2.2.

   “0 1 0 0” to boot from the on board NAND Flash

   “1 0 0 1” to boot from an SD/MMC card
6. Slide Power Source Selector Switch (S12) to the REG position (left).
7. Momentarily depress the Power Button (S2) to power on the EVK.

   LED8 and LED10 will both be powered ON during normal operations.

2.2.2 Connect the optional LCD to the EVK board.

Figure 2-3 illustrates how to connect the optional LCD Daughter Card to the EVK Board.

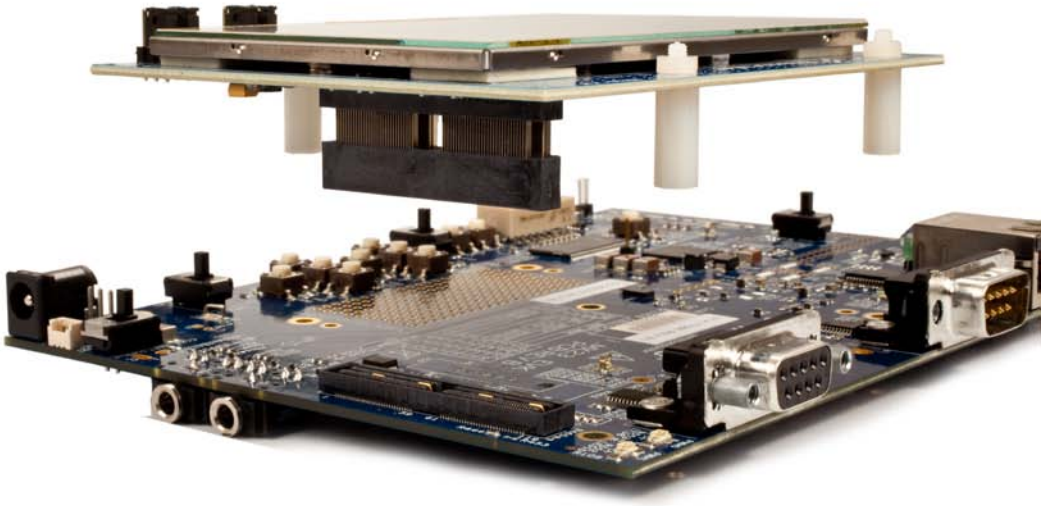

Figure2-3 Connecting LCD to EVK

Chapter 3
Functional Operation

3.1 Functional Block Diagrams

Figure 3-1 illustrates the functional blocks of i.MX23 EVK.

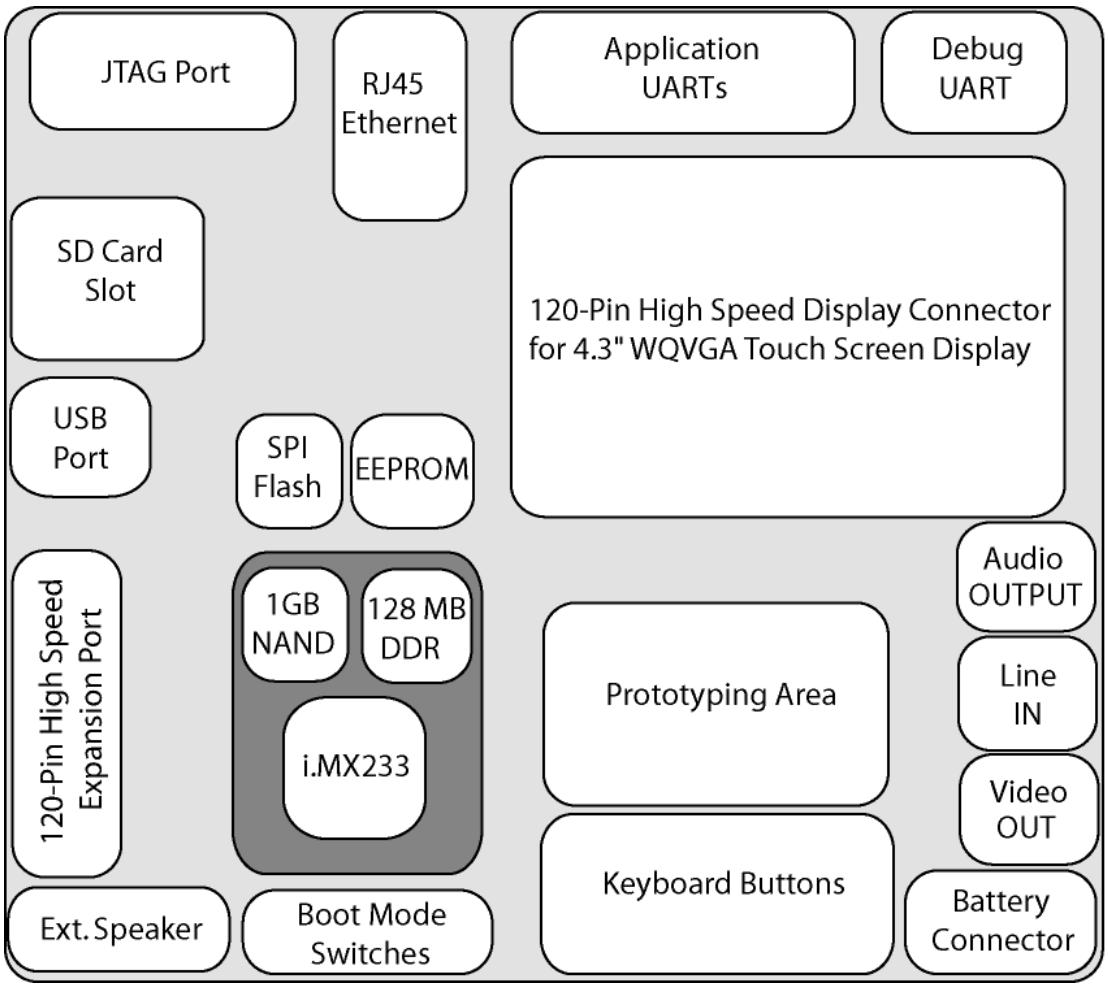

Figure3-1 i.MX23 EVK Functional Block

3.2 EVK Memory Map

Table 3.1 describes the memory map for the EVK. The i.MX23 chip is capable of using up to 512 MB of SDRAM. The unused Address Ranges for SDRAM mirror the data stored in the physically present DDR1 SDRAM. For example, addresses 0x48000000, 0x50000000, and 0x58000000 will all contain the same data as physically located at 0x40000000.

Table 3.1 Memory Map

Peripheral	Chip Select	Address Range (HEX)	Size
DDR1	EMI_CE0n	0x40000000 to 0x43FFFFFF	64MB
DDR1	EMI_CE1n	0x44000000 to 0x47FFFFFF	64MB

3.3 Using the EVK to provide JTAG/UART support for custom designed prototype boards (Only on Rev C boards)

The i.MX23 EVK, on the revision C of the board, is designed to allow the serial JTAG function and the Debug UART functions to be disconnected from the CPU and used independently to support the bring up of other prototype boards. To use this feature, the designer must have available:

-A wire connected to the DEBUG pin of the CPU (E12).

- A wire connected to the PSWITCH pin of the CPU (B3).

- A wire connected to PWM0 (C3).

- A wire connected to PWM1 (D2).

- A wire connected to system ground.

To use the EVK to support the prototype:

1. Place the SJTAG DEBUG switch (S22) in the down (TO JP122) position.

2. Place switch S23 in the right position (TO JP122).

3. Connect the prototype wires to the EVK as follows:

a. PWM0 to JP122 Pin 1

b. PWM1 to JP122 pin 2

c. DEBUG to JP122 pin 4

d. PSWITCH to JP122 pin 5

e. GROUND to JP122 pin 6.

4. Ensure that 5V wall power is supplied to the board. The UART driver IC and the CPLD will automatically receive power from the EVK regulators. Any CPU operations at this time will not affect the JATG/DUART signals. To ensure that the CPU is kept off, the BATTERY SUPPLY switch (S12) can be moved to the right and any Li-ION battery detached from the EVK.

The JTAG and UART connections should now work for the attached prototype board in the same way they work for the EVK CPU.

Chapter 4
Connectors and Signals

This chapter provides connector pin assignments and signals for EVK board.

- The tables in this section list signal names as they appear in the board schematics.

4.1 LCD Connector

On the EVK, J37 is the connector normally used to attach the optional 4.3” WQVGA Touch Screen LCD Panel. Table 4.1 provides the pin information of the connector.

Table 4.1 LCD Connector Pin-Out

Pin Number	Symbol	Description
1	VDDA	1.8V Power Supplied by i.MX23
2	EXT_5VDC	5.0V DC Power Supplied directly from External Power Supply
3	NC	Not used on EVK
4	EXT_5VDC	5.0V DC Power Supplied directly from External Power Supply
5	VDDIO_P	3.3 V Power Supplied by i.MX23
6	GND	Power Ground
7	NC	Not used on EVK
8	EXT_5VDC	5.0V DC Power Supplied directly from External Power Supply
9	NC	Not used on EVK
10	NC	Not used on EVK
11	BL_VIN	Power Source for LCD Backlight selected by EVK
12	GND	Power Ground
13	BL_VIN	Power Source for LCD Backlight selected by EVK
14	NC	Not used on EVK
15	NC	Not used on EVK
16	NC	Not used on EVK
17	VDDA	1.8V Power Supplied by i.MX23
18	GND	Power Ground
19	VDDA	1.8V Power Supplied by i.MX23

Pin Number	Symbol	Description
20	NC	Not used on EVK
21	EXT_5VDC	5.0V DC Power Supplied directly from External Power Supply
22	NC	Not used on EVK
23	GND	Power Ground
24	GND	Power Ground
25	NC	Not used on EVK
26	NC	Not used on EVK
27	NC	Not used on EVK
28	NC	Not used on EVK
29	LCD_I2C_SDA	I2C Data Signal option for an alternate LCD panel design.
30	GDN	Power Ground
31	LCD_I2C_SCL	I2C Clock Signal option for an alternate LCD panel design.
32	NC	Not used on EVK
33	LCD_RESET	Powers ON/OFF the LCD Panel
34	NC	Not used on EVK
35	NC	Not used on EVK
36	GND	Power Ground
37	NC	Not used on EVK
38	NC	Not used on EVK
39	BL_VIN	Power Source for LCD Backlight selected by EVK
40	NC	Not used on EVK
41	BL_VIN	Power Source for LCD Backlight selected by EVK
42	GND	Power Ground
43	DOTCLK	LCD Clock Input signal
44	NC	Not used on EVK
45	VDDIO_P	3.3 V Power Supplied by i.MX23
46	NC	Not used on EVK
47	VDDIO_P	3.3 V Power Supplied by i.MX23
48	GND	Power Ground
49	VDDIO_P	3.3 V Power Supplied by i.MX23
50	NC	Not used on EVK
51	NC	Not used on EVK

Pin Number	Symbol	Description
52	NC	Not used on EVK
53	NC	Not used on EVK
54	GND	Power Ground
55	NC	Not used on EVK
56	NC	Not used on EVK
57	NC	Not used on EVK
58	NC	Not used on EVK
59	NC	Not used on EVK
60	GND	Power Ground
61	PORT5_ID1	Optional Panel Identification Pin
62	LCD_D00	Blue Data 0
63	NC	Not used on EVK
64	LCD_D01	Blue Data 1
65	Li-ION_BATTERY	Power Supplied from Battery Rail
66	LCD_D02	Blue Data 2
67	Li-ION_BATTERY	Power Supplied from Battery Rail
68	LCD_D03	Blue Data 3
69	Li-ION_BATTERY	Power Supplied from Battery Rail
70	LCD_D04	Blue Data 4
71	Li-ION_BATTERY	Power Supplied from Battery Rail
72	LCD_D05	Blue Data 5
73	USB_5V	Power Supplied from USB-5V Rail
74	LCD_D06	Blue Data 6
75	USB_5V	Power Supplied from USB-5V Rail
76	LCD_D07	Blue Data 7
77	USB_5V	Power Supplied from USB-5V Rail
78	LCD_D08	Green Data 0
79	NC	Not used on EVK
80	LCD_D09	Green Data 1
81	NC	Not used on EVK
82	LCD_D10	Green Data 2
83	PORT5_ID0	Optional Panel Identification Pin
84	LCD_D11	Green Data 3
85	NC	Not used on EVK
86	LCD_D12	Green Data 4

Pin Number	Symbol	Description
87	NC	Not used on EVK
88	LCD_D13	Green Data 5
89	NC	Not used on EVK
90	LCD_D14	Green Data 6
91	NC	Not used on EVK
92	LCD_D15	Green Data 7
93	GND	Power Ground
94	LCD_D16	Red Data 0
95	TOUCHSCREEN_Y+	Resistive Touch Screen UP Signal
96	LCD_D17	Red Data 1
97	TOUCHSCREEN_Y-	Resistive Touch Screen DOWN Signal
98	LCD_D18	Red Data 2
99	TOUCHSCREEN_X+	Resistive Touch Screen RIGHT Signal
100	LCD_D19	Red Data 3
101	TOUCHSCREEN_X-	Resistive Touch Screen LEFT Signal
102	LCD_D20	Red Data 4
103	GND	Power Ground
104	LCD_D21	Red Data 5
105	LCD_CS0	LCD Select used for an alternate LCD Panel Design
106	LCD_D22	Red Data 6
107	NC	Not used on EVK
108	LCD_D23	Red Data 7
109	LCD_WR0	LCD Write used for an alternate LCD Panel Design
110	LCD_VSYNCH	Vertical Synchronization Signal
111	NC	Not used on EVK
112	BACKLIGHT_PWM	Signal used to control LCD Backlight Brightness
113	NC	Not used on EVK
114	LCD_HSYNCH	Horizontal Synchronization Signal
115	NC	Not used on EVK
116	LCD_EN	LCD Enable effects data communications pins of the LCD
117	NC	Not used on EVK

Pin Number	Symbol	Description
118	NC	Not used on EVK
119	LCD_RS0	LCD Reset for an alternate LCD Panel Design
120	NC	Not used on EVK

4.2 Optional Expansion Port Connector

On the EVK, J38 is an optional 120-pin connector that may be used for future expansion designs. Table 4.2 provides the pin information of the connector.

Table 4.2 Expansion Port Connector Pin-Out

Pin Number	Symbol	Description
1	NC	Not used on EVK
2	EXT_5VDC	5.0V DC Power Supplied directly from External Power Supply
3	NC	Not used on EVK
4	EXT_5VDC	5.0V DC Power Supplied directly from External Power Supply
5	NC	Not used on EVK
6	GND	Power Ground
7	NC	Not used on EVK
8	EXT_5VDC	5.0V DC Power Supplied directly from External Power Supply
9	NC	Not used on EVK
10	NC	Not used on EVK
11	NC	Not used on EVK
12	GND	Power Ground
13	NC	Not used on EVK
14	NC	Not used on EVK
15	VDDA	1.8V Power Supplied by i.MX23
16	NC	Not used on EVK
17	VDDA	1.8V Power Supplied by i.MX23
18	GND	Power Ground
19	NC	Not used on EVK
20	NC	Not used on EVK
21	NC	Not used on EVK
22	NC	Not used on EVK

Pin Number	Symbol	Description
23	NC	Not used on EVK
24	GND	Power Ground
25	NC	Not used on EVK
26	NC	Not used on EVK
27	NC	Not used on EVK
28	NC	Not used on EVK
29	NC	Not used on EVK
30	GDN	Power Ground
31	NC	Not used on EVK
32	NC	Not used on EVK
33	NC	Not used on EVK
34	NC	Not used on EVK
35	NC	Not used on EVK
36	GND	Power Ground
37	NC	Not used on EVK
38	NC	Not used on EVK
39	NC	Not used on EVK
40	NC	Not used on EVK
41	NC	Not used on EVK
42	GND	Power Ground
43	NC	Not used on EVK
44	NC	Not used on EVK
45	VDDIO_P	3.3 V Power Supplied by i.MX23
46	NC	Not used on EVK
47	VDDIO_P	3.3 V Power Supplied by i.MX23
48	GND	Power Ground
49	VDDIO_P	3.3 V Power Supplied by i.MX23
50	NC	Not used on EVK
51	NC	Not used on EVK
52	NC	Not used on EVK
53	NC	Not used on EVK
54	GND	Power Ground
55	NC	Not used on EVK
56	NC	Not used on EVK
57	NC	Not used on EVK

Pin Number	Symbol	Description
58	NC	Not used on EVK
59	NC	Not used on EVK
60	GND	Power Ground
61	PORT1_ID1	Optional Panel Identification Pin
62	UART1_TX	Application 1 UART Transmit from i.MX23 device
63	NC	Not used on EVK
64	UART1_RX	Application 1 UART Receive from i.MX23 device
65	Li-ION_BATTERY	Power Supplied from Battery Rail
66	UART1_RTS	Application 1 UART RTS from i.MX23 device
67	Li-ION_BATTERY	Power Supplied from Battery Rail
68	UART1_CTS	Application 1 UART CTS from i.MX23 device
69	Li-ION_BATTERY	Power Supplied from Battery Rail
70	NC	Not used on EVK
71	Li-ION_BATTERY	Power Supplied from Battery Rail
72	NC	Not used on EVK
73	USB_5V	Power Supplied from USB-5V Rail
74	NC	Not used on EVK
75	USB_5V	Power Supplied from USB-5V Rail
76	NC	Not used on EVK
77	USB_5V	Power Supplied from USB-5V Rail
78	NC	Not used on EVK
79	NC	Not used on EVK
80	NC	Not used on EVK
81	NC	Not used on EVK
82	NC	Not used on EVK
83	PORT1_ID0	Optional Panel Identification Pin
84	NC	Not used on EVK
85	XPORT_SPI1_MISO	Shared SPI bus Master Input Slave Output Signal
86	NC	Not used on EVK
87	XPORT_SPI1_MOSI	Shared SPI bus Master Output Slave Input Signal
88	NC	Not used on EVK
89	XPORT_SPI1_SCK	Shared SPI bus Clock Signal

Pin Number	Symbol	Description
90	NC	Not used on EVK
91	XPORT_SPI1_SS#	Shared SPI bus Device Select
92	NC	Not used on EVK
93	GND	Power Ground
94	NC	Not used on EVK
95	LCD_D08	Software defined GPMIO pin
96	NC	Not used on EVK
97	LCD_D09	Software defined GPMIO pin
98	NC	Not used on EVK
99	LCD_D10	Software defined GPMIO pin
100	NC	Not used on EVK
101	LCD_D11	Software defined GPMIO pin
102	SSP1_DATA2	SPI Data Post Data 2 Signal
103	GND	Power Ground
104	XPORT_SPI1_SS#	Shared SPI bus Device Select
105	NC	Not used on EVK
106	GPMI_D08	Software defined GPMIO pin
107	LCD_I2C_SDA	I2C Data Signal
108	XPORT_SPI1_MOSI	Shared SPI bus Master Output Slave Input Signal
109	LCD_I2C_SCL	I2C Clock Signal
110	GPMI_D09	Software defined GPMIO pin
111	NC	Not used on EVK
112	XPORT_SPI1_SCK	Shared SPI bus Clock Signal
113	NC	Not used on EVK
114	GPMI_D10	Software defined GPMIO pin
115	NC	Not used on EVK
116	GPMI_D11	Software defined GPMIO pin
117	SSP1_DETECT	Shared SPI bus device detect pin
118	XPORT_SPI1_MISO	Shared SPI bus Master Input Slave Output Signal
119	PWM4	PWM4 signal from i.MX23 device
120	SSP1_DATA1	SPI Data Post Data 1 Signal