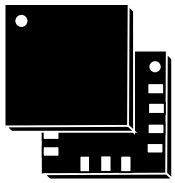
LIS25BA

MEMS digital output motion sensor: low-noise, high-bandwidth 3-axis accelerometer with TDM interface

Datasheet - production data



LGA-14 (2.5x2.5x0.86 mm)

Features

- ±3.85 *g* full scale
- TDM slave interface
- Low noise
- Signal bandwidth 2400 Hz
- High, flat bandwidth
- 16-bit data output
- 20000 *g* high shock survivability
- Lead-free, ECOPACK®, RoHS and “Green” compliant

Description

The LIS25BA is a low-noise high-bandwidth three-axis digital accelerometer with a dedicated TDM interface.

The LIS25BA has a full scale of ±3.85 *g* and works with a Time-Division Multiplexing (TDM) interface.

The LIS25BA is available in a small thin plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order codes	Temp. range [°C]	Package	Packaging
LIS25BA	-40 to +85	LGA-14	Tray
LIS25BATR	-40 to +85	LGA-14	Tape and reel

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1 Pin description

Figure 1. Pin connections

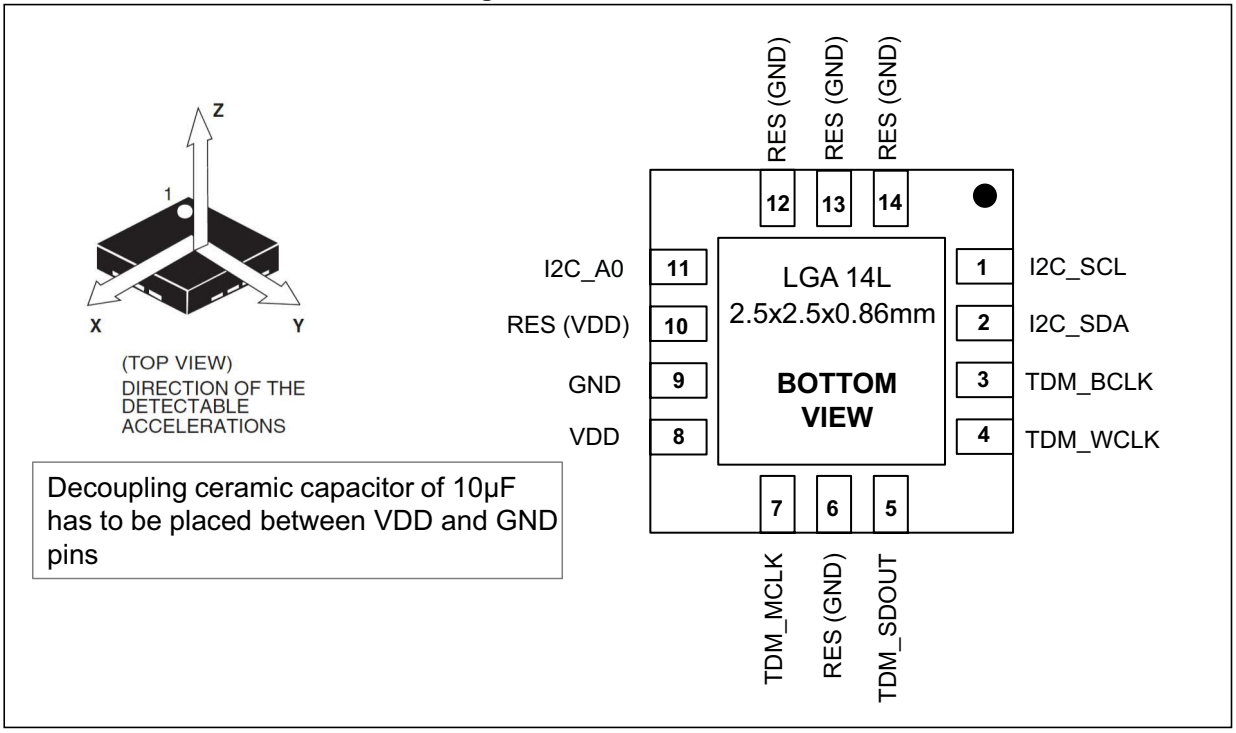


Table 2. Pin description

Pin#	Name	IN/OUT	Function
1	I2C_SCL(1)	IN	I²C serial clock - SCL
2	I2C_SDA(1)	IN/OUT	I²C serial data - SDA
3	TDM_BCLK	IN	TDM bit clock
4	TDM_WCLK	IN	TDM word clock
5	TDM_SDOUT	OUT	TDM serial data output
6	RES (GND)	-	Reserved pin (connect to GND)
7	TDM_MCLK	IN	TDM master clock
8	VDD		Power supply
9	GND		0 V supply
10	RES (VDD)	-	Reserved pin (connect to VDD)
11	I2C_A0	IN	I²C slave address selection
12	RES (GND)	-	Reserved pin (connect to GND)
13	RES (GND)	-	Reserved pin (connect to GND)
14	RES (GND)	-	Reserved pin (connect to GND)

1. Only for test and trim. I²C timing values are not guaranteed.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
FS	Measurement range	After factory calibration (trimming performed with 1 *g* DC stimulus)	3.26	3.85	4.16	*g*
So	Sensitivity	After factory calibration (trimming performed with 1 *g* DC stimulus)	0.112	0.122	0.132	mg/LSB
		After factory calibration (trimming performed with 1 *g* DC stimulus)	-11.37	-11.71	-12.38	dBFS/*g*
		After factory calibration - 100 Hz 1 *g*rms sine stimulus	-8.37	-8.71	-9.38	dBFS/*g*rms
TCSo	Sensitivity change vs. temperature		-0.08		+0.08	%/°C
TyOff	Zero-*g* level offset accuracy		-300		+300	m*g*
TCOff	Zero-*g* level change vs. temperature		-3.5		+3.5	mg/°C
An	Acceleration noise	X-axis, Y-axis, FS = ±3.85 *g*, BW = 2400 Hz			1.5	m*g* rms
		Z-axis, FS = ±3.85 *g*, BW = 2400 Hz			2.4	
BW	Signal bandwidth[2] (DC coupling)	MCLK accuracy ±0.1%		2400		Hz
NL	Non-linearity[3]		-2		+2	%FS
RFm	Mechanical resonant frequency of the MEMS element	X-axis		5150		Hz
		Y-axis		5150		Hz
		Z-axis		4950		Hz
ST	Self-test[4]	X-axis	300		950	m*g*
		Y-axis	300		950	m*g*
		Z-axis	500		2700	m*g*
THD+N	Total Harmonic Distortion + Noise[5]	@ sinusoidal vibration of 1 *g* peak, freq = 1 kHz			1	%

1. Typical specifications are not guaranteed.
2. By design.
3. MEMS non-linearity based on simulation data.
4. Values are based on preliminary corner simulation data.
5. Max. value is guaranteed by characterization and not tested in production.

a. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.71 V to 1.99 V.

2.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted[b].

Table 4. Electrical characteristics [1]

Symbol	Parameter	Test conditions	Min.	Typ.[2]	Max.	Unit
Vdd	Supply voltage		1.71	1.8	1.99	V
IddT	Current consumption in triaxial mode[3]			2.58	3.3	mA
IddB	Current consumption in biaxial mode[3]			2.13	2.75	mA
IddM	Current consumption in monoaxial mode[3]			1.68	2.2	mA
IddD0	Current consumption in disabled mode	no external clock switching[4]			10	uA
IddD1	Current consumption in disabled mode	TDM standard clock (MCLK = 12.288 MHz, BCLK=3.072 MHz)[4]			205	uA
ODR	Output data rate	TDM @ 8 kHz		8		kHz
		TDM @ 16 kHz		16		kHz
		TDM @ 24 kHz		24		kHz
Tstart	Startup time				10	ms
VIH	Digital high-level input voltage	all pins, except pin 10 and 11	0.7*Vdd			V
		pin 10 and 11	0.8*Vdd			V
VIL	Digital low-level input voltage				0.2*Vdd	V
VOH	High-level output voltage	IOH = 2 mA[5]	Vdd - 0.2			V
VOL	Low-level output voltage	IOL = 2 mA[5]			0.2	V
$PSR_{IBX/Y}$	PSR in band	"Electrical noise" test mode. Vdd = 1.8 V, Vripple = 50 mVpp sin(2πωt) Sweep ω from 20 Hz to 20 kHz See *Figure 2*			3.16	mg_{rms}
PSR_{IBZ}					6.32	mg_{rms}
$PSR_{OBX/Y}$	PSR out of band	"Electrical noise" test mode. Vdd = 1.8 V, Vripple = 50 mVpp sin(2πωt) Sweep ω from 1 MHz to 10 MHz See *Figure 3*			31.6	mg_{rms}
PSR_{OBZ}					63.2	mg_{rms}
Top	Operating temperature range		-40		+85	°C

b. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.71 V to 1.99 V.

1. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.71 V to 1.99 V.
2. Typical specifications are not guaranteed.
3. Min. and max. values are guaranteed by characterization and not tested in production. Values are intended in the temperature and voltage operating range.
4. Min. and max. values are guaranteed by characterization and not tested in production.
5. 2 mA is the maximum driving capability, i.e. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels VOH and VOL.

Figure 2. RMS noise (in band)

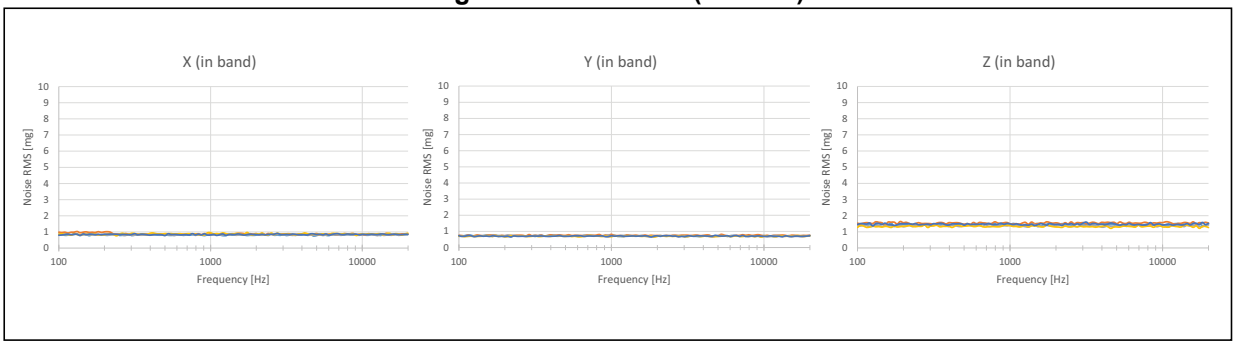
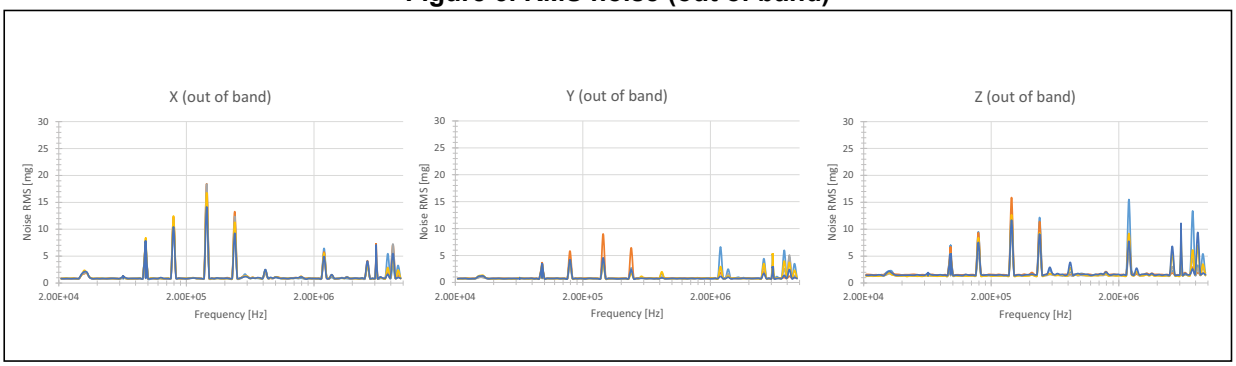


Figure 3. RMS noise (out of band)



2.3 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
STR	Storage temperature range	-40 to +125	°C
Sg	MIL-STD-883H, Method 2002.5, Condition F	20,000	*g*
	MIL-STD-883H, Method 2002.5, Condition E	10,000	
	MIL-STD-883H, Method 2002.5, Condition D	5,000	
EDP	Electrostatic discharge protection (HBM)	2	kV
V_{MAX}	Maximum input voltage on all input pins	4.8	V
V_{MIN}	Minimum input voltage on all input pins	-0.3	V
I_{IN}	Input current on all I/O pins (does not cause SCR latch-up)	+/-10	mA

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 TDM interface characteristics

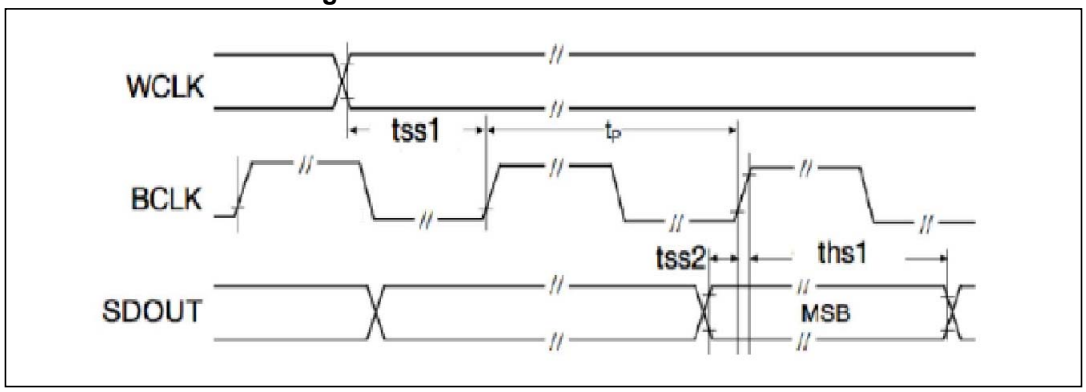
Please refer to *Section 4: TDM interface specifications* for additional details.

Table 6. TDM interface characteristics (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
MCLK	MCLK frequency nominal			12.288		MHz
MCLKA	MCLK frequency accuracy		-0.1		0.1	%
MCLKJ	MCLK jitter				1	ns (peak to peak)
BCLK	BCLK frequency (1/tp)	in disabled mode			MCLK	MHz
		WCLK = 8 kHz		1.024		MHz
		WCLK = 16 kHz		2.048		MHz
		WCLK = 24 kHz		3.072		MHz
WCLK8	8 kHz WCLK mode			8		kHz
WCLK16	16 kHz WCLK mode			16		
WCLK24	24 kHz WCLK mode			24		
PDC	All clock pin duty cycle (except WCLK)		45		55	%
WT	WCLK setup time before BCLK rising/falling edge (tss1)		20			ns
SDOST	SDOUT setup time before BCLK rising/falling edge (tss2)		15			ns
SDOHTR	SDOUT hold time after BCLK rising/falling edge (ths1)		15			ns
SDOHTZ	SDOUT hold time of LSB after BCLK rising/falling edge (ths2)		15		50	ns
C_{MCLK}	MCLK pin capacitance				10	pF
C_{BCLK}	BCLK pin capacitance				10	
C_{WCLK}	VCLK pin capacitance				10	
C_{SDOUT}	SDOUT load capacitance				60	
FR_{REL}	Relative frequency response(2)	(3)	-0.5		0.4	dB

1. All setup times and hold times in *Table 6* and in *Figure 4* are valid for BCLK polarity set to “clock on rising”. If BCLK polarity is set to “clock on falling”, then all setup and hold times will refer to the falling edge of BCLK instead. Please refer to *Section 4: TDM interface specifications* for additional details.
2. Data by simulation
3. All the DUT measurement points are normalized to the 294 Hz measurement. The deviation between each point and 294 Hz is calculated. The maximum deviation for points measured at frequencies below 2.0 kHz is given as FR_{REL}.

Figure 4. TDM interface characteristics



3.1 I²C interface characteristics

Please refer to *Section 5: I²C- inter-IC control interface* for additional details.

Table 7. Digital input/output voltage for I²C pins(1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
VIH	Digital high-level input voltage		0.7*Vdd			V
VIL	Digital low-level input voltage				0.2*Vdd	V
VOL	Low-level output voltage	IOL = 4 mA(3)	0.2			V

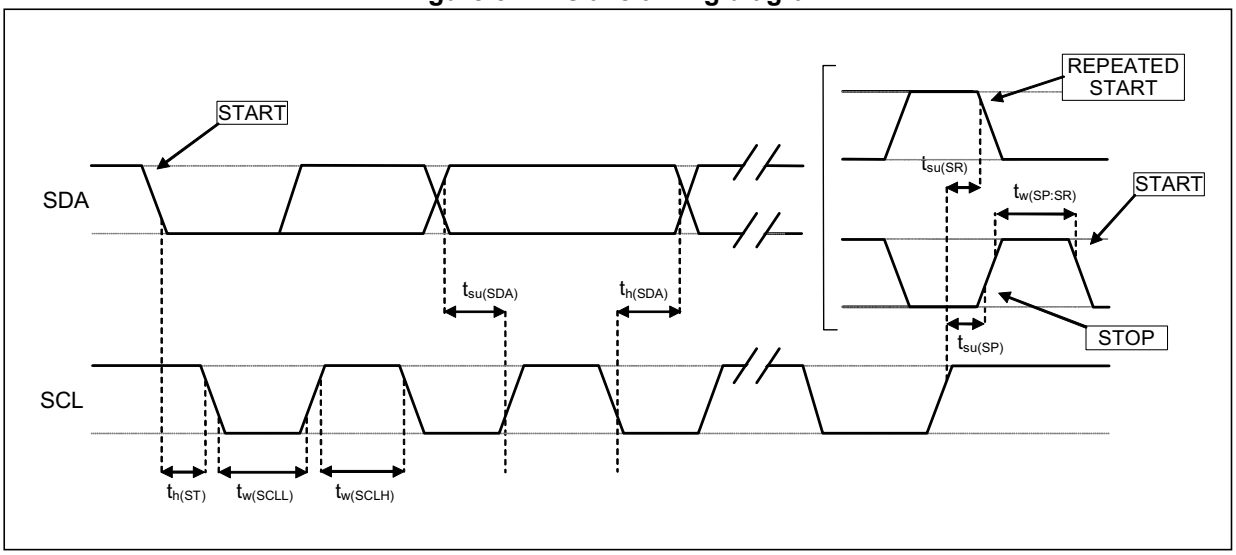
1. Data based on standard I²C protocol requirement, intended only for test and trim. Values are not guaranteed.
2. Typical specifications are not guaranteed.
3. 4 mA is the maximum driving capability, i.e. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels VOH and VOL.

Table 8. I²C interface characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
$f_{(SCL)}$	SCL		96		400	kHz
C_{SDA-N}	SDA/SCL bus capacitance normal mode	R_{SDA} = 2.5 kOhm			150	pF
C_{SDA-HS}	SDA/SCL bus capacitance high speed mode	R_{SDA} = 2.5 kOhm			50	pF
R_{SDA}	SDA/SCL pull-up resistance		2500			Ohm
$t_{w(SCLL)}$	SCL clock low time		1.3			µs
$t_{w(SCLH)}$	SCL clock high time		0.6			
$t_{su(SDA)}$	SDA setup time		100			ns
$t_{h(SDA)}$	SDA data hold time		0		0.9	µs
$t_{h(ST)}$	START condition hold time		0.6			µs
$t_{su(SR)}$	Repeated START condition setup time		0.6			
$t_{su(SP)}$	STOP condition setup time		0.6			
$t_{w(SP:SR)}$	Bus free time between STOP and START condition		1.3			
I2C_HYST	SDA/SCL minimum pulse width hysteresis				50	ns

1. Typical specifications are not guaranteed.

Figure 5. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd and 0.8·Vdd, for both ports.

Table 9. I²C high-speed mode specifications at 1 MHz

	Symbol	Parameter	Min	Max	Unit
Fast mode plus(1)	f_{SCL}	SCL clock frequency	0	1	MHz
	$t_{HD;STA}$	Hold time (repeated) START condition	260	-	ns
	t_{LOW}	Low period of the SCL clock	500	-	
	t_{HIGH}	High period of the SCL clock	260	-	
	$t_{SU;STA}$	Setup time for a repeated START condition	260	-	
	$t_{HD;DAT}$	Data hold time	0	-	
	$t_{SU;DAT}$	Data setup time	50	-	
	t_{rDA}	Rise time of SDA signal	-	120	
	t_{fDA}	Fall time of SDA signal	-	120	
	t_{rCL}	Rise time of SCL signal	20*Vdd/5.5	120	
	t_{fCL}	Fall time of SCL signal	20*Vdd/5.5	120	
	$t_{SU;STO}$	Setup time for STOP condition	260	-	
	C_b	Capacitive load for each bus line	-	550	pF
	$t_{VD;DAT}$	Data valid time	-	450	ns
	$t_{VD;ACK}$	Data valid acknowledge time	-	450	
	V_{nL}	Noise margin at low level	0.1Vdd	-	V
	V_{nH}	Noise margin at high level	0.2Vdd	-	
	t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0	50	ns

1. Data based on characterization, not tested in production

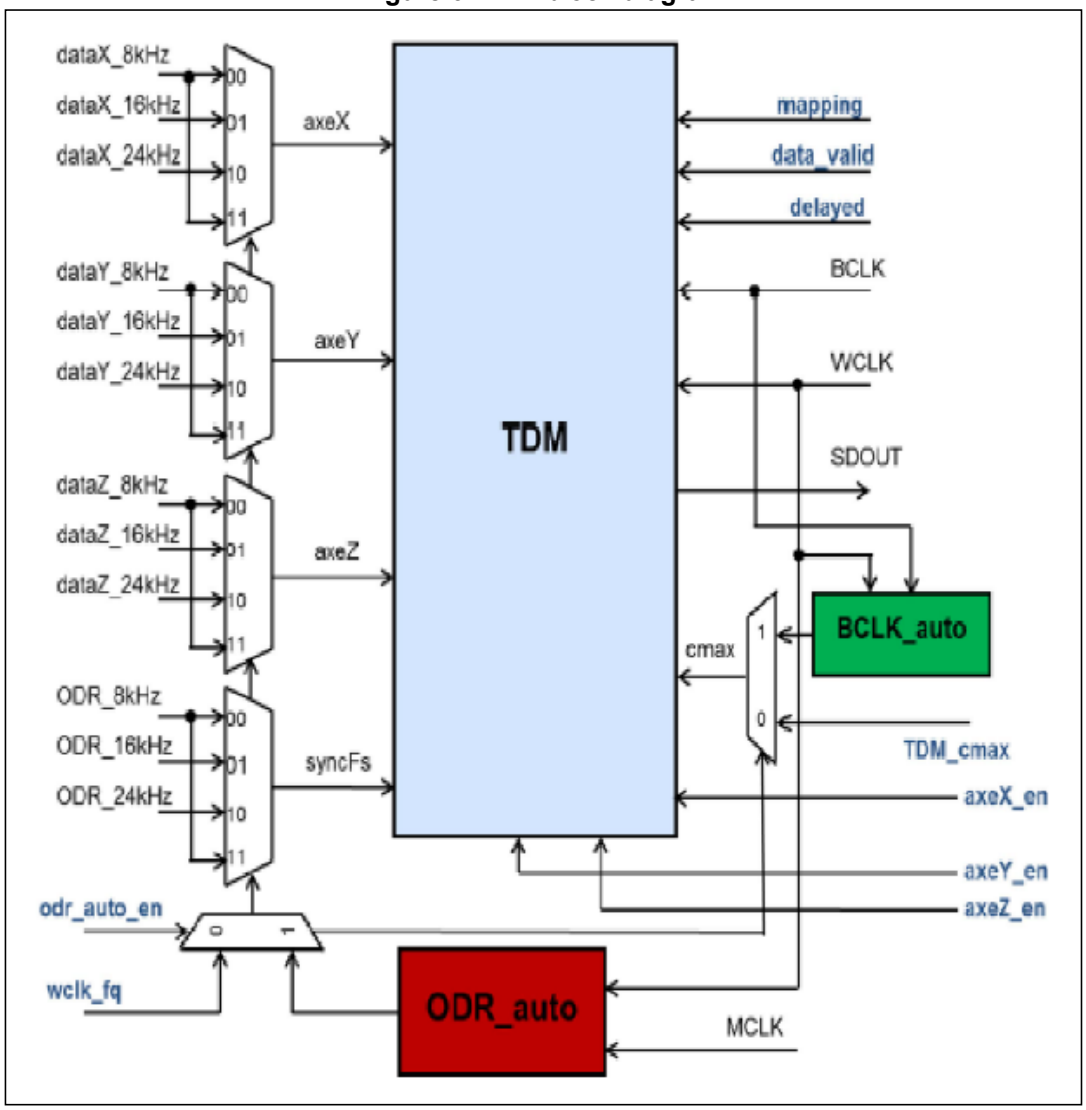
4 TDM interface specifications

Time-division multiplexing (TDM) is a method of putting multiple data streams in one data signal by separating the signal into many frames. There are many ways to accomplish this.

4.1 TDM interface overview

The block diagram of the TDM interface implemented in the LIS25BA device is given in *Figure 6*.

Figure 6. TDM block diagram



As depicted in the figure above, the TDM interface is comprised of two control clocks, a frame synchronization (WCLK) a serial clock (BCLK), and the serial data out (SDOUT).

4.2 Frame synchronization (WCLK)

The function of the WCLK is simply to identify the beginning of a frame. In particular the frame start at the rising edge of WCLK, and the WCLK widths supported are:

- 50% duty cycle
- One slot width (16 BCLK)
- One BCLK width

In TDM mode, LIS25BA shall output accelerometer data on the SDOUT pin at the following sampling rates:

- WCLK = 8 kHz
- WCLK = 16 kHz
- WCLK = 24 kHz

As depicted in *Figure 6*, the TDM input sampling rate (ODR_8kHz, ODR_16kHz and ODR_24kHz), and the associated data inputs (dataX_8kHz, dataX_16kHz, dataX_24kHz, dataY_8kHz, dataY_16kHz, dataY_24kHz, dataZ_8kHz, dataZ_16kHz and dataZ_24kHz) can be selected in two different ways:

1. Using the I²C register *wclk_fq* (*TDM_CTRL_REG (2Eh), bits 2 and 1*). In this case the I²C register ODR_AUTO_EN *(AXES_CTRL_REG (2Fh), bit 0)* is equal to zero, that means that the *ODR_auto* functionality is disabled.
2. Using the output of the *ODR_auto* block (ODR_AUTO_EN *(AXES_CTRL_REG (2Fh), bit 0)* equal to one*)*. This latter simply receives as inputs both the MCLK and the WCLK and it computes the current sampling frequency as a ratio between the MCLK and WCLK.

The possible outputs of the ODR_auto block are:

a) 00: sampling rate equal to 8 kHz (MCLK/WCLK = 1536)

b) 01: sampling rate equal to 16 kHz (MCLK/WCLK = 768)

c) 10: sampling rate equal to 24 kHz (MCLK/WCLK = 512)

Observing *Figure 6*, it is possible to see, that if a ratio between MCLK and WCLK differ from 1536, 768 and 512, the sampling rate equal to 8 kHz is selected.

4.3 Serial clock (BCLK)

The sole purpose of the serial clock BCLK is to shift the data out of the serial SDOUT port. To this purpose, the TDM interface uses an internal counter that is set to one when the rising edge of the WCLK is detected, and it is reset to zero when the maximum number of BCLK in a WCLK period is reached.

The maximum number of BCLK contained in a WCLK period (cmax input of the TDM in *Figure 6*) can be expressed as a function of both the BCLK and WCLK frequencies, and can be computed using the following equation:

Equation 1

$$cmax = \frac{BCLK}{WCLK} - 1$$

In order to support a serial clock BCLK variable in the range [1024 MHz, 12.288 MHz], and consequently to compute the correct maximum value of the internal TDM counter, two possible solutions can be selected:

- The cmax value at the input of the TDM interface can be computed on the fly employing the *BCLK_AUTO block* (see *Figure 6*), which is able to compute the cmax value using *Equation 1*. This functionality by default is enabled, and can be disabled employing the I²C register ODR_AUTO_EN (*AXES_CTRL_REG (2Fh) bit 0*).
- The TDM cmax can be programmed through the I²C registers *TDM_cmax (24h-25h)*.

4.4 TDM axes mapping

Within one frame, the data signal (DOUT) is divided into multiple segments. We call each segment a slot thereafter in this document.

The data slot width is fixed and equal to 16 bits.

In each slot, data should be left-justified (MSB first).

The number of slots in a WCLK frame can be variable, and it depends on the ratio between BCLK and WCLK. However, as depicted in *Figure 7* and *Figure 8*, only the slots 0,1,2 and 4,5,6 can be used to send accelerometer data, all the others slots are always set in high-impedance.

The mapping between the input data and the TDM output slots is flexible and can be configured through the I²C register mapping (*TDM_CTRL_REG (2Eh) bit 4*) in *Figure 6*.

In particular two possible configurations can be selected:

- Axes data (X,Y,Z) mapped on TDM slots (0,1,2) (mapping = 0)
- Axes data (X,Y,Z) mapped on TDM slots (4,5,6) (mapping = 1)

Figure 7. Axes X, Y, Z mapped to SLOT0, SLOT1, SLOT2

SLOT0	SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7	SLOTN
X-axis	Y-axis	Z-axis	HiZ	HiZ	HiZ	HiZ	HiZ	HiZ

Figure 8. Axes X, Y, Z mapped to SLOT4, SLOT5, SLOT6

SLOT0	SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7	SLOTN
HiZ	HiZ	HiZ	HiZ	X-axis	Y-axis	Z-axis	HiZ	HiZ

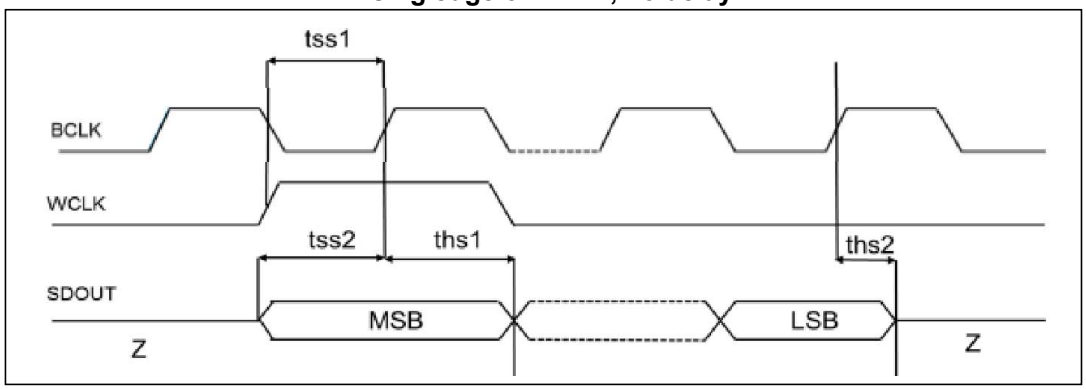
4.5 TDM configurations

In the following subsections all the LIS25BA TDM configurations programmable through the I²C interface will be detailed.

4.5.1 Configuration 1

- No delay: SLOT0 data MSB is sampled on the first rising edge of BCLK after rising edge of WCLK (delayed I²C register *TDM_CTRL_REG (2Eh)* bit 6 equal to zero)
- Data valid: data valid on the rising edge of BCLK (data_valid I²C register *TDM_CTRL_REG (2Eh)* bit 5 equal to zero)

Figure 9. WCLK, SDOUT change on the falling edge of BCLK and are valid on the rising edge of BCLK, no delay

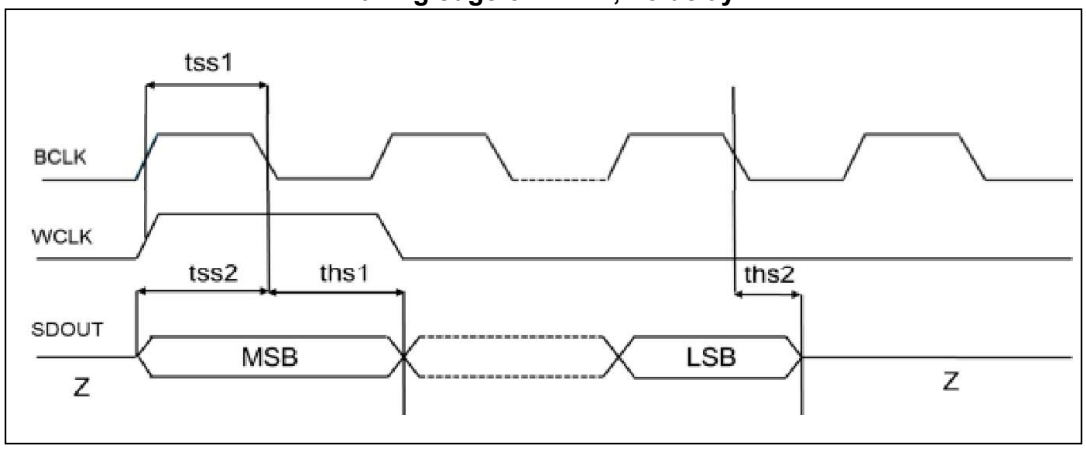


Note: Setup and hold times are defined in Table 6: TDM interface characteristics.

4.5.2 Configuration 2

- No delay: SLOT0 data MSB is sampled on the first falling edge of BCLK after rising edge of WCLK (delayed I²C register *TDM_CTRL_REG (2Eh)* bit 6 equal to zero)
- Data valid: data valid on the falling edge of BCLK (data_valid I²C register *TDM_CTRL_REG (2Eh)* bit 5 equal to one)

Figure 10. WCLK, SDOUT change on the rising edge of BCLK and are valid on the falling edge of BCLK, no delay

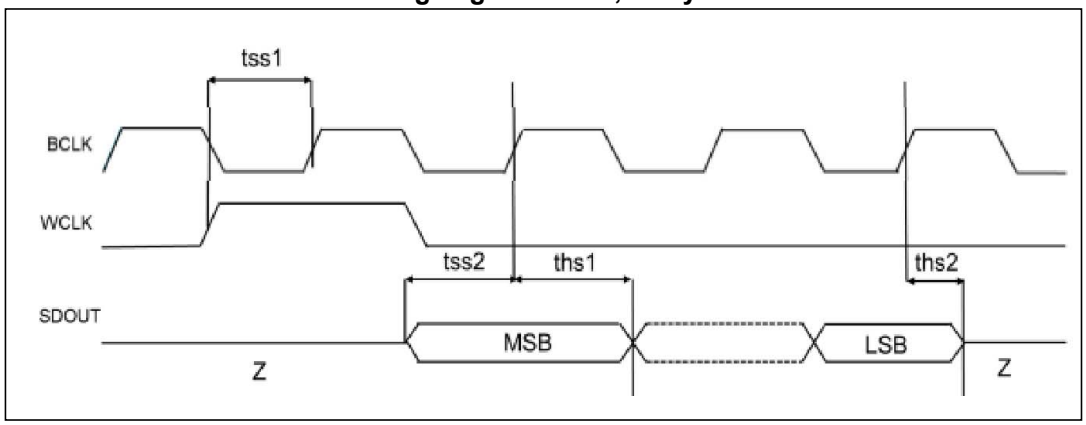


Note: Setup and hold times are defined in Table 6: TDM interface characteristics.

4.5.3 Configuration 3

- Delayed: SLOT0 data MSB is sampled on the second rising edge of BCLK after rising edge of WCLK (delayed I²C register *TDM_CTRL_REG (2Eh)* bit 6 equal to one)
- Data valid: data valid on the rising edge of BCLK (data_valid I²C register *TDM_CTRL_REG (2Eh)* bit 5 equal to zero)

Figure 11. WCLK, SDOUT change on the falling edge of BCLK and are valid on the rising edge of BCLK, delayed

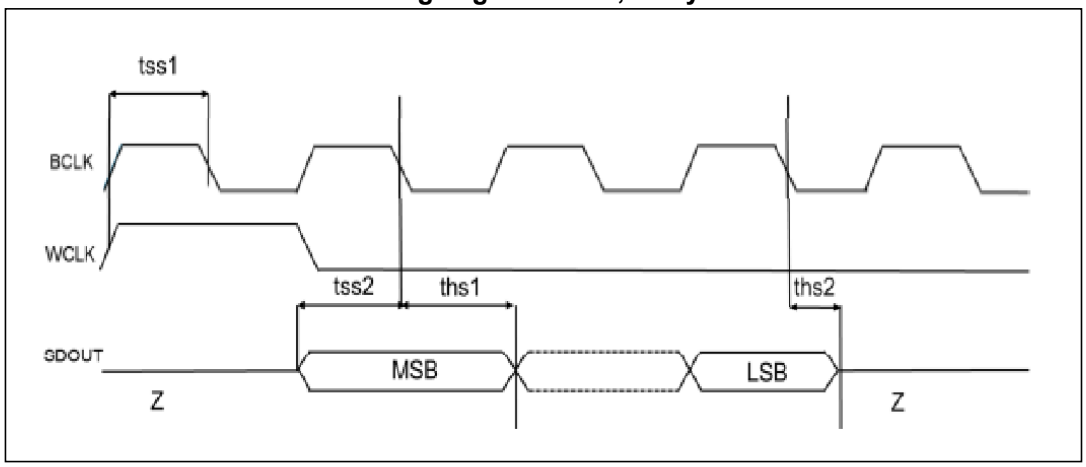


Note: Setup and hold times are defined in Table 6: TDM interface characteristics.

4.5.4 Configuration 4

- Delayed: SLOT0 data MSB is sampled on the second falling edge of BCLK after rising edge of WCLK (delayed I²C register *TDM_CTRL_REG (2Eh)* bit 6 equal to one)
- Data valid: data valid on the falling edge of BCLK (data_valid I²C register *TDM_CTRL_REG (2Eh)* bit 5 equal to one)

Figure 12. WCLK, SDOUT change on the rising edge of BCLK and are valid on the falling edge of BCLK, delayed



Note: Setup and hold times are defined in Table 6: TDM interface characteristics.

4.6 TDM clocks and MCLK requirements

The relationship between TDM clocks and MCLK should be:

- Both BCLK and WCLK must be obtained from MCLK by integer division. This requirement is mandatory since ADC is clocked by MCLK, so the TDM data rate must be perfectly synchronous in frequency and phase with the decimated ADC data rate.
- The BCLK/WCLK ratio must be an integer value.

4.7 I²C axis disable

In TDM mode, a host processor can power down each axis of the LIS25BA accelerometer independently, overriding the I²C registers (AXISX_EN, AXISY_EN, AXISZ_EN in *AXES_CTRL_REG (2Fh)*) interface to reduce power consumption during operation. When an axis is powered down, the corresponding TDM slot will be put in HiZ.

5 I²C- inter-IC control interface

5.1 I²C interface

The registers embedded inside the LIS25BA may be accessed also through the I²C serial interfaces.

Table 10. I²C serial interface pin description

Pin name	Pin description
I2C_SCL	I²C serial clock (SCL)
I2C_SDA	I²C serial data (SDA)

The LIS25BA I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in the table below.

Table 11. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd through an external pull-up resistor. When the bus is free, both lines are high.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

5.2 I²C interface details

The transaction on the bus is started through a START signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH (refer to ST condition in the following paragraph). After this signal has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave (SAD subsequences). When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master. The address can be made up of a programmable part and a fixed part, thus allowing more than one device of the same type to be connected to the I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse (SAK subsequence). A receiver which has been addressed is obliged to generate an

acknowledge after each byte of data has been received. The I²C embedded inside the LIS25BA behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge has been returned (SAK), an 8-bit sub-address will be transmitted (SUB): the 7 LSB represent the actual register address while the MSB enables address auto-increment. If the MSB of the SUB field is '1', the SUB (register address) will be automatically incremented to allow multiple data read/write at increasing addresses. Otherwise if the MSB of the SUB field is '0', the SUB will remain unchanged and multiple read/write on the same address can be performed. If the LSB of the slave address is '1' (read), a repeated START (SR) condition will have to be issued after the sub-address byte; if the LSB is '0' (write) the master will transmit to the slave with direction unchanged.

5.3 I²C slave address

The slave address is equal to 001100yx (TDM mode, where y = not(I2C_A0 pin)) or in case of writing or reading respectively.

5.4 I²C read and write sequences

Previous subsequences are used for the actual write and read sequences described in the tables below.

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant Bit (MSB) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition (SP). Each data transfer must be terminated by the generation of a STOP condition.

6 Features

6.1 Self-test mode

In self-test mode the mechanical element is stimulated by electrostatic force to obtain an equivalent input force applied to the sensor. This equivalent input force applied has to be comparable with the full-scale range in order to have an effective self-test mode.

The self-test mode can be enabled using the I²C interface, setting the ST bit in register *TEST_REG (0Bh)* to '1'.

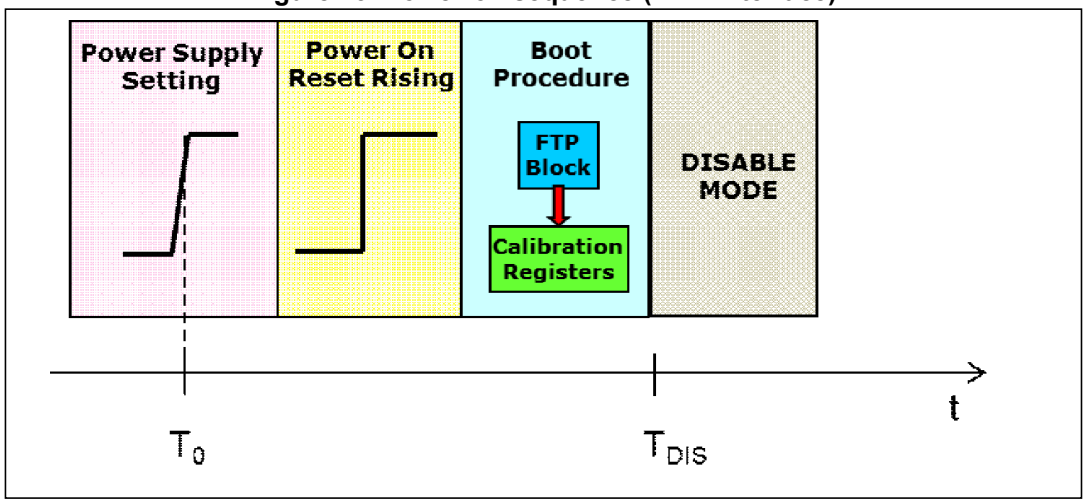
For the self-test values of each axis please refer to *Table 3: Mechanical characteristics*.

6.2 Power cycle/reset information

6.2.1 TDM interface power-on sequence

In TDM, the LIS25BA starts in disabled mode with the following sequence.

Figure 13. Power-on sequence (TDM interface)



In *Figure 13* T_0 represents the time when Vdd reaches 90% of the final value.

After T_{DIS} = 5.5 ms the LIS25BA reaches the disabled mode condition.

The TDM interface must be activated explicitly with I²C configuration. The first 3 samples after the enabling of the TDM may be invalid samples due to the fact that the interface should sync on the external WCLK. The samples will be invalid also after any subsequent Disable-Enable transition that may happen. TDM protocol can be changed on the fly, but also in this case the first 3 samples after the TDM configuration change will be invalid.

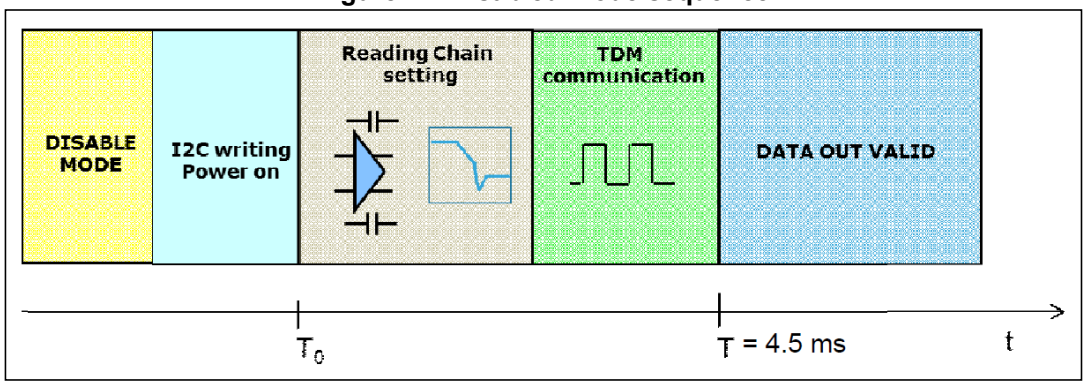
6.2.2 Disabled mode

The LIS25BA can be put in disabled mode using the I²C interface. The power-down command will be executed immediately (no wait state).

The LIS25BA can be resumed from disabled mode using the I²C as well. In this case the MCLK/BCLK/WCLK clocks must be set to the correct values before writing to the I²C.

Please refer to *Figure 14* for the disabled mode sequence.

Figure 14. Disabled mode sequence



7 Register mapping

The table given below provides a list of the 8-bit registers embedded in the device and their respective addresses.

Table 16. Register address map

Name	Type(1)	Register address		Default
		Hex	Binary	
TEST_REG	rw	0B	000 1100	0000 0000
WHO_AM_I	r	0F	000 1111	0010 0000
TDM_cmax[11:8]	rw	24	010 0100	0000 0000
TDM_cmax[7:0]	rw	25	010 0101	0111 1111
CTRL_REG	rw	26	0100110	0010 0000
TDM_CTRL_REG	rw	2E	010 1110	1111 0000
AXES_CTRL_REG	rw	2F	010 1111	1110 0001

1. Read only (r) - read/write (rw)

8 Register description

8.1 TEST_REG (0Bh)

Self-test register (r/w).

Table 17. TEST_REG register

0(1)	0(1)	0(1)	0(1)	ST	0(1)	0(1)	0(1)

1. For proper operation of the device, this bit must be set to '0'.

Table 18. TEST_REG register description

ST	Enables self-test mode. Default value: 0 (0: disabled; 1: enabled)

8.2 WHO_AM_I (0Fh)

Table 19. WHO_AM_I register

0	0	1	0	0	0	0	0

Device identification register.

8.3 TDM_cmax (24h-25h)

TDM counter max value when the BCLK autoconfiguration feature is disabled.

Table 20. TDM_cmax register

-	-	-	-	TDM_cmax[11:8] MSB

TDM_cmax[7:0] LSB

8.4 CTRL_REG (26h)

Control register (r/w)

Table 21. CTRL_REG register

0(1)	0(1)	PD	0(1)	0(1)	0(1)	0(1)	0(1)

1. For proper operation of the device, this bit must be set to '0'.

Table 22. CTRL_REG register description

PD	Device in disabled mode. Default value: 1 (0: Normal mode; 1: Disabled mode: minimum power consumption, I²C still active)

8.5 TDM_CTRL_REG (2Eh)

Table 23. TDM_CTRL_REG register

TDM_pd	Delayed	data_valid	mapping	0(1)	WCLK_fq1	WCLK_fq0	0(1)

1. For proper operation of the device, this bit must be set to '0'.

Table 24. TDM_CTRL_REG register description

TDM_pd	TDM enable. Default value: 1 (0: TDM on; 1: TDM off)
Delayed	TDM delayed configuration. Default value: 1 (0: TDM no delayed configuration; 1: TDM delayed configuration)
data_valid	TDM data valid. Default value: 1 (0: data valid on the rise edge of BCLK; 1: data valid on the falling edge of BCLK)
mapping	TDM mapping. Default value: 1 (0: AXEX --> SLOT0; AXEY --> SLOT1; AXEZ --> SLOT2; 1: AXEX --> SLOT4; AXEY --> SLOT5; AXEZ --> SLOT6)
WCLK_fq [1:0]	TDM clock frequencies. Default value: 00 (00: WCLK = 8 kHz; 01: WCLK = 16 kHz; 10: WCLK = 24 kHz)

8.6 AXES_CTRL_REG (2Fh)

Table 25. AXES_CTRL_REG register

AXISZ_EN	AXISY_EN	AXISX_EN	0(1)	0(1)	0(1)	0(1)	ODR_AUTO_EN

1. For proper operation of the device, this bit must be set to '0'.

Table 26. AXES_CTRL_REG register description

AXISZ_EN	Z-axis enable. Default value: 1 (0: disabled; 1: enabled)
AXISY_EN	Y-axis enable. Default value: 1 (0: disabled; 1: enabled)
AXISX_EN	X-axis enable. Default value: 1 (0: disabled; 1: enabled)
ODR_AUTO_EN	ODR AUTO enable. Default value: 1 (0: ODR and BCLK auto disabled(1); 1: ODR and BCLK auto enabled(2))

1. In this case it is mandatory to set *TDM_CTRL_REG (2Eh)* bits 2 and 1 to match the WCLK sampling rate and *TDM_cmax (24h-25h)* to match the BCLK/WCLK ratio
2. LIS25BA automatically measures the ratio r = MCLK/WCLK. The WCLK frequency is internally determined as FW=12.288 MHz/r. FW will be used to configure automatically the decimation ratio between the ADC and TDM input data rate (same as TDM output data rate) bypassing *TDM_CTRL_REG (2Eh)* bits 2 and 1 configuration. When ODR_AUTO is '1' also the BCLK/WCLK ratio is automatically computed for proper TDM configuration as described in *TDM_cmax (24h-25h)*.

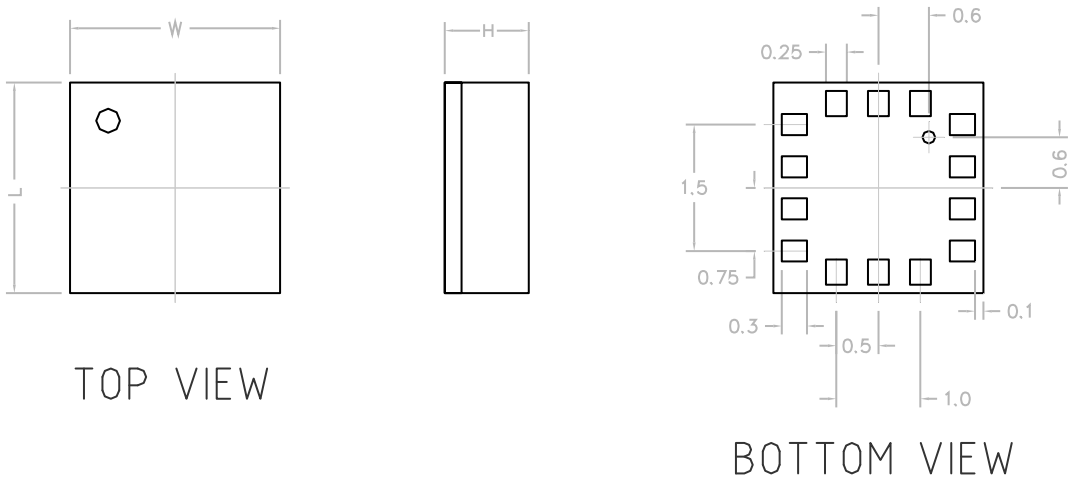
9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

9.1 LGA-14 package information

The LGA-14 package is classified MSL 3.

Figure 15. LGA-14 2.5x2.5x0.86 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	±0.1
Width [W]	2.50	±0.1
Height [H]	0.86	MAX

8535515_A

10 Revision history

Table 27. Document revision history

Date	Revision	Changes
05-Feb-2018	1	Initial release
07-May-2018	2	Document status promoted to production data Updated pin 11 in *Table 2: Pin description* Added footnote *5* to *Table 3: Mechanical characteristics* Updated footnote *3* and *4* of *Table 4: Electrical characteristics* Updated *Section 6.1: Self-test mode* Updated *TEST_REG (0Bh)*, *CTRL_REG (26h)*, and *AXES_CTRL_REG (2Fh)*
24-May-2018	3	Updated bandwidth in *Features* and in *Table 3: Mechanical characteristics* Updated test conditions of IddD1 in *Table 4: Electrical characteristics* Updated *Table 16: Register address map* Updates throughout *Section 8: Register description*