CogniBlox

Hardware User's Manual

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COGNIMEM

Technologies, Inc.

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Contact Information

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B. Getting Started

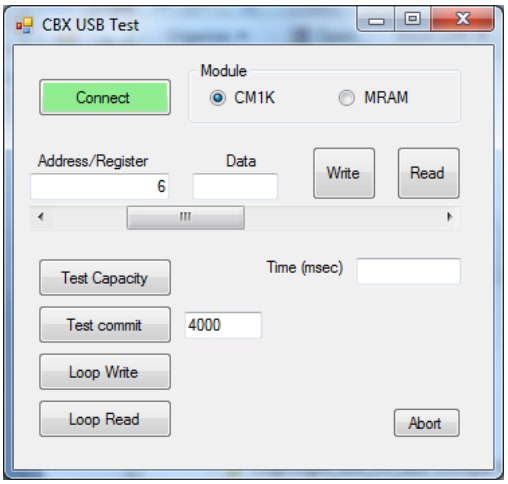
1.B. Configure a single board or a stack of boards

- Single board configuration:
  - pin#7 of SW1 is down
  - pin#8 of SW1 is down
  - pin#8 of SW2 is down
- Multiple boards configuration:
  - All boards → pin#7 of SW1 is up
  - master board → pin#8 of SW1= down
  - slave board → pin#8 of SW1 = up
  - If top or bottom board of a stack → pin#8 of SW2 = down
  - If in-between board of a stack → Pin#8 of the SW2 = up

2.B. Testing a single board or a stack of boards

1 Connect the CogniBlox board to your PC through its USB connector and wait until the new device is detected. Follow the instructions on screen. The FTDI driver is supplied in the folder CBX/USB Drivers.

2 Install the CogniBlox_Diagnostics program. The following panel will appear and the Connect button should be green if the board is properly detected.



3 The default module targets the CM1K chip. Reading the register 6 must return the value 2 at factory settings. For more testing, refer to the technical brief CM1K_Getting_Started_Programmers.pdf. The list of the CM1K registers is supplied in the paragraph "Register Descriptions" of the CM1K Hardware Manual. Examples of Read/Write sequences to learn and recognize a vector are described in the paragraph "Programming Sequences" of the CM1K Hardware manual.

4 Test Capacity automatically commits all the neurons of the four CM1K chips and reads their number back. It should report the value 4096 at the end of the test.

5 Test Commit automatically loads a user-defined number of neurons with random patterns

6 The Loop Write and Loop Read functions execute a user-defined number of read or write instructions and stop if any communication error occurs.

3.B. Programming the board

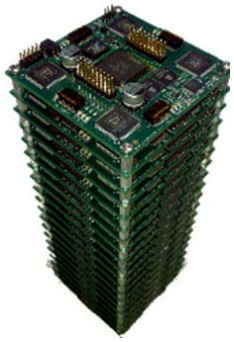
The FPGA can be programmed using Lattice's Diamond software which is available as a download from the Lattice website for both Windows and Linux. Once downloaded and installed, it can be used with either a free license or a subscription license.

The default firmware programmed on the FPGA at factory settings implements a simple Register Transfer Level protocol to access the chain of the four CM1K chips. It is described in the next chapter.

4.B. Examples of applications you can program

4.B.a. Stack of CogniBlox for Data Mining

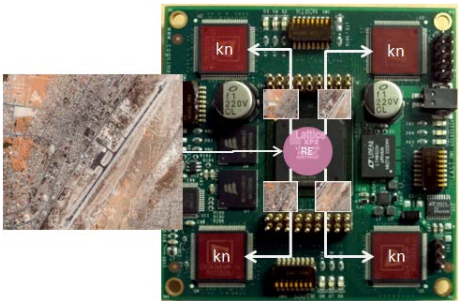
Recognize and classify of vectors against large datasets or knowledge bases.



4.B.b. CogniBlox for Video Analytics

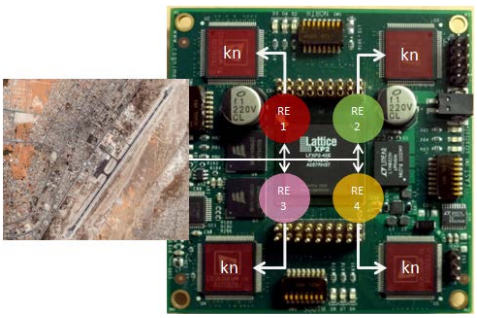
Process images N times faster by distributing the recognition to multiple CM1K chips.

Example1:



The four quadrants of a high resolution image are recognized in parallel by four neural networks (of 1024 neurons or more) loaded with the same knowledge. The latter can be simple and just intended to recognize edges or simple objects, or it can be more complex and composed of neurons assigned to different contexts to build a decision based on multiple features.

Example2:

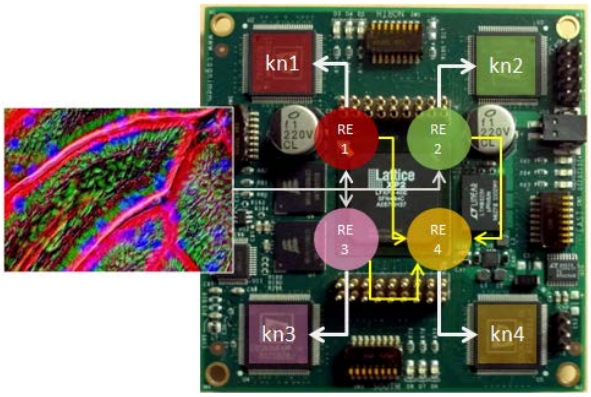


The image is recognized in parallel at four different scales:
Expert at Scale1 (RE1+kn)
Expert at Scale2 (RE2+kn)
Expert at Scale3 (RE3+kn)
Expert at Scale4 (RE4+kn)
The same knowledge is loaded in the four CM1Ks.

4.B.c. CogniBlox for Complex Recognition

Build robust diagnostics using multiple recognition engine and hypothesis generation

Example:

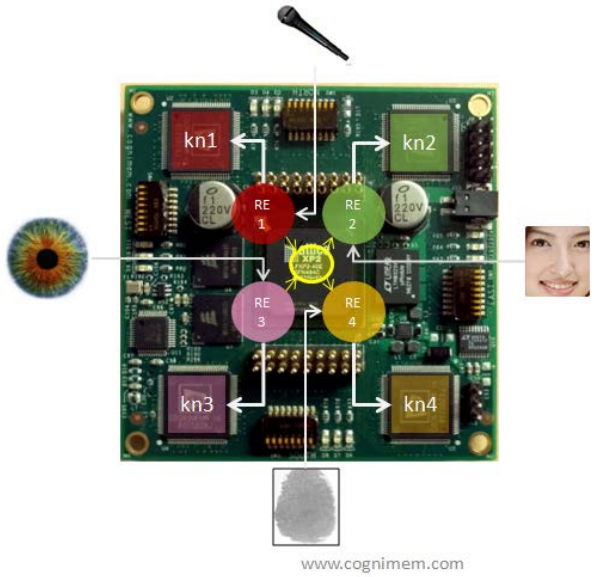


Expert in color (RE1+kn1)
Expert in texture (RE2+kn2)
Expert in shapes (RE3+kn3)
Expert in cell biology (RE4+kn4)

4.B.d. CogniBlox for Sensor Fusion

Multiple sensor inputs (video, sound, accelerometer) for composite recognition.

Example1:

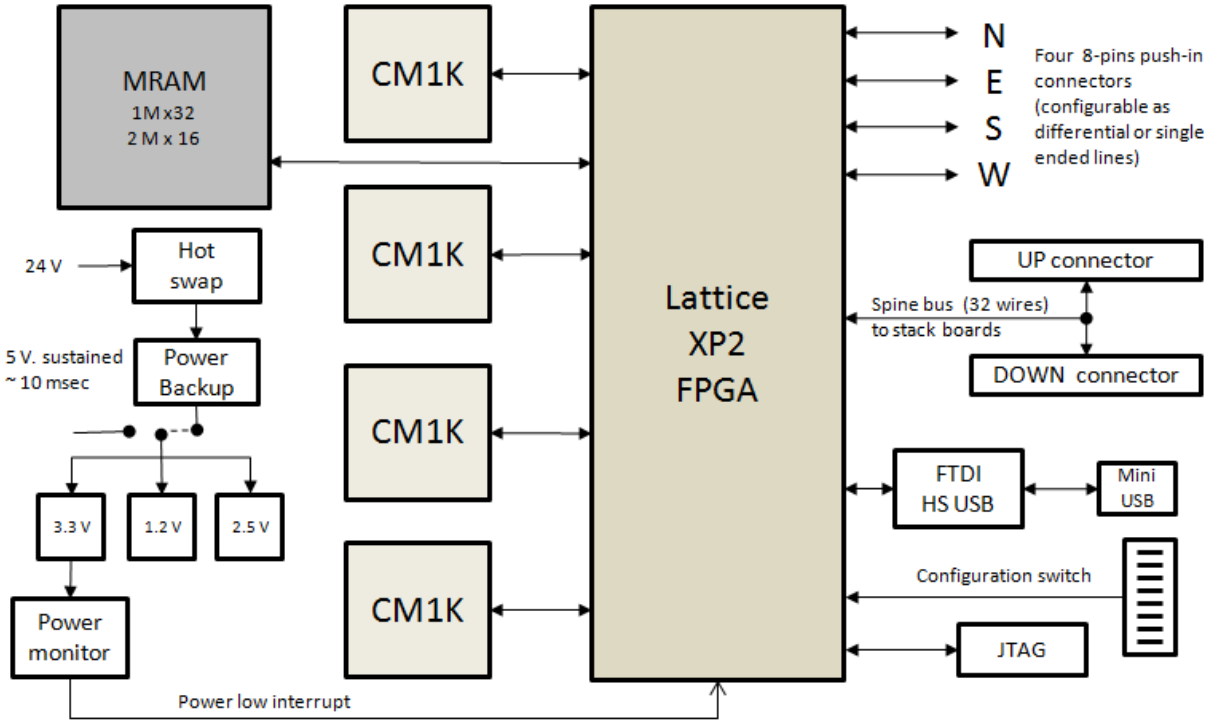


Robust recognition of a person based on its iris and fingerprint and if the person has authorized access to the “appliance” detection of its emotions based on its facial expression and tone of voice.

Expert in voice (RE1+kn1)
Expert in face expression (RE2+kn2)
Expert in fingerprint (RE3+kn3)
Expert in iris(RE4+kn4)

C. Hardware Description

1.C. Overview



1.C.a. Bank of CM1K chips

- 4 CM1K chips with 1024 neurons each
- The four chips can be configured to work independently from one another or to be daisy-chained to build one or multiple networks with more than 1024 neurons. Furthermore, one of the network can also be daisy-chained to additional CM1Ks residing on stacked CogniBlox boards through the spine connector.
- The configuration of the neural networks is defined by the firmware loaded in the FPGA. This firmware can be programmed to implement a single given configuration or to take advantage of the general-purpose switch inputs to define multiple configurations.

i) Examples of possible network configurations for the first board of a stack

CM1K_1		CM1K_2		CM1K_3		CM1K_4		Spine	Description
DCI	**DCO**	**DCI**	**DCO**	**DCI**	**DCO**	**DCI**	**DCO**	**DCI**	
Vcc	Wire1	Wire1	Wire2	Wire2	Wire3	Wire3	N/A		1 network of 4096 neurons (1+2+3+4), non expandable
Vcc	Wire1	Wire1	Wire2	Wire2	Wire3	Wire3	Wire4	Wire4	1 network of 4096 neurons (1+2+3+4), expandable
Vcc	N/A	Vcc	Wire2	Wire2	Wire3	Wire3	N/A		1 network of 1024 neurons (1) and 1 network of 3072 neurons (2+3+4)
Vcc	Wire1	Vcc	Wire2	Wire2	Wire3	Wire3	N/A	Wire1	1 network of 1024 neurons (1) expandable and 1 network of 3072 neurons (2+3+4)
Vcc	N/A	Vcc	Wire2	Wire2	Wire3	Wire3	Wire4	Wire4	1 network of 1024 neurons (1) and 1 network of 3072 neurons (2+3+4) expandable
Vcc	Wire1	Wire1	N/A	Vcc	Wire3	Wire3	N/A		1 network of 2048 neurons (1+2) and 1 network of 2048 neurons (3+4)
Vcc	Wire1	Wire1	Wire2	Vcc	Wire3	Wire3	N/A	Wire2	1 network of 2048 neurons (1+2) expandable and 1 network of 2048 neurons (3+4)
Vcc	Wire1	Wire1	N/A	Vcc	Wire3	Wire3	Wire4	Wire4	1 network of 2048 neurons (1+2) and 1 network of 2048 neurons (3+4) expandable

1.C.b. Field Programmable Gate Array

- Lattice XP2 FPGA with 40,000 logic elements (Model LFXP2-40E, BGA 484 balls)
- Programmable through a JTAG connector, USB connector or 2 SPI lines.

1.C.c. Bank of MRAMs

- Two 2 Mbytes (2M x16bits) MRAM, 35 ns access time

1.C.d. FTDI USB chip

The FT232H is a single channel USB 2.0 Hi-Speed (480Mb/s) to UART/FIFO IC. It has the capability of being configured in a variety of industry standard serial or parallel interfaces.

It must be configured as a single channel synchronous 245 FIFO hardware interface mode (FT245) and interfaces through a Virtual Com port or D2XX Direct driver.

2.C. Connectivity and I/Os

2.C.a. Power supply

- A single CogniBlox can be powered through its USB power supply, otherwise you will need to use an external 24v power supply.
- The 24v power supply is connected to a hot swap circuitry.
    - In case of power shut down, the power backup time lasts approximately 5 ms and is generous enough to allow saving the contents of the neurons to the MRAM provided that this feature is programmed in the firmware of the FPGA.

i) 5V Source Select (J13)

This jumper requires a jumper connector to be present in order for power to be delivered to the board. A Jumper across 1-2 sources power to the card from the USB connector (single board configuration only). A jumper across 2-3 sources power from the on board 24V to 5V Regulator.

Pin #	Pin Name
1	VBUS
2	5V
3	VOUT

ii) 24V Source Connector (J10)

This header is a poke-home connector for connecting the board to an external 24v power supply. Insert strip wires into the bottom portion of the connector as described in the table below. To release the wires, you will need push a small wire in the upper holes of the connector.

Pin #	Pin Name
1 (+)	24V
2 (-)	Ground

2.C.b. Spine connectors

- The spinal connectors enable the vertical stack ability of the CogniBlox modules and the expansion of the neural network by connecting the CM1K chips from multiple boards on a same parallel bus.
- The top side connectors are 2 “spinal” spring-loaded 18-pin connectors. The bottom side connectors are simple pads mirroring the top connectors, except for the daisy-chain in (DCI) signal of J8 which becomes the daisy-chain out (DCO) signal on J6.

Warning: If you probe the signals of the spinal connectors J6 and J8, DO NOT short pins 1 and 2 which are the 24v VCC lines.

i) Spine connector North Top (J5)

Pin #	Pin Name	Pin Name	Pin Number
1	CMB_D00	CMB_D08	2
3	CMB_D01	CMB_D09	4
5	CMB_D02	CMB_D10	6
7	CMB_D03	CMB_D11	8
9	CMB_D04	CMB_D12	10
11	CMB_D05	CMB_D13	12
13	CMB_D06	CMB_D14	14
15	CMB_D07	CMB_D15	16
17	Ground	Ground	18

ii) Spine connector North Bottom (J7)

Pin #	Pin Name	Pin Name	Pin Number
1	CMB_D00	CMB_D08	2
3	CMB_D01	CMB_D09	4
5	CMB_D02	CMB_D10	6
7	CMB_D03	CMB_D11	8
9	CMB_D04	CMB_D12	10
11	CMB_D05	CMB_D13	12
13	CMB_D06	CMB_D14	14
15	CMB_D07	CMB_D15	16
17	Ground	Ground	18

iii) Spine connector South Top (J6)

Pin #	Pin Name	Pin Name	Pin Number
1	24V	24V	2
3	CMB_SP0	CMB_RDY	4
5	CMB_CSn	CMB_CLK	6
7	CMB_BSY	CMB_IDn	8
9	CMB_R0	CMB_UNCn	10
11	CMB_R1	CMB_DS	12
13	CMB_R2	CMB_RWn	14
15	CMB_R3	**CMB_DCO**	16
17	CMB_R4	CMB_RSTn	18

iv) Spine connector South Bottom (J8)

Pin #	Pin Name	Pin Name	Pin Number
1	24V	24V	2
3	CMB_SP0	CMB_RDY	4
5	CMB_CSn	CMB_CLK	6
7	CMB_BSY	CMB_IDn	8
9	CMB_R0	CMB_UNCn	10
11	CMB_R1	CMB_DS	12
13	CMB_R2	CMB_RWn	14
15	CMB_R3	**CMB_DCI**	16
17	CMB_R4	CMB_RSTn	18

2.C.c. General purpose switch (SW1)

The switch SW1 allows defining the configuration and operation of the board through external switch positions, provided that the firmware loaded in the FPGA takes these inputs into considerations.

Pin #	Pin Name	Pin Number	Pin Name
1	Ground	2	*TBD*
3	Ground	4	*TBD*
5	Ground	6	*TBD*
7	Down, Single board Up, Stackable board	8	Down, Master board Up, Slave board
9	Ground	10	*TBD*
11	Ground	12	*TBD*
13	Ground	14	*TBD*
15	Ground	16	*TBD*

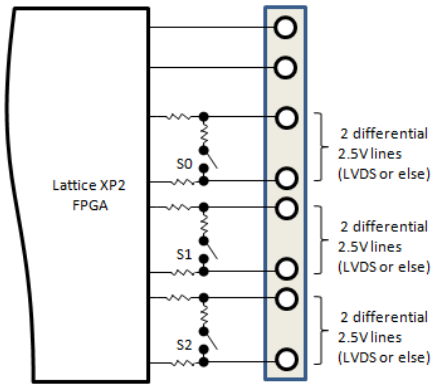
2.C.d. Cardinal connectors and switches

Four configurable “cardinal” connectors allow interfacing the board with sensors and other I/O devices including other CogniBlox boards or stacks. The connector is an 8-pin push-in connector and its electrical properties are defined through an associated dip switch.

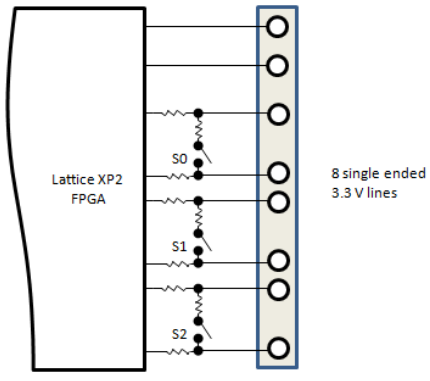
	Connector	Configuration Switch
North	J1	SW2
East	J4	SW5
South	J2	SW3
West	J3	SW4

The switch configuration allows for 3 differential pairs and 2 single-ended wires, or eight single-ended wires:

The differential pairs can be LVDS. They require that the switch between their lines is closed.



The single-ended wires can be used to connect I2C, SPI or other signals.



i) Cardinal Connector

All four cardinal connectors have the following pin assignment:

Pin #	Pin Name
1	User defined, 3.3V
2	User defined, 3.3V
3	User defined, 2.5V
4	User defined, 2.5V
5	User defined, 2.5V
6	User defined, 2.5V
7	User defined, 2.5V
8	User defined, 2.5V

ii) Cardinal Switch

The pin assignment of the four cardinal switches may defer slightly as described in the table below:

Pin #	Pin Name	Pin Name	Pin #
1	3.3V	I2C_SDA	2
3	3.3V	I2C_SCL	4
5	S0	S0 [2]	6
7	S1 (2)	S1 [1]	8
9	S2	S2	10
11	No Connect	No Connect	12
13	No Connect	No Connect	14
15	No Connect	No Connect	16

[1] On the North switch (SW2) pin#8 is reserved to define if the pull-up resistors shall be enabled or not. Pin#8 must be down for the bottom and top boards of a stack.
[1] On the West switch (SW4) pin#8 is reserved to define the boot configuration of the FPGA
[2] On the North switch (SW2) pin#6-7 are reserved to enable the future programming of the FPGA via a USB connection without the need for a Lattice programming cable.

2.C.e. JTAG (J9)

- JTAG to program and debug the FPGA

Pin #	Pin Name	Pin Name	Pin #
1	JTAG_TDI	VCC (3.3V)	2
3	JTAG_TDO	No Connect	4
5	JTAG_TCK	No Connect	6
7	JTAG_ TMS	No Connect	8
9	JTAG_TRST	Ground	10

2.C.f. LEDs

Four sets of three LEDS are placed along the four edges of the board. Their functionality of defined by the firmware programmed on the board.

3.C. Default settings summary

- Single board configuration:
    - pin#7 of SW1 is down
    - pin#87of SW1 is down
    - pin#8 of SW2 is down
- Multiple boards configuration:
    - All boards → pin#7 of SW1 is up
    - master board ➔ pin#8 of SW1= down
    - slave board ➔ pin#8 of SW1 = up
    - If top or bottom board of a stack ➔ pin#8 of SW2 = down
    - If in-between board of a stack ➔ Pin#8 of the SW2 = up

D. Firmware at Factory Default

At factory settings, the board is programmed with a simple USB protocol to read and write data to registers or addresses of modules instantiated in the FPGA. The only module instantiated at first is the controller of the chain of 4 CM1K chips residing on the board.

1.D. Address Mapping

The default modules instantiated in the board are accessible through the following 32-bit address map:

Address Range	**Module=** Address[30-24]	**Functionality defined by registers =** Address[23:8]
0x01000000 0x0100001F	CogniMem 0x01 (d01)	Access to the CM1K neurons to learn and recognize vectors, save and restore knowledge. Also access to the recognition logic in bypass and video mode.
0x10000000 0x0100001F	MRAM 0x10 (d16)	Not yet implemented
TBD	More to come…	

2.D. USB communication protocol

The communication protocol programmed in the FPGA of the V1KU board is based on the following packet sequence:

2.D.a. Write protocol

Reserved	Address[31:0]			Data length[23:0]	Data
0x00	Bit 31=1	Module[6:0]	Register[24:0]	Size of the input array **expressed in words**	Input array
1 byte	1 byte		3 bytes	3 bytes	Data length *2 bytes

2.D.b. Read protocol

Reserved	Address[31:0]			Data length[23:0]	Data
0x00	Bit 31=0	Module[6:0]	Register[24:0]	Size of the output array **expressed in words**	Output array
1 byte	1 byte		3 bytes	3 bytes	Data length *2 bytes

3.D. Examples

The following examples used dummy modules and registers numbers.

i) Single Read

Read the register 5 of the module 4 Data is returned into 2 bytes or a word	0x00 04 00 00 05 00 00 01

ii) Single Write

Write the 16-bit value 0x33AA to the register 5 of the module 4	0x00 84 00 00 05 00 00 01 33 AA

iii) Multiple Read

Read 8 consecutive byte values starting at the address 0x234567 of the module 0x02 Data is returned into 8 bytes.	0x00 02 23 45 67 00 00 04

iv) Multiple Write

Write 4 consecutive byte values 9,8,7,6 starting at the address 0x234567 of the module 0x02	0x00 82 23 45 67 00 00 02 09 08 07

4.D. CogniMem controller

The CogniMem controller is the module 0x01. It transmits and receives data to and from the chain of CM1K chips residing on the board and possibly extending to the CM1K chips of additional boards stacked on top of this master board.

4.D.a. Command and control lines

DS	Data strobe line
RW_	Read/Write line (default is Read with RW_=1)
REG	5 bit register address
DATA	16-bit register data
RDY	Ready control line mixing the ready output signal of all the neurons in the chain and indicating that the neurons are all ready to execute a new command
ID_	Control line mixing the ready output signal of all the neurons in the chain and indicating that neurons have identified the last vector and that these neurons are all in agreement for its classification.
UNC_	Control line mixing the ready output signal of all the neurons in the chain and indicating that neurons have identified the last vector but that these neurons are in disagreement with its classification. This line is an in/out line because used as an input during the execution of certain Write register.

All the neurons of the CM1K chips sample a new command on the positive edge of the system clock and pull down their RDY line for the duration of its execution. Upon completion, the RDY line is pulled back up on the positive edge of the system clock.

A Write command (DS, RW_=0, REG, DATA) must be stable on the positive edge of the system clock and released before the next positive edge of the system clock.

A Read command (DS, RW_=1, REG) must be stable on the positive edge of the system clock and released before the next positive edge of the system clock. DATA is stable when the RDY control line is pulled high.

4.D.b. Registers

For more information about the CogniMem registers and programming examples, refer to the CM1K hardware user's manual and the CogniMem technology Reference Guide.

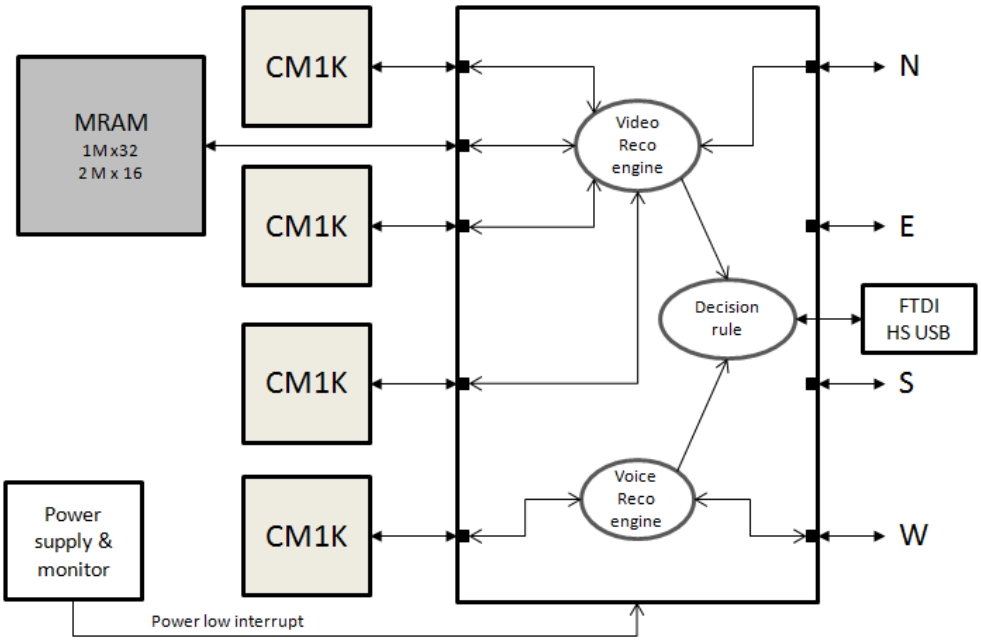
Register	Hex	Description	Default	Access
CM_NCR	0x00	Neuron Context	0	R/W in SR mode
CM_COMP	0x01	Component	0	W, R/W in SR mode
CM_LCOMP	0x02	Last Component	0	W, R/W in SR mode
CM_INDEXCOMP	0x03	Component Index	0	W
CM_DIST	0x03	Distance	0xFFFF	R
CM_CAT	0x04	Category	0xFFFF	R/W
CM_AIF	0x05	Active Influence Field	0x4000	R/W in SR mode
CM_MINIF	0x06	Minimum Influence Field	2	R/W
CM_MAXIF	0x07	Maximum Influence Field	0x4000	R/W
CM_NID	0x0A	Neuron identifier	0	R
CM_GCR	0x0B	Global Norm and Context	1	W
CM_RESET CHAIN	0x0C	Point to the 1st neuron in SR mode		W
CM_NSR	0x0D	Network Status Register	0	R/W
CM_FORGET	0x0F	Clear the neuron registers, the Minif, Maxif and GCR global registers. Does NOT reset the NSR register.		W
CM_NCOUNT	0x0F	Return the number of committed neurons		R
CM_RSR	0x1C	Recognition Status Register	0	R/W
CM_RTDIST	0x1D	Real-Time distance	0xFFFF	R
CM_RTCAT	0x1E	Real-Time category	0xFFFF	R
CM_LEFT	0x11	Left position of the ROI	200	R/W
CM_TOP	0x12	Top position of the ROI	120	R/W
CM_NWIDTH(1)	0x13	Width of the ROI	340	R/W
CM_NHEIGHT(1)	0x14	Height of the ROI	220	R/W
CM_BWIDTH(1)	0x15	Width of the inner block	20	R/W
CM_BHEIGHT(1)	0x16	Height of the inner block	20	R/W
CM_ROIINIT	0x1F	Reset the ROI to default		W

E. Examples of CogniBlox firmware architecture

1.E. Combined vision and sound recognition

In the following example, a video recognition engine receives input from a camera on the North bus and interfaces to a chain of 3 CM1Ks to the recognize the contents of the video frames. The output is transferred to a decision rule shared with the Voice recognition engine.

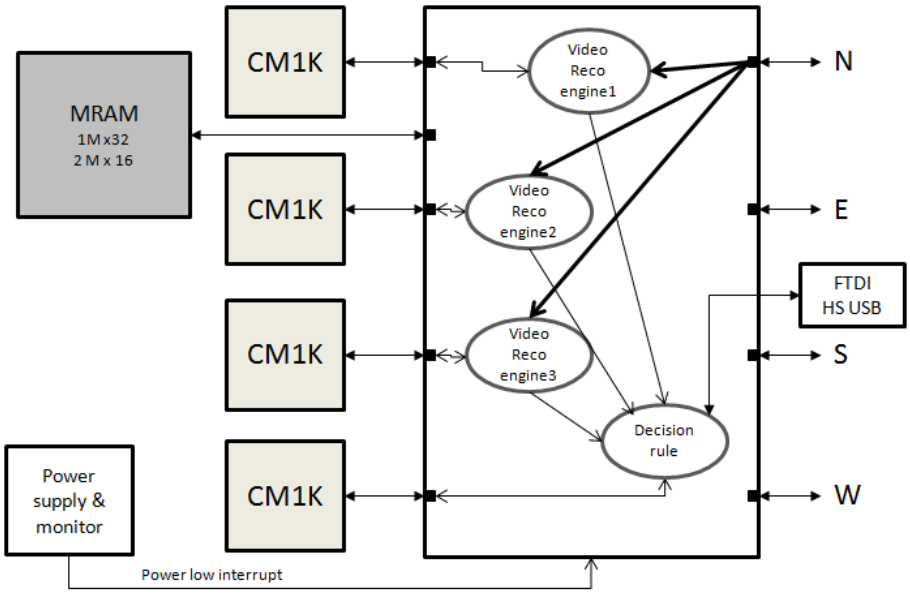
A voice recognition engine receives input from a microphone on the West bus and interfaces to a single CM1K to the recognize a voice. The output is transferred to a decision rule shared with the Video recognition engine.



2.E. Multi scale image recognition

In the following example, the same video signal received on the North bus is transmitted to three different Video Recognition engines which are each interfaced to their own CM1K chip. These engines can be designed to recognize the video frames at different scales, or with different feature extraction methods, or with different regions of search, etc.

The outputs of the three engines are transmitted to a decision rule engine which assembles them into a feature vector and uses a CM1K chip to classify this vector as a global response.



F. Mechanical and Electrical Specifications

Power supply: 24v
Power consumption: 50 mA per board

G. Schematics Overview