Octal Multiprotocol Switch

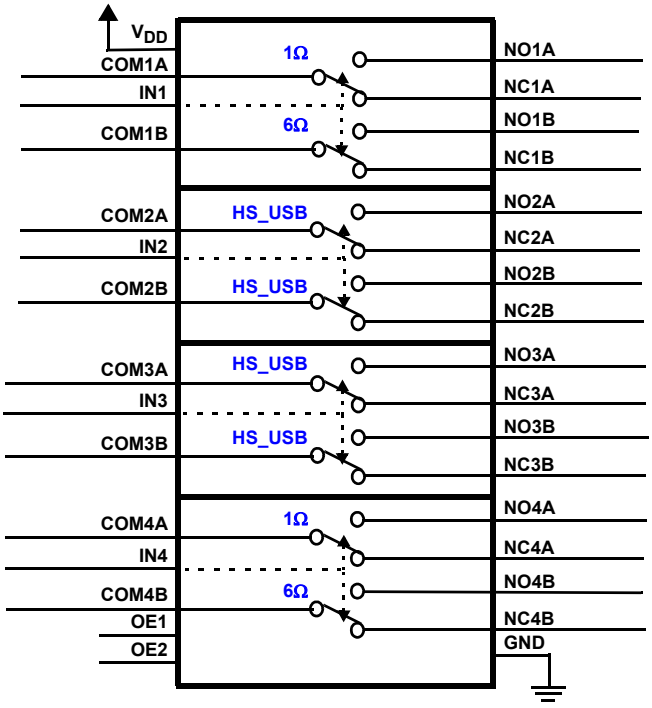
The Intersil ISL54230 is a multiprotocol Quad Double-Pole Double-Throw (DPDT) analog switch that can operate from a single +2.0V to +5.5V supply. It contains eight SPDT (Single Pole/Double Throw) switches configured into four DPDT blocks. Each DPDT block is independently controlled by a logic input for Normally Open (NO) or Normally Closed (NC) switch configuration.The part is designed for switching or routing a combination of USB High-Speed, USB Full-Speed, digital, and analog signals in portable battery powered products.

The digital inputs are 1.8V logic compatible when operated with a 2.7V to 3.6V supply. The ISL54230 has two switch enable pins to disable certain blocks of the switch. The ISL54230 is available in a 36 ball 2.5mmx2.5mm WLCSP or a 32 Ld TQFN 5mmx5mm package. It operates over a temperature range of -40 to +85°C.

Applications

- Cellular/Mobile Phones
- PDAs
- Digital Cameras and Camcorders
- USB/UART/Audio Switching

Block Diagram



Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0
- Compliant with USB 2.0 Short Circuit and Overvoltage Requirements Without Additional External Components
- 1.8V Logic Compatible (+2.7V to +3.6V Supply)
- Switch Terminals Overvoltage Protected Up to +5.5V
- Enable Pin to disable Switch Blocks
- Two DPDT 1Ω/6Ω Switches
- Two DPDT USB 2.0 FS/HS Capable Switches
- USB Switch Low ON Capacitance 12pF
- USB Switch Low ON-Resistance 6Ω
- Single Supply Operation (V_{DD}) . . . . . +2.0V to +5.5V
- Low Power Consumption (P_D) 1µA
- Low I+ Current when V_{INH} is not at the V+ Rail
- Available in 36 Ball WLCSP and 32 Ld 5mmx5mm TQFN Package
- Pb-Free (RoHS Compliant)

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54230IRTZ (Note 1)	54230 IRTZ	-40 to +85	32 Ld 5x5 TQFN	L32.5x5A
ISL54230IRTZ-T* (Note 1)	54230 IRTZ	-40 to +85	32 Ld 5x5 TQFN	L32.5x5A
ISL54230IIZ-T* (Note 2)	230Z	-40 to +85	36 Ball 6x6 Array WLCSP	W6x6.36

*Please refer to TB347 for details on reel specifications.

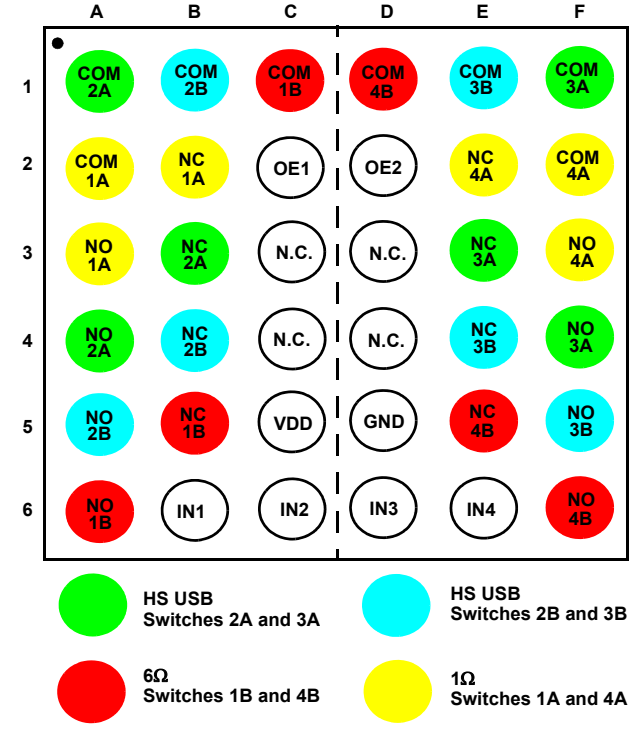
NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free WLCSP and BGA packaged products products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

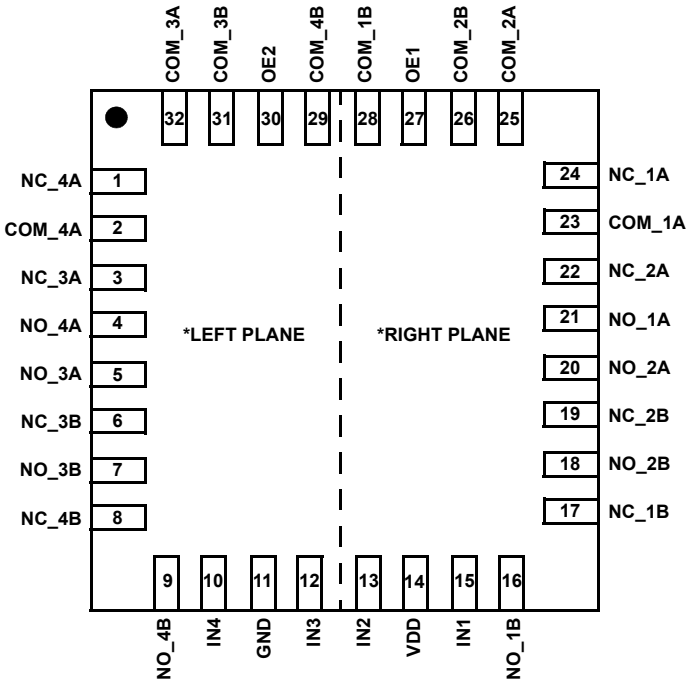
Pinouts

ISL54230
(36 BALL 6X6 ARRAY WLCSP)
TOP VIEW

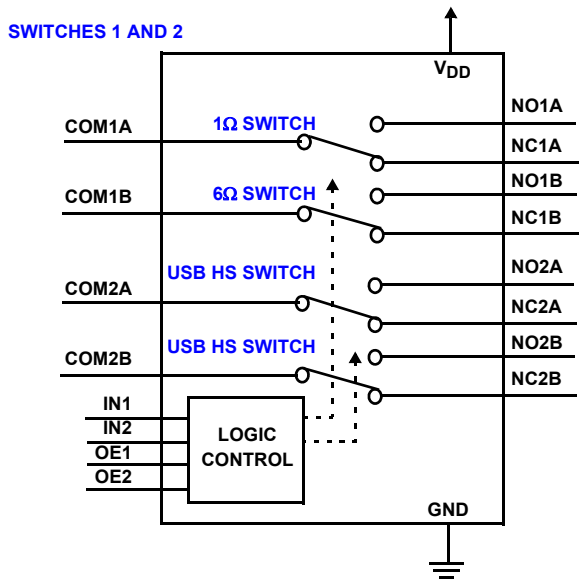
*Columns A, B, C = Left Plane
*Columns D, E, F = Right Plane
*Refer to OE Control Truth Table, pg. 3

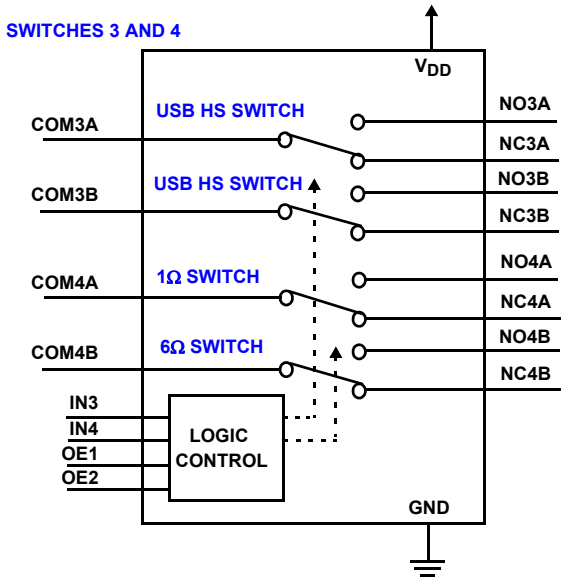


ISL54230
(32 LD 5X5 TQFN)
TOP VIEW



Pinouts





NOTE: Switches shown in Logic “0” position. Logic “0” when INx <0.5V

Input Select Truth Table

INx	NOx	NCx
0	OFF	ON
1	ON	OFF

Logic “0” when ≤ 0.5V, Logic “1” when ≥ 1.4V with a 2.7V to 3.6V Supply.

OE Control Truth Table

OE1	OE2	SWITCH ON	SWITCH OFF	MODE, WLCSP	MODE, TQFN
0	0	COM2x, COM3x	COM1x, COM4x	USB	USB
0	1	COM3x, COM4x	COM1x, COM2x	Right Plane	Left Plane
1	0	COM1x, COM2x	COM3x, COM4x	Left Plane	Right Plane
1	1	ALL	NONE	All On	All On

Logic “0” when ≤ 0.5V, Logic “1” when ≥ 1.4V with a 2.7V to 3.6V Supply.

Pin Descriptions

PIN NAME	COLUMN-ROW WLCSP	PIN NUMBER TQFN	DESCRIPTION
VDD	C5	14	Power Supply Pin
GND	D5	11	Ground Connection
OE1	C2	27	Switch Enable Control 1
OE2	D2	30	Switch Enable Control 2
IN1	B6	15	Switch Input Select 1
IN2	C6	13	Switch Input Select 2
IN3	D6	12	Switch Input Select 3
IN4	E6	10	Switch Input Select 4
COM_1A	A2	23	HS Switch Common 1A
COM_1B	C1	28	HS Switch Common 1B

Pin Descriptions (Continued)

PIN NAME	COLUMN-ROW WLCSP	PIN NUMBER TQFN	DESCRIPTION
COM_2A	A1	25	HS Switch Common 2A
COM_2B	B1	26	HS Switch Common 2B
COM_3A	F1	32	6Ω Switch Common 3A
COM_3B	E1	31	1Ω Switch Common 3B
COM_4A	F2	2	6Ω Switch Common 4A
COM_4B	D1	29	1Ω Switch Common 4B
NC_1A	B2	24	Switch Normally Closed 1A
NC_1B	B5	17	Switch Normally Closed 1B
NC_2A	B3	22	Switch Normally Closed 2A
NC_2B	B4	19	Switch Normally Closed 2B
NC_3A	E3	3	Switch Normally Closed 3A
NC_3B	E4	6	Switch Normally Closed 3B
NC_4A	E2	1	Switch Normally Closed 4A
NC_4B	E5	8	Switch Normally Closed 4B
NO_1A	A3	21	Switch Normally Open 1A
NO_1B	A6	16	Switch Normally Open 1B
NO_2A	A4	20	Switch Normally Open 2A
NO_2B	A5	18	Switch Normally Open 2B
NO_3A	F4	5	Switch Normally Open 3A
NO_3B	F5	7	Switch Normally Open 3B
NO_4A	F3	4	Switch Normally Open 4A
NO_4B	F6	9	Switch Normally Open 4B
N.C.	C3, C4, D3, D4	-	No Connect

Absolute Maximum Ratings

V_{DD} to GND . . . . . -0.3V to +6.5V
Input Voltages
NCx, NOx (Note 3) . . . . . - 0.3V to +6.5V
INx, OEx (Note 3) . . . . . -0.3V to +6.5V
Output Voltages
COMx (Note 3) . . . . . -0.3V to +6.5V
Continuous Current (NC2x, NO3x) . . . . . ±40mA
Continuous Current (NC1x, NO4x) . . . . . ±150mA
Peak Current (NC2x, NO3x)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
Peak Current (NC1x, NO4x)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±300mA
ESD Rating:
Human Body Model . . . . . >8kV
Machine Model . . . . . >400V
Charged Device Model . . . . . >2kV

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld 5x5mm TQFN Package	30	1.5
36 Ball WLCSP Package	60	

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Logic Control Input Voltage . . . . . 0V to V_{DD}
Analog Signal Range . . . . . 0V to V_{DD}

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. Signals on NCx, NOx, COMx, INx, and OEx exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
5. For θ_{JC}, the “case temperature” location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +2.7V, GND = 0V, V_{INxH} = 1.4V, V_{INxL} = 0.5V, V_{OExH} = 1.4V, V_{OExL} = 0.5V, (Note 6), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 8)	TYP	MAX (Notes 7, 8)	UNITS
ANALOG SWITCH CHARACTERISTICS						
USB HS Switch, COM2x and COM3x						
Analog Signal Range, V_{ANALOG}		Full	0	-	V_{DD}	V
ON-Resistance, r_{ON} High Speed	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 40mA, V_{NOx} or V_{NCx} = 0V to 400mV (see Figure 1)	25	-	8.3	-	Ω
		Full	-	9.25	-	Ω
r_{ON} Matching Between Channels, Δr_{ON}, High Speed	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 40mA, V_{NOx} or V_{NCx} = Voltage at max r_{ON}, (Note 10)	25	-	0.11	-	Ω
		Full	-	0.22	-	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$ High Speed	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 40mA, V_{NOx} or V_{NCx} = 0V to 400mV, (Note 9)	25	-	1.45	-	Ω
		Full	-	1.8	-	Ω
ON-Resistance, r_{ON} Full Speed	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 1mA, V_{NOx} or V_{NCx} =0V to 2.7V (see Figure 1, Note 11)	25	-	130	150	Ω
		Full	-	150	178	Ω
r_{ON} Matching Between Channels, Δr_{ON}, Full-Speed	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 1mA, V_{NOx} or V_{NCx} = Voltage at max r_{ON} over signal range of 0V to 2.7V (Note 10)	25	-	1.2	-	Ω
		Full	-	2.6	-	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$ Full-Speed	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 1mA, V_{NOx} or V_{NCx} = 0V to 1V (Note 9)	25	-	4	-	Ω
		Full	-	5	-	Ω
ON-Resistance, r_{ON}	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 1mA, V_{NOx} or V_{NCx} = 0V to 1.8V (see Figure 1)	25	-	128	-	Ω
		Full	-	140	-	Ω
OFF Leakage Current, $I_{NOx(OFF)}$ or $I_{NCx(OFF)}$	V_{DD} = 3.6V, V_{OEx} = Such that switch is disabled, V_{COMx} = 0.3V, 3.3V, V_{NOx} = 3.3V, 0.3V, V_{NCx} = 3.3V, 0.3V	25	-20	4	20	nA
		Full	-100	-	100	nA
ON Leakage Current, $I_{COMx(ON)}$	V_{DD} = 3.6V, V_{OEx} = V_{OExH}, V_{COMx} = 0.3V, 3.3V, V_{NOx} = 0.3V, 3.3V, V_{NCx} = 0.3V, 3.3V	25	-50	4	50	nA
		Full	-100	-	100	nA

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +2.7V, GND = 0V, V_{INxH} = 1.4V, V_{INxL} = 0.5V, V_{OExH} = 1.4V, V_{OExL} = 0.5V, (Note 6), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 8)	TYP	MAX (Notes 7, 8)	UNITS
Power OFF Leakage Current, I_{D+}, I_{D-}	V_{DD} = 0V, V_{NOx} = 0V to 5.25V, V_{NCx}= 0V to 5.25V, V_{INX} = 0V, V_{OEX} such that switch is disabled (see Figure 5)	25	-	2	100	nA
		Full	-	-	2	µA
1Ω Switch, COM1A and COM4A						
Analog Signal Range, V_{ANALOG}		Full	0	-	V_{DD}	V
ON-Resistance, r_{ON}	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 100mA, V_{NOx} or V_{NCx} = 0V to 2.7V (see Figure 1, Note 11)	25	-	1.26	1.5	Ω
		Full	-	1.5	1.74	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 100mA, V_{NOx} or V_{NCx} = Voltage at max r_{ON} over signal range of 0V to 2.7V, (Note 10)	25	-	0.05	-	Ω
		Full	-	0.07	-	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 100mA, V_{NOx} or V_{NCx} = 0V to 2.7V (Note 9)	25	-	0.37	0.52	Ω
		Full	-	0.37	0.6	Ω
ON-Resistance, r_{ON}	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 100mA, V_{NOx} or V_{NCx} = 0V to 1.8V (see Figure 1)	25	-	1.3	-	Ω
		Full	-	1.4	-	Ω
OFF Leakage Current, $I_{NOx(OFF)}$ or $I_{NCx(OFF)}$	V_{DD} = 3.6V, V_{OEx} = V_{OExL}, V_{COMx} = 0.3V, 3.3V, V_{NOx} = 3.3V, 0.3V, V_{NCx} = 3.3V, 0.3V	25	-20	4	20	nA
		Full	-150	-	150	nA
ON Leakage Current, $I_{COMx(ON)}$	V_{DD} = 3.6V, V_{OEx} = V_{OExH}, V_{COMx} = 0.3V, 3.3V, V_{NOx} = 0.3V, 3.3V, V_{NCx} = 0.3V, 3.3V	25	-50	10	50	nA
		Full	-300	-	300	nA
6Ω Switch, COM1B and COM4B						
Analog Signal Range, V_{ANALOG}		Full	0	-	V_{DD}	V
ON-Resistance, r_{ON}	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 40mA, V_{NOx} or V_{NCx} = 0V to 2.7V (see Figure 1, Note 11)	25	-	8	9.2	Ω
		Full	-	9.2	10.8	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 40mA, V_{NOx} or $V_{NC\ x}$= Voltage at max r_{ON} over signal range of 0V to 2.7V, (Note 10)	25	-	0.08	-	Ω
		Full	-	0.3	-	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 40mA, V_{NOx} or V_{NCx} = 0V to 2.7V (Note 9)	25	-	1.9	2.8	Ω
		Full	-	1.9	3.3	Ω
ON-Resistance, r_{ON}	V_{DD} = 2.7V, V_{OEx} = V_{OExH}, I_{COMx} = 40mA, V_{NOx} or V_{NCx} = 0V to 1.8V (see Figure 1)	25	-	8	-	Ω
		Full	-	8.8	-	Ω
OFF Leakage Current, $I_{NOx(OFF)}$ or $I_{NCx(OFF)}$	V_{DD} = 3.6V, V_{OEx} = V_{OExL}, V_{COMx} = 0.3V, 3.3V, V_{NOx} = 3.3V, 0.3V, V_{NCx} = 3.3V, 0.3V	25	-20	4	20	nA
		Full	-100	-	100	nA
ON Leakage Current, $I_{COMx(ON)}$	V_{DD} = 3.6V, V_{OEx} = V_{OExH}, V_{COMx} = 0.3V, 3.3V, V_{NOx} = 0.3V, 3.3V, V_{NCx} = 0.3V, 3.3V	25	-50	4	50	nA
		Full	-130	-	130	nA
DYNAMIC CHARACTERISTICS						
USB HS Switch						
Skew, t_{SKEW}	V_{DD} = 3.0V, V_{OEx} = V_{OExH}, R_L = 45Ω, C_L = 10pF, t_R = t_F = 720ps at 480Mbps, Duty Cycle = 50% (see Figure 6)	25	-	50	-	ps
Total Jitter, t_J	V_{DD} =3.0V, V_{OEx} = V_{OExH}, R_L = 45Ω, C_L = 10pF, t_R = t_F = 750ps at 480Mbps	25	-	210	-	ps
Propagation Delay, t_{PD}	V_{DD} = 3.0V, V_{OEx} = V_{OExH}, R_L = 45Ω, C_L = 10pF (see Figure 6)	25	-	250	-	ps
OFF-Isolation	V_{DD} = 3.0V, R_L = 50Ω, f = 240MHz (see Figure 2)	25	-	-15	-	dB

Electrical Specifications - 2.7V to 3.6V Supply

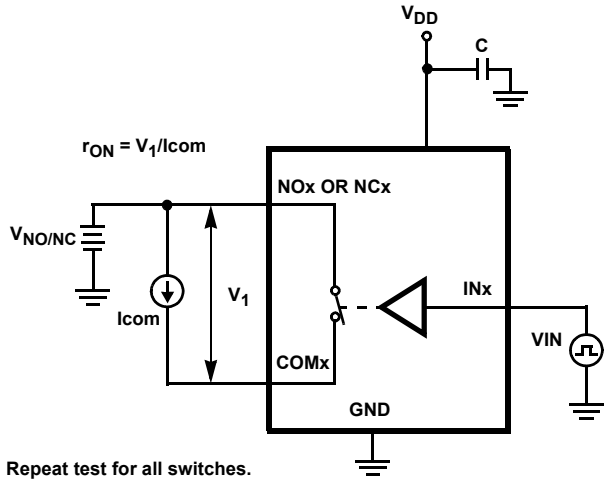
Test Conditions: V_{DD} = +2.7V, GND = 0V, V_{INxH} = 1.4V, V_{INxL} = 0.5V, V_{OExH} = 1.4V, V_{OExL} = 0.5V, (Note 6), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 8)	TYP	MAX (Notes 7, 8)	UNITS
HS Switch -3dB Bandwidth,	Signal = 50mV_{RMS}, R_L = 50Ω	25	-	500	-	MHz
OFF Capacitance, C_{NOxOFF} or C_{NCxOFF}	f = 1MHz, V_{DD} = 3.0V, V_{OEx} = V_{OExH}, V_{NOx} or V_{NCx} = 0V (see Figure 3)	25	-	6.2	-	pF
COM ON Capacitance, C_{COMxON}	f = 1MHz, V_{DD} = 3.0V, V_{OEx} = V_{OExH}, V_{NOx} or V_{NCx} = 0V (see Figure 3)	25	-	12.5	-	pF
1Ω Switches						
Crosstalk	V_{DD} = 3.0V, R_L = 50Ω, f = 10MHz (see Figure 4)	25	-	-90	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 50Ω, f = 1MHz (see Figure 2)	25	-	55	-	dB
Switch -3dB Bandwidth	Signal = 50mV_{RMS}, R_L = 50Ω	25	-	78	-	MHz
OFF Capacitance, C_{NOxOFF} or C_{NCxOFF}	f = 1MHz, V_{DD} = 3.0V, V_{OEx} = V_{OExH}, V_{NOx} or V_{NCx} = 0V (see Figure 3)	25	-	21	-	pF
COM ON Capacitance, C_{COMxON}	f = 1MHz, V_{DD} = 3.0V, V_{OEx} = V_{OExH}, V_{NOx} or V_{NCx} = 0V (see Figure 3)	25	-	61	-	pF
6Ω Switches						
Crosstalk	V_{DD} = 3.0V, R_L = 50Ω, f = 10MHz (see Figure 4)	25	-	-67	-	dB
OFF-Isolation	V_{DD} = 3.0V, R_L = 50Ω, f = 10MHz (see Figure 2)	25	-	50	-	dB
Switch -3dB Bandwidth	50mV_{RMS}, R_L = 50Ω	25	-	310	-	MHz
OFF Capacitance, C_{NOxOFF} or C_{NCxOFF}	f = 1MHz, V_{DD} = 3.0V, V_{OEx} = V_{OExH}, V_{NOx} or V_{NCx} = 0V (see Figure 3)	25	-	6	-	pF
COM ON Capacitance, C_{COMxON}	f = 1MHz, V_{DD} = 3.0V, V_{OEx} = V_{OExH}, V_{NOx} or V_{NCx} = 0V (see Figure 3)	25	-	15	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	2.7		3.6	V
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, V_{OEx} = V_{INx} = 0V, V_{NOx} or V_{NCx} = 0V, V_{COMx} = 0V	25	-	1	2	µA
		Full	-	1.24	-	µA
Power Supply Current, I_{DD}	V_{DD} = 3.6V, V_{Logic} = 1.8V, V_{NOx} or V_{NCx} = 0V, V_{COMx} = 0V. Driving one logic pin only.	25	-	1	-	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INLx}, V_{OELx}	V_{DD} = 2.7V to 3.6V	Full	-	-	0.5	V
Input Voltage High, V_{INHx}, V_{OEHx}	V_{DD} = 2.7V to 3.6V	Full	1.4	-	-	V
Input Current Low, I_{INLx}, I_{OELx}	V_{DD} = 2.7V to 3.6V	Full	-50	20	50	nA
Input Current High, I_{INHx}, I_{OEHx}	V_{DD} = 2.7V to 3.6V	Full	-2	1	2	µA

NOTES:

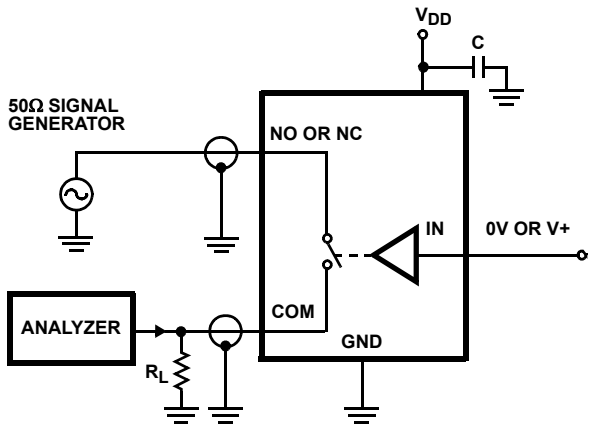
6. V_{logic} = Input voltage to perform proper function.
7. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range
10. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between NCx or NOx.
11. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



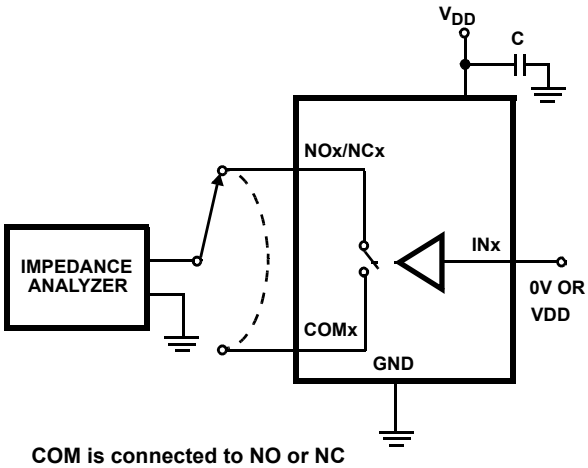
Repeat test for all switches.

FIGURE 1. r_{ON} TEST CIRCUIT



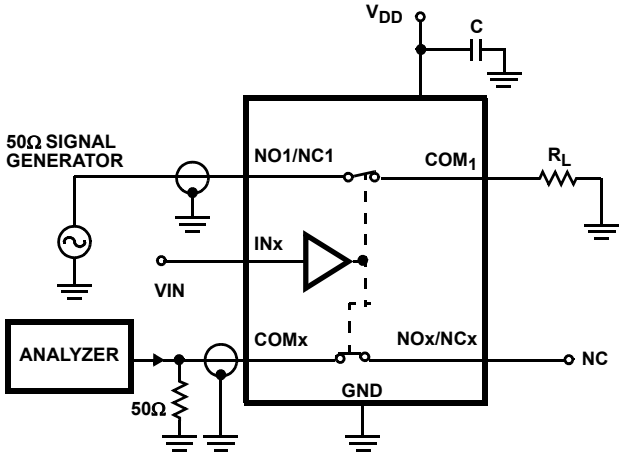
Signal direction through switch is reversed, worst case values are recorded.

FIGURE 2. OFF-ISOLATION TEST CIRCUIT



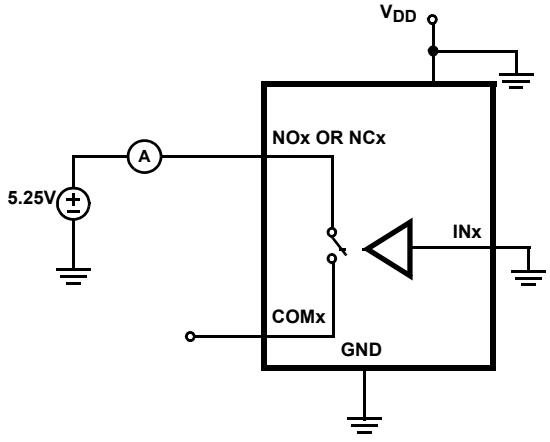
COM is connected to NO or NC during ON capacitance measurement.

FIGURE 3. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 4. CROSSTALK TEST CIRCUIT



NOTE: OEx such that switch is disabled

FIGURE 5. POWER OFF LEAKAGE TEST CIRCUIT

Test Circuits and Waveforms (Continued)

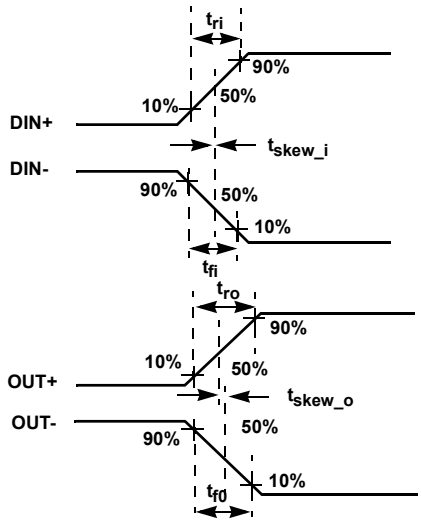
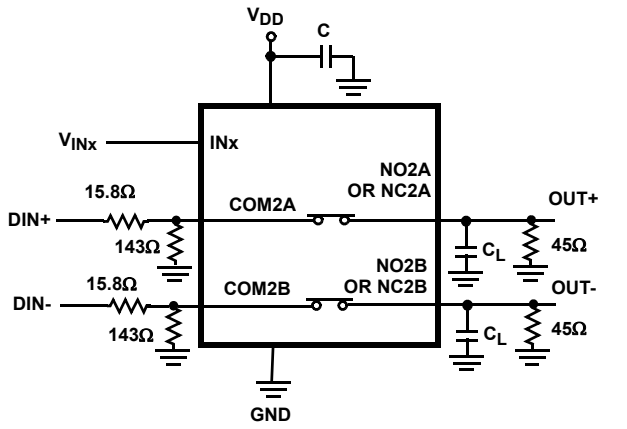


FIGURE 6A. MEASUREMENT POINTS



|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.

|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 6B. TEST CIRCUIT

FIGURE 6. SKEW TEST

Detailed Description

The ISL54230 is a multiprotocol switch containing eight switches configured as a Quad DPDT. Each DPDT switch is independently controlled by a logic pin. The ISL54230 has four switches that are compliant in passing USB2.0 signals and four switches with low r_{ON} that can be used to pass analog or digital signals such as audio or UART. It is offered in a 36 ball WLCSP or a 32 Ld 5mmx5mm TQFN package for applications which require small package size such as cellphones and PDAs.

The ISL54230 contains four switches capable of passing USB2.0 Full-Speed and High-Speed signals with minimal distortion, two 1Ω switches and two 6Ω switches for analog/digital signals. The USB capable switches were designed with low capacitance and high bandwidth to pass USB HS signals (480Mbps) with minimal edge and phase distortion. The 1Ω switches are designed for passing low bandwidth signals (<8MHz) and are ideal for switching power lines since the low ON-resistance minimizes power dissipation. The 6Ω switches are designed to pass audio or data signals up to 100MHz while maintaining a low r_{ON} for good THD performance.

In addition to the four independent logic control pins that control each DPDT switch, the ISL54230 contains two Output Enable (OE) logic pins that permits the IC to disable certain switches giving the user a high degree of flexibility in signal routing. Please see “OE Control Truth Table” on page 3 for an explanation of the OE pins. All logic pins on the ISL54230 are 1.8V logic compatible up to a +3.3V supply.

Power Supply Considerations

The power supply connected to the V_{DD} and GND pins provides the DC bias voltage necessary to operate the IC. The ISL54230 can be operated with a supply voltage in the range of +2.0V to +5.5V. For USB applications, the supply voltage should be in the range of +3.0V to +5.5V to ensure proper signal levels on the USB data lines.

A decoupling capacitor in the range 0.01µF to 0.1µF should be connected to the V_{DD} supply pin of the IC to filter out any power supply noise that may be present on the supply lines. The capacitor should be place as closed as possible to the V_{DD} pin.

Supply Sequencing and Power-On Reset Protection

Proper power supply sequencing is necessary to protect the ISL54230 from operating in fault conditions. The ISL54230 integrates Power-On Reset (POR) circuitry that prevents the switches from turning ON until the supply voltage is at least +1.4V. The POR has a 100mV hysteresis built in that will turn the switches OFF when the supply has gone below +1.3V. This function prevents signals from the switch input being passed to the output when the device operating voltage has not reached appropriate levels yet, protecting the switch from fault conditions.

The POR circuitry also protects the switch from operating in a fault condition should the power supply to the IC drop below the POR threshold. Thus, the recommended operational supply voltage is within +2.0V to +5.5V. Operating at supply voltages below +2.0V may still be functional but the noise margin between the POR threshold and supply voltage will be reduced. The device may

unexpectedly shut down if transient voltages trigger the POR.

Overvoltage and Short Circuit Considerations

The ISL54230 should be protected from overvoltage conditions. The IC contains ESD protection diodes that are back biased from the switch terminals to ground. Negative voltages on the switch terminals that are large enough to forward-bias these ESD protection diodes will result in a large current flowing from ground that may destroy these diodes. Thus, signals on the switch terminals should not swing below ground and cannot exceed the specified "Absolute Maximum Ratings" on page 5 for safe operation.

The ISL54230 can have signals that go above the positive supply rail with no adverse effects up to +5.5V. The ESD protection circuitry permits the signal from going beyond the V_{DD} supply (even with V_{DD} = 0V) without inducing large leakage currents on the switch pins when the supply voltage is less than +5.5V. This feature complies with the USB 2.0 Specifications for short circuit protection in the event that the 5.25V V_{BUS} line shorts to the USB signal lines.

Note: When the supply voltage is above the POR threshold and a V_{BUS} fault conditions occurs, the V_{BUS} signal will be passed to the other side of the switch if the logic control pins are biased such that the switch is turned ON.

USB Switches (COM2x and COM3x)

The four USB FS and HS capable switches are bi-directional analog switches that can pass rail-to-rail signals with minimal distortion. With a 3.0V power supply, these switches have a nominal ON-resistance of 6Ω in the 0V to 400mV signal range. The low capacitance and high bandwidth of the switches makes them ideal for USB applications. They are specifically designed to pass both USB FS (12Mbps) and USB HS (480Mbps) differential signals while meeting the USB 2.0 signal quality eye diagrams (Figures 25 and 26).

The USB switches are designed with integrated protection circuitry for fault conditions as defined in the USB 2.0 Specifications-Section 7.1.1. If a condition where V_{BUS} (5.25V) is shorted to the D+ or D- pin this will not damage the device, even without power to the IC.

1Ω Switches (COM1A and COM4A) and 6Ω Switches (COM1B and COM4B)

The two 1Ω switches are bi-directional analog switches that can pass rail-to-rail signals, making them well suited for analog or digital signal routing. The low ON-resistance of the switches makes them ideal for switching ON/OFF power supply lines for applications that interface with devices that require power (ie: SIM cards or flash memory devices). With a ON-resistance of 1Ω the power dissipation through the switch is minimal.

The two 6Ω switches are bi-directional analog switches that can pass rail-to-rail signals, making them well suited for analog or digital signal routing such as audio, UART or Full-Speed USB.

The low ON-resistance of these switches are well suited for passing audio signals with good THD performance, even with low impedance loads such as 32Ω headphones (see Figure 24 for THD performance curves).

Logic Control Pins

The ISL54230 contains six logic control pins, IN1 through IN4 for independently controlling each DPDT switch and two OE enable pins. The logic control pins determine the state of the switches. Refer to the "Input Select" and "OE Control" Truth Tables on page 3.

When the OEx control pins are logic LOW, only the switches on COM2x and COM3x are active and the switch state determined by IN2 and IN3 respectively. When the OEx control pins are logic HIGH, all switches are active and the switch state determined by the INx control pins.

When the OEx control pins are in opposing logic states either COM1x and COM2x are active or COM3x and COM4x are active depending on what states OE1 and OE2 are at. The active switches are controlled by the respective INx control pin. This feature is useful for applications that interface the ISL54230 to Master/Slave devices or controlling two SIM cards in Dual SIM Card cellphones. The OEx control pins permit total deactivation of each half of the switch blocks to disable devices connected to those switches.

LOGIC CONTROL VOLTAGE LEVELS

OEx = Logic "0" (Low) when $V_{OEx} \leq 0.5V$

OEx = Logic "1" (High) when $V_{OEx} \geq 1.4V$

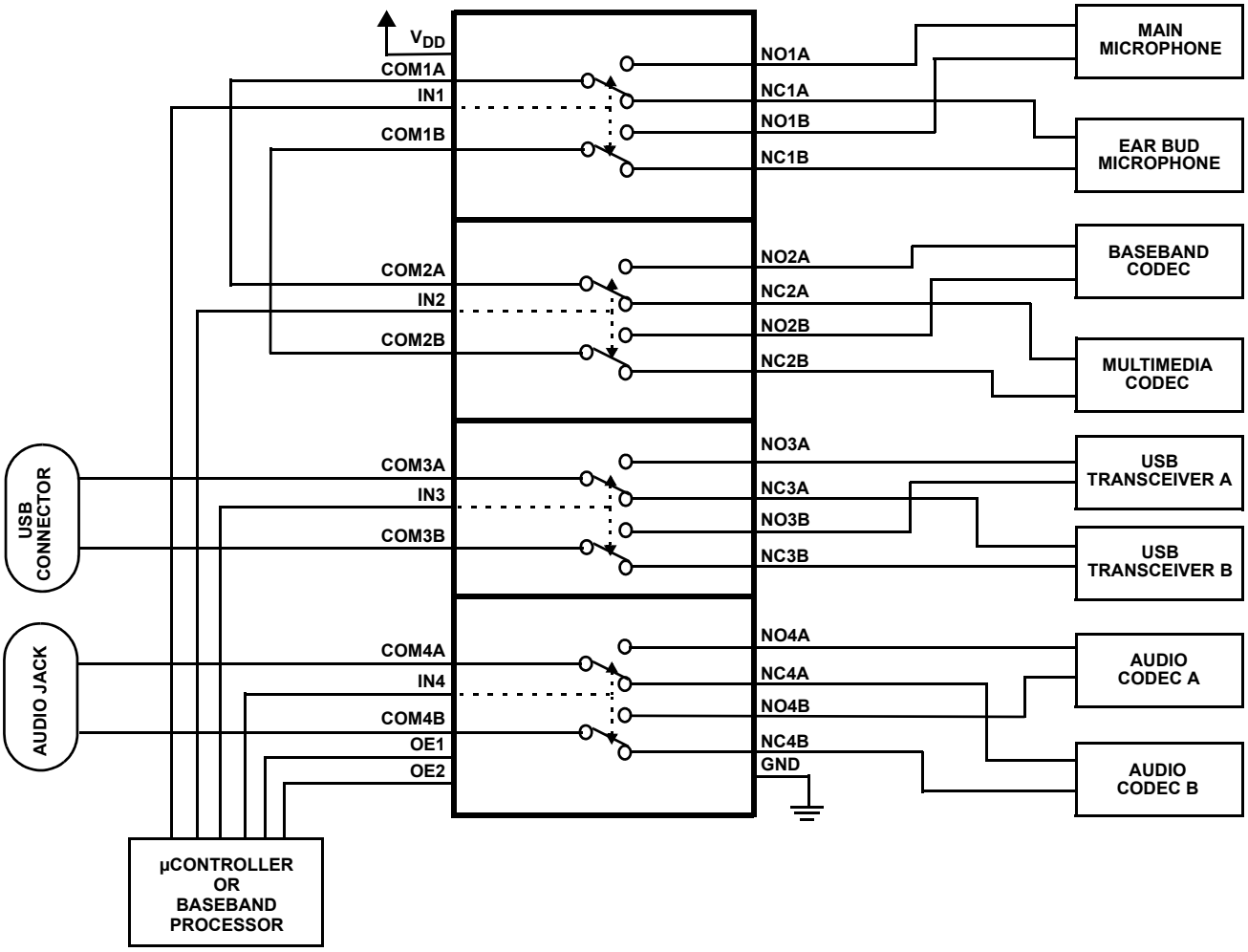
INx = Logic "0" (Low) when $V_{INx} \leq 0.5V$

INx = Logic "1" (High) when $V_{INx} \geq 1.4V$

The logic control pins are +1.8V CMOS logic compatible (0.45V V_{OLMAX} and 1.35V V_{OHMIN}) for supply voltages from +1.8V to +3.6V. over a supply range of 1.8V to 3.3V (see Figure 23). At 3.6V the V_{IL} level is 0.5V maximum. This is still below the 1.8V CMOS guaranteed low output maximum level of 0.45V, but noise margin is reduced. At 3.6V the V_{IH} level is 1.4V minimum. While this is above the 1.8V CMOS guaranteed high output minimum of 1.35V under most operating conditions the switch will recognize this as a valid logic high.

The digital input stages draws a larger supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL54230 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 1.8V logic high while operating with a 3.6V supply the device draws only 1µA of current.

Application Block Diagram



Typical Performance Curves

T_A = +25°C, Unless Otherwise Specified.

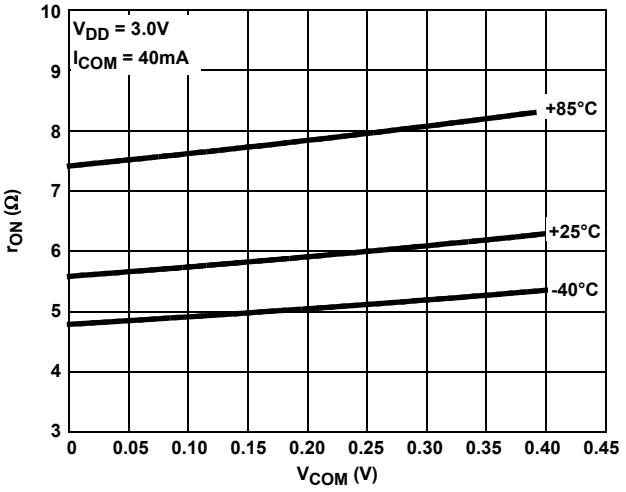


FIGURE 7. ON-RESISTANCE vs SWITCH VOLTAGE; COM2x AND COM3x

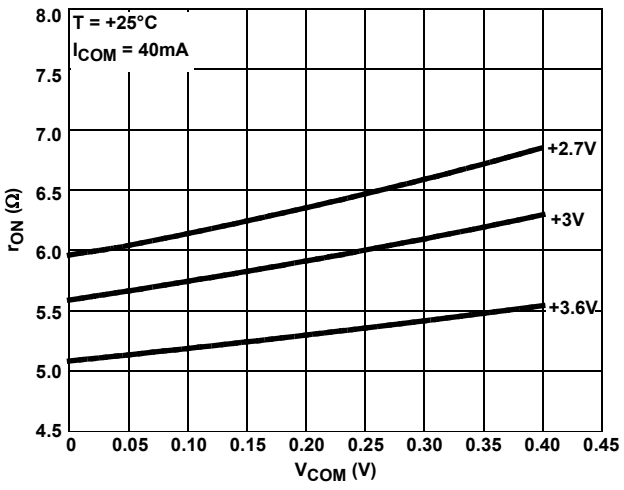


FIGURE 8. ON- RESISTANCE vs SWITCH VOLTAGE; COM2, COM3

Typical Performance Curves

T_A = +25°C, Unless Otherwise Specified. **(Continued)**

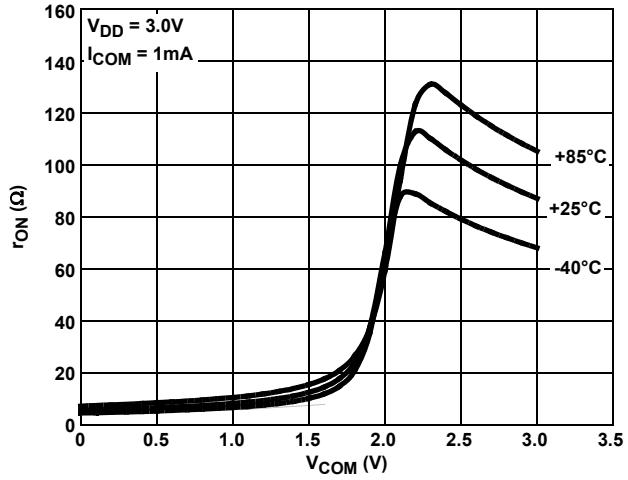


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE; COM2x AND COM3x

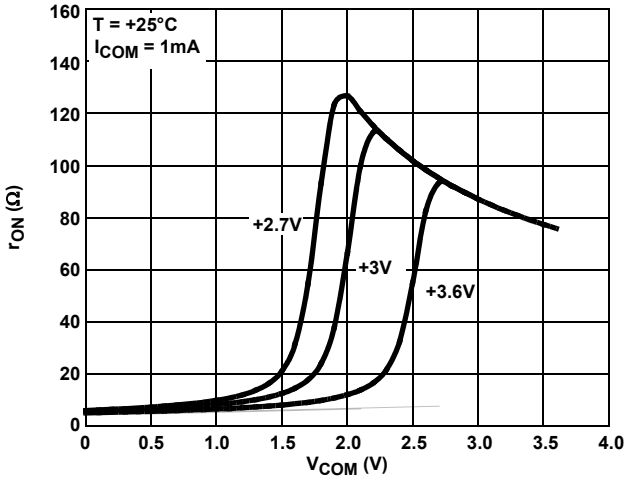


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE; COM2x AND COM3x

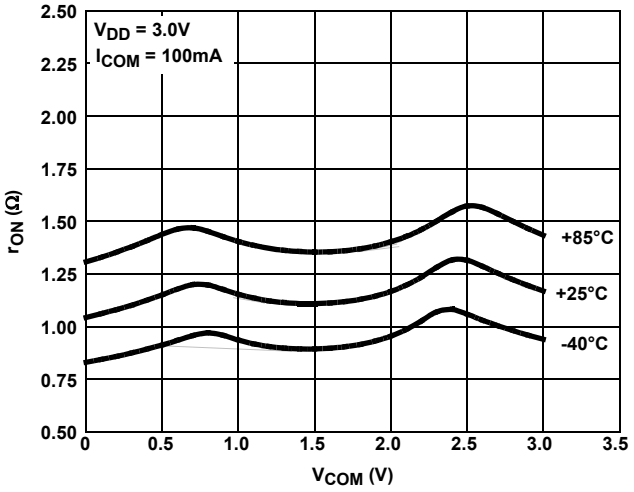


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE; COM1A AND COM4A

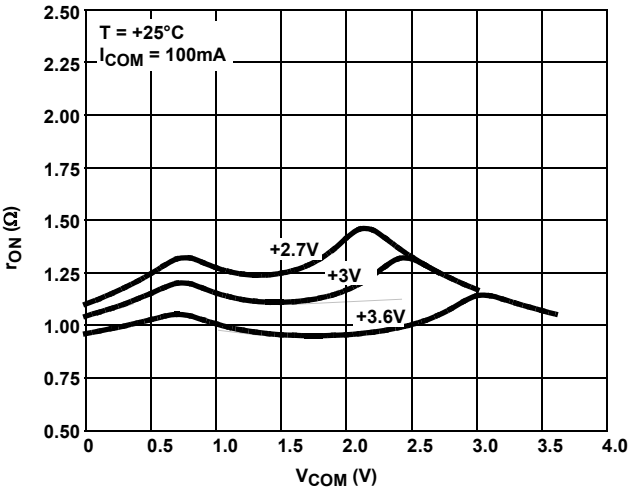


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE; COM1A AND COM 4A

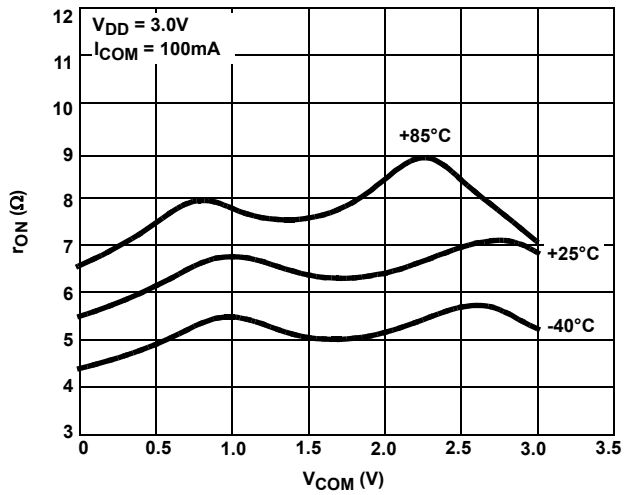


FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE; COM1B AND COM4B

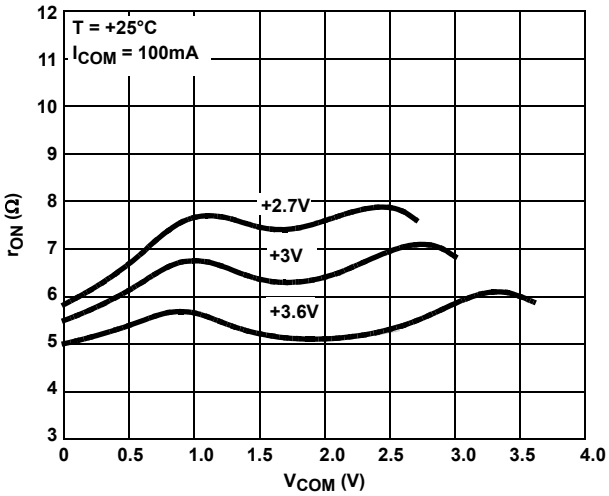


FIGURE 14. ON-RESISTANCE vs SWITCH VOLTAGE; COM1B AND COM4B

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

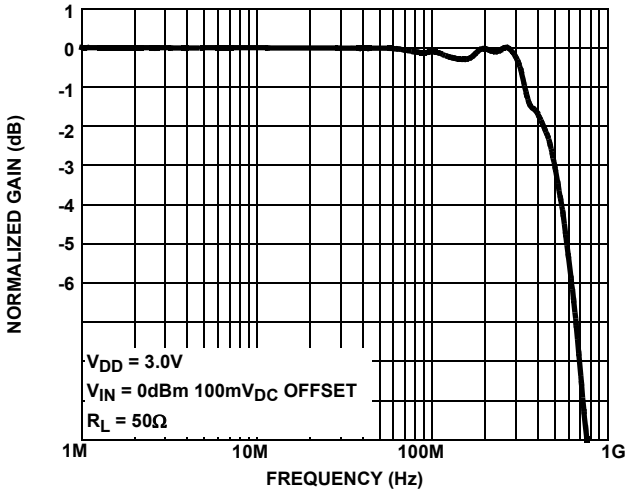


FIGURE 15. FREQUENCY RESPONSE; COM2x and COM3x

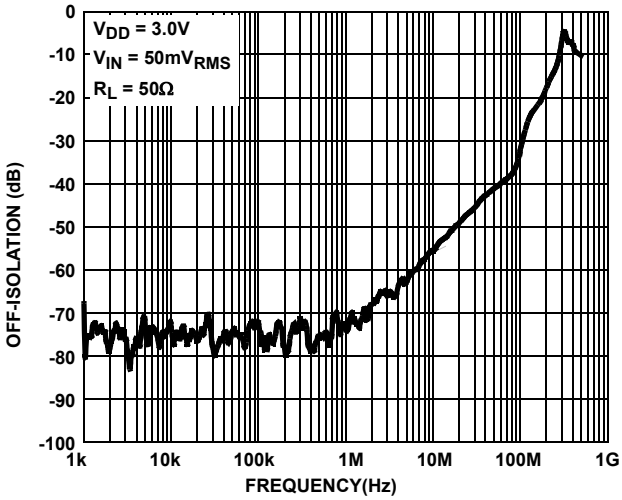


FIGURE 16. OFF-ISOLATION; COM2x and COM3x

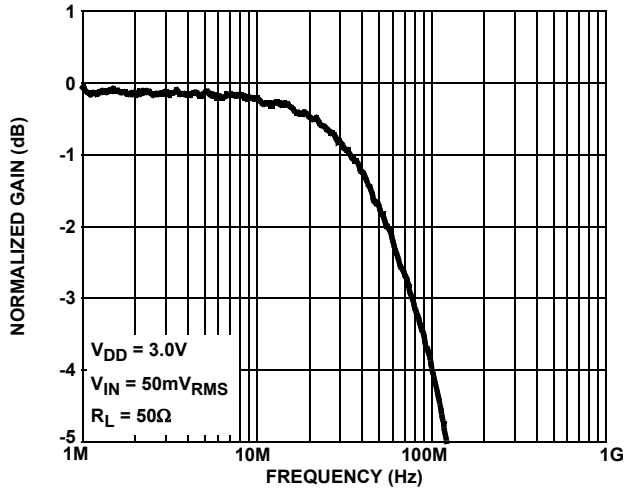


FIGURE 17. FREQUENCY RESPONSE; COM1A AND COM4A

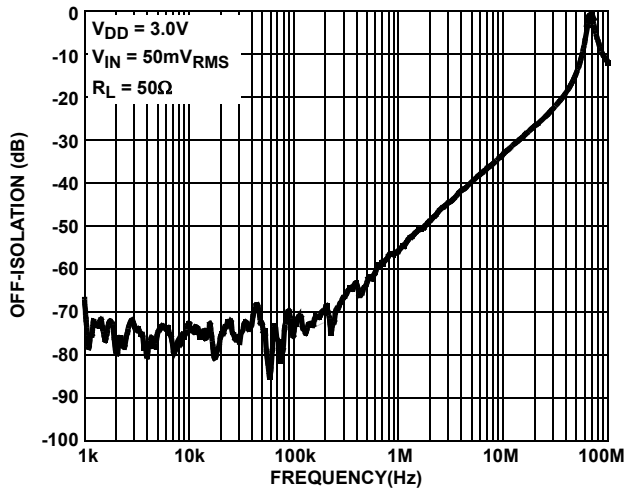


FIGURE 18. OFF-ISOLATION; COM1A AND COM4A

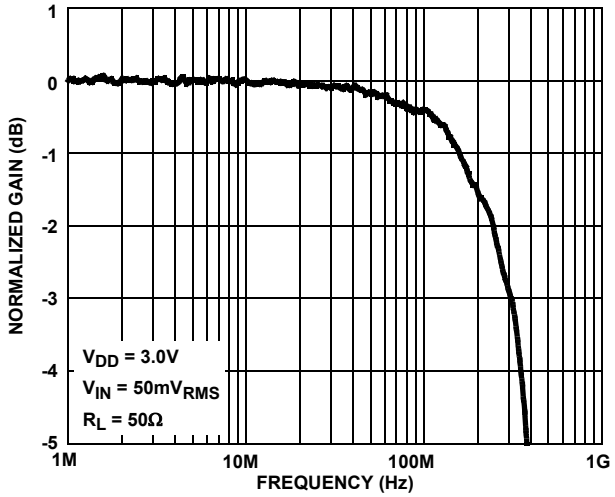


FIGURE 19. FREQUENCY RESPONSE; COM1B and COM4B

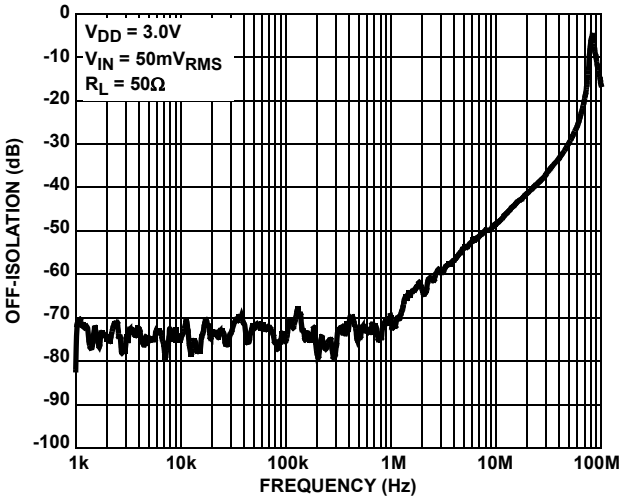


FIGURE 20. OFF-ISOLATION; COM1B and COM4B

Typical Performance Curves

T_A = +25°C, Unless Otherwise Specified. **(Continued)**

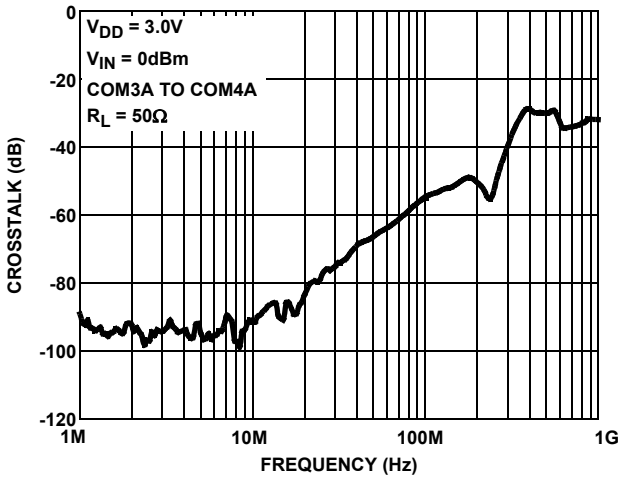


FIGURE 21. CROSSTALK

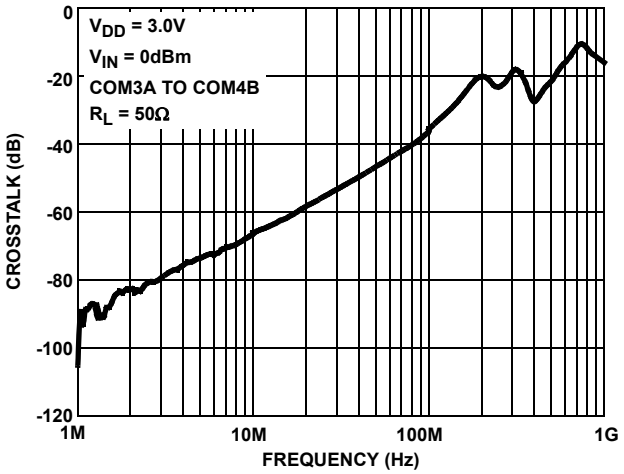


FIGURE 22. CROSSTALK

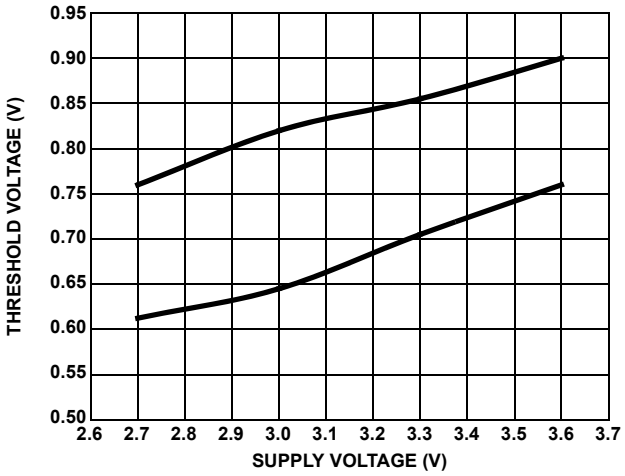


FIGURE 23. LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

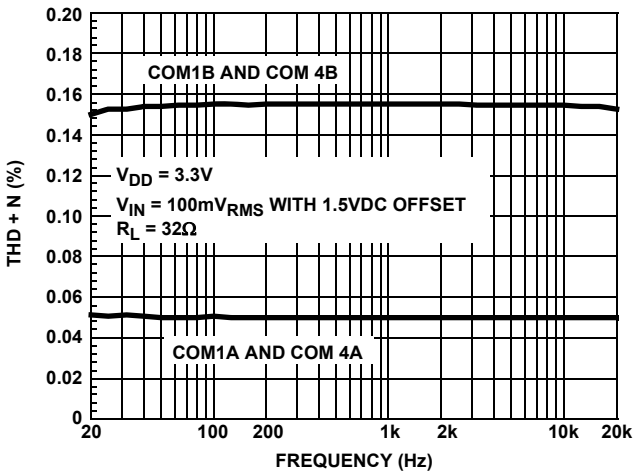


FIGURE 24. TOTAL HARMONIC DISTORTION vs FREQUENCY

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

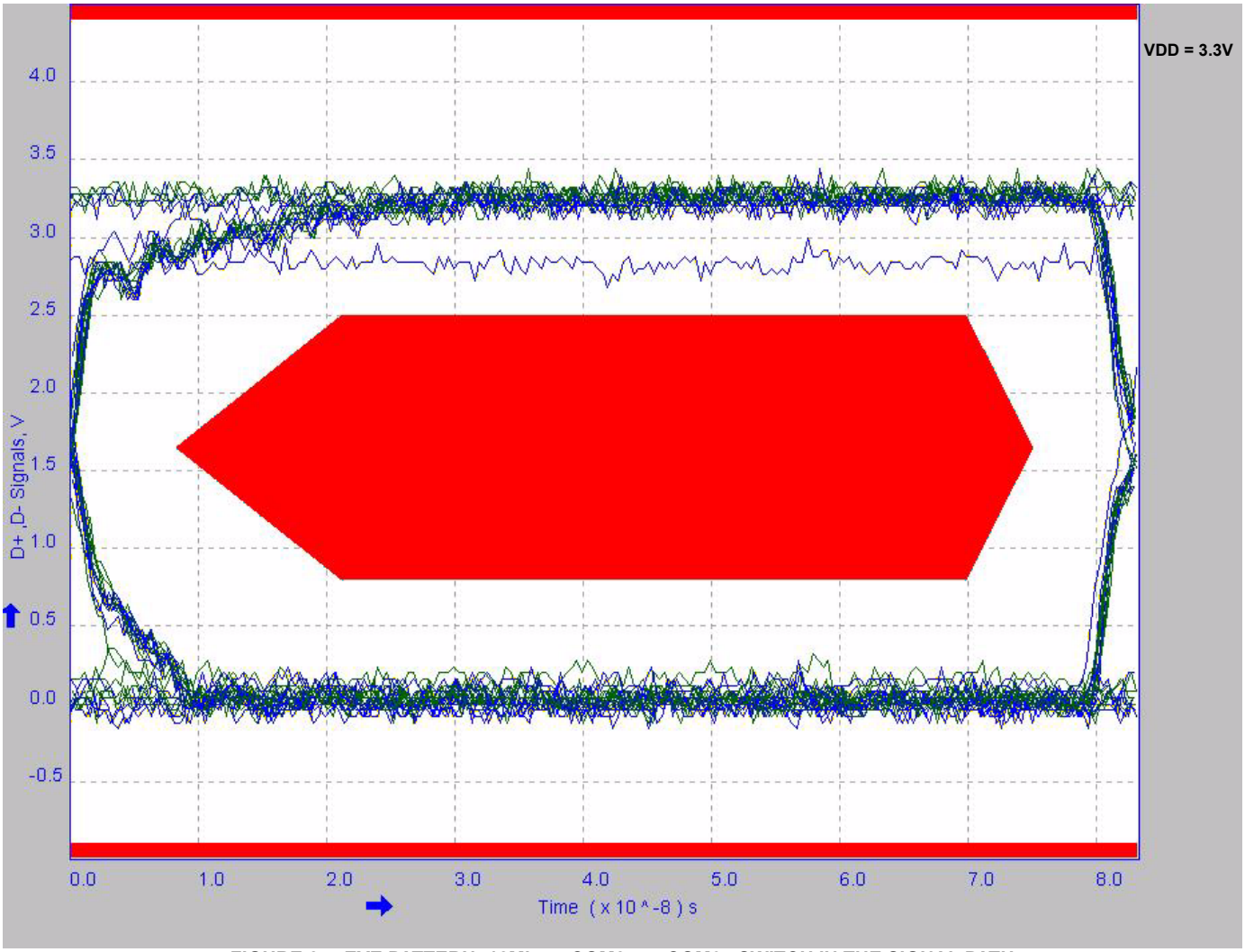


FIGURE 25. EYE PATTERN: 12Mbps; COM2x or COM3x SWITCH IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

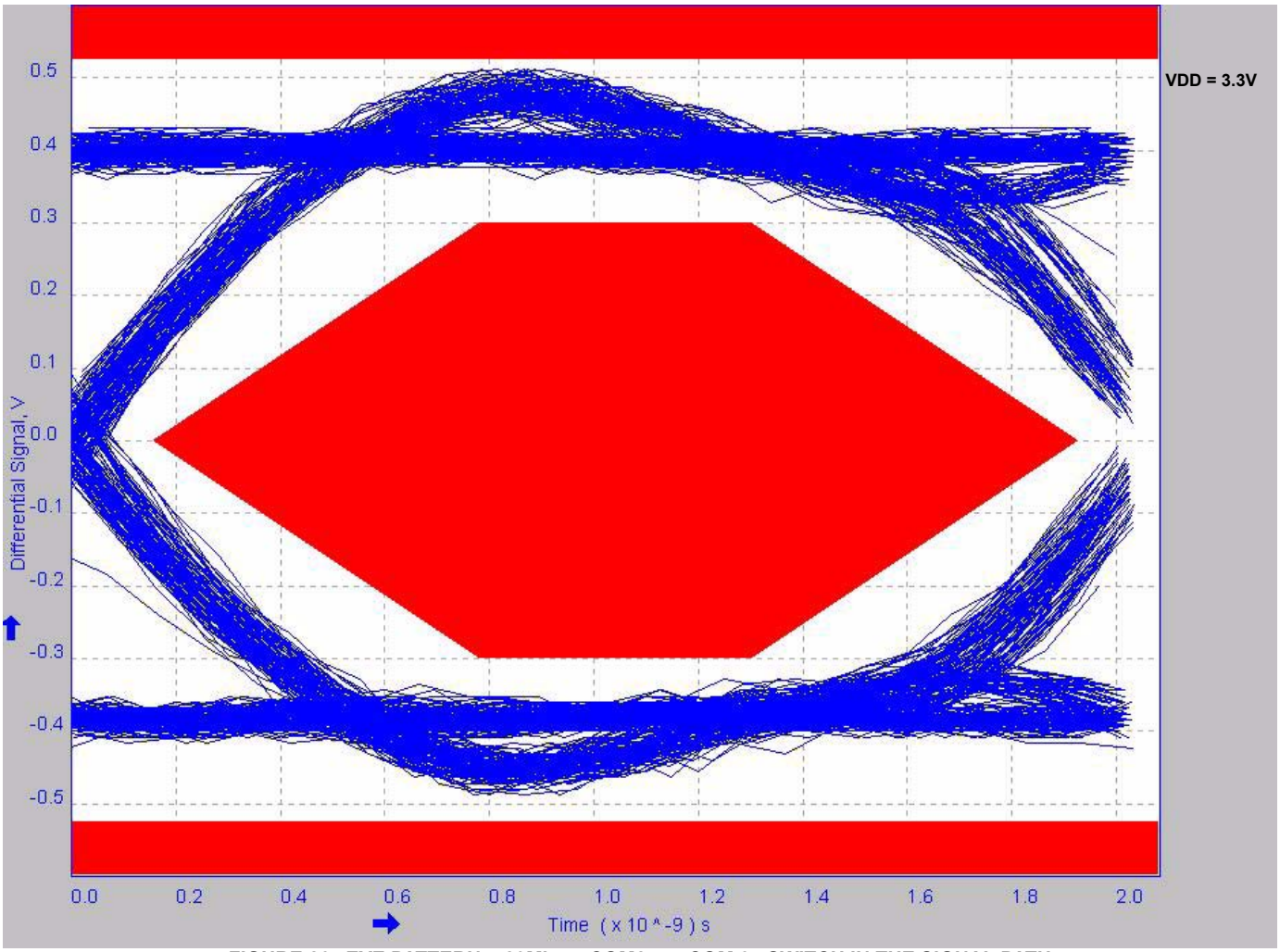


FIGURE 26. EYE PATTERN: 480Mbps; COM2x or COM 3x SWITCH IN THE SIGNAL PATH

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

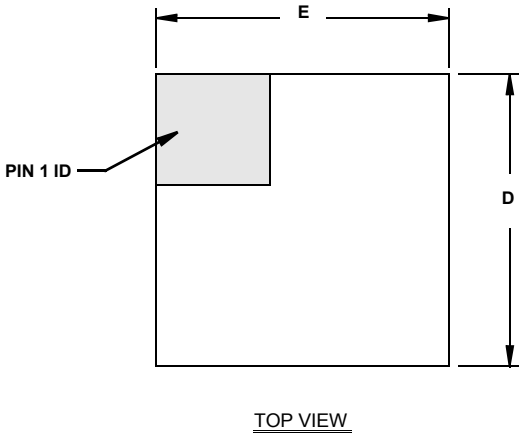
TRANSISTOR COUNT:

1216

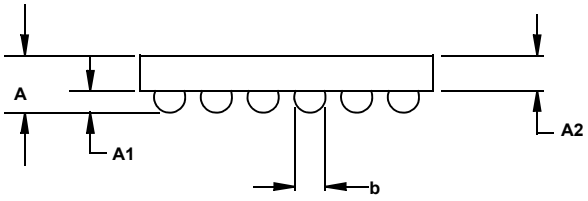
PROCESS:

Submicron, Dual Gate, Analog CMOS

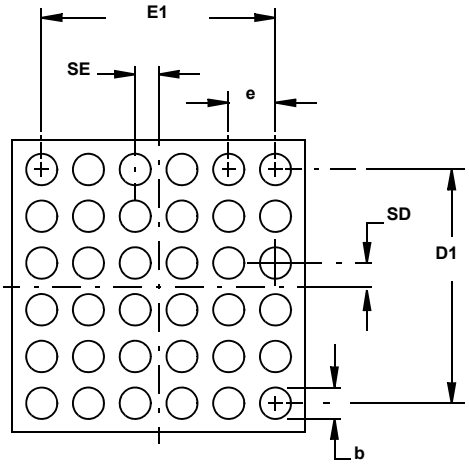
Wafer Level Chip Scale Package (WLCSP)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

W6x6.36

6x6 ARRAY 36 BALL WAFER LEVEL CHIP SCALE PACKAGE

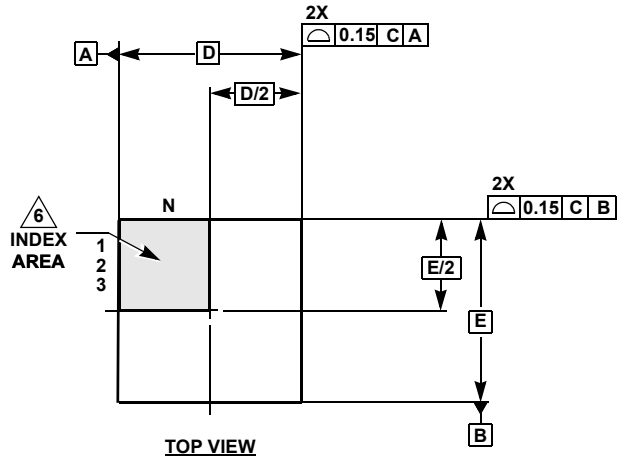
SYMBOL	MILLIMETERS
A	0.44 Min, 0.495 Nom, 0.55 Max
A_1	0.190 ±0.030
A_2	0.305 ±0.025
b	0.270 ±0.030
D	2.530 ±0.020
D_1	2.000 BASIC
E	2.530 ±0.020
E_1	2.000 BASIC
e	0.400 BASIC
SD	0.200 BASIC
SE	0.200 BASIC
Number of Bumps: 36	

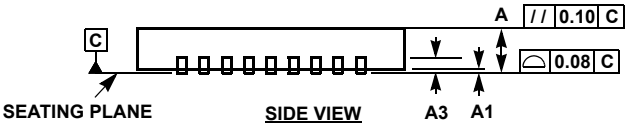
Rev. 0 6/08

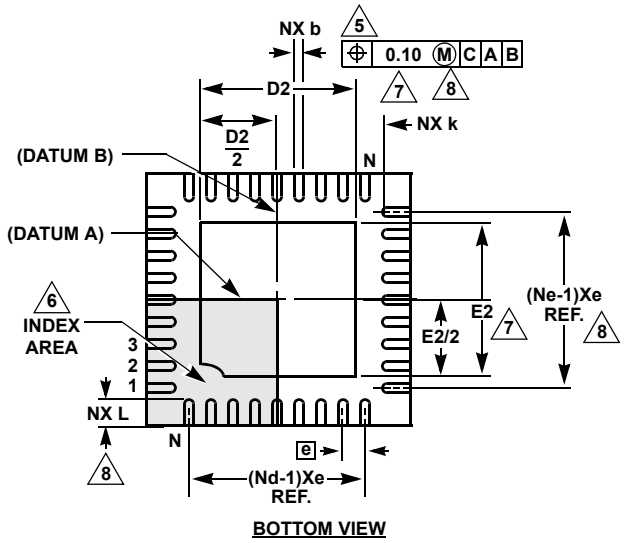
NOTES:

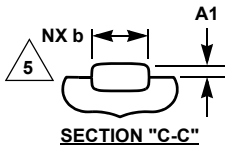
1. Dimensions are in millimeters.

Thin Quad Flat No-Lead Plastic Package (TQFN)
Thin Micro Lead Frame Plastic Package (TMLFP)









L32.5x5A

32 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220WJJD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.25	0.30	5, 8
D		5.00 BSC		-
D2	3.30	3.45	3.55	7, 8
E		5.00 BSC		-
E1		5.75 BSC		9
E2	3.30	3.45	3.55	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		32		2
Nd		8		3
Ne		8		3

Rev. 2 05/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.