NCP4586

150 mA, Low Noise, Low Dropout Regulator

The NCP4586 is a CMOS 150 mA low dropout linear with low noise, high ripple rejection, low dropout, high output voltage accuracy and low supply current. The device is available in three configurations: enable high, enable low and enable high plus auto−discharge. Small packages allow mounting on high density PCBs. This is an excellent general purpose regulator, well suited to many applications.

Features

- Operating Input Voltage Range: 1.7 V to 6.5 V
- Output Voltage Range: 1.2 to 5.0 V (available in 0.1 V steps)
- Very Low Dropout: 320 mV Typ. at 150 mA
- ±1% Output Voltage Accuracy (V_{OUT} > 2 V, T_J = 25°C)
- High PSRR: 80 dB at 1 kHz
- Current Fold Back Protection
- Stable with a 0.47 μF Ceramic Capacitors
- Available in 1.0 x 1.0 UDFN, SC−82AB and SOT23−5 Package
- These are Pb−Free Devices

Typical Applications

- Battery Powered Equipment
- Portable Communication Equipment
- Cameras, MP3 Players and Camcorder
- High Stability Voltage Reference

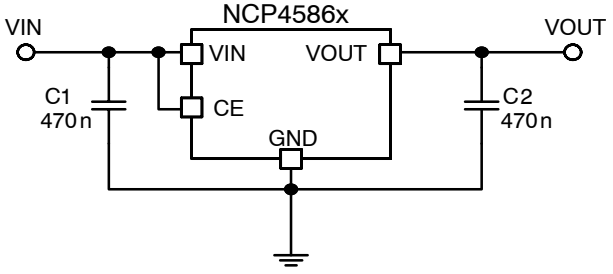


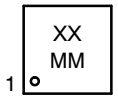
Figure 1. Typical Application Schematic

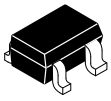
ON Semiconductor™

http://onsemi.com

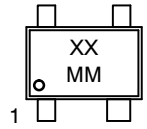
MARKING DIAGRAMS

UDFN4
CASE 517BR

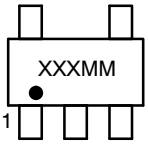




SC−82AB
CASE 419C



SOT−23−5
CASE 1212



XX, XXX = Specific Product Code
MM = Lot Number

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

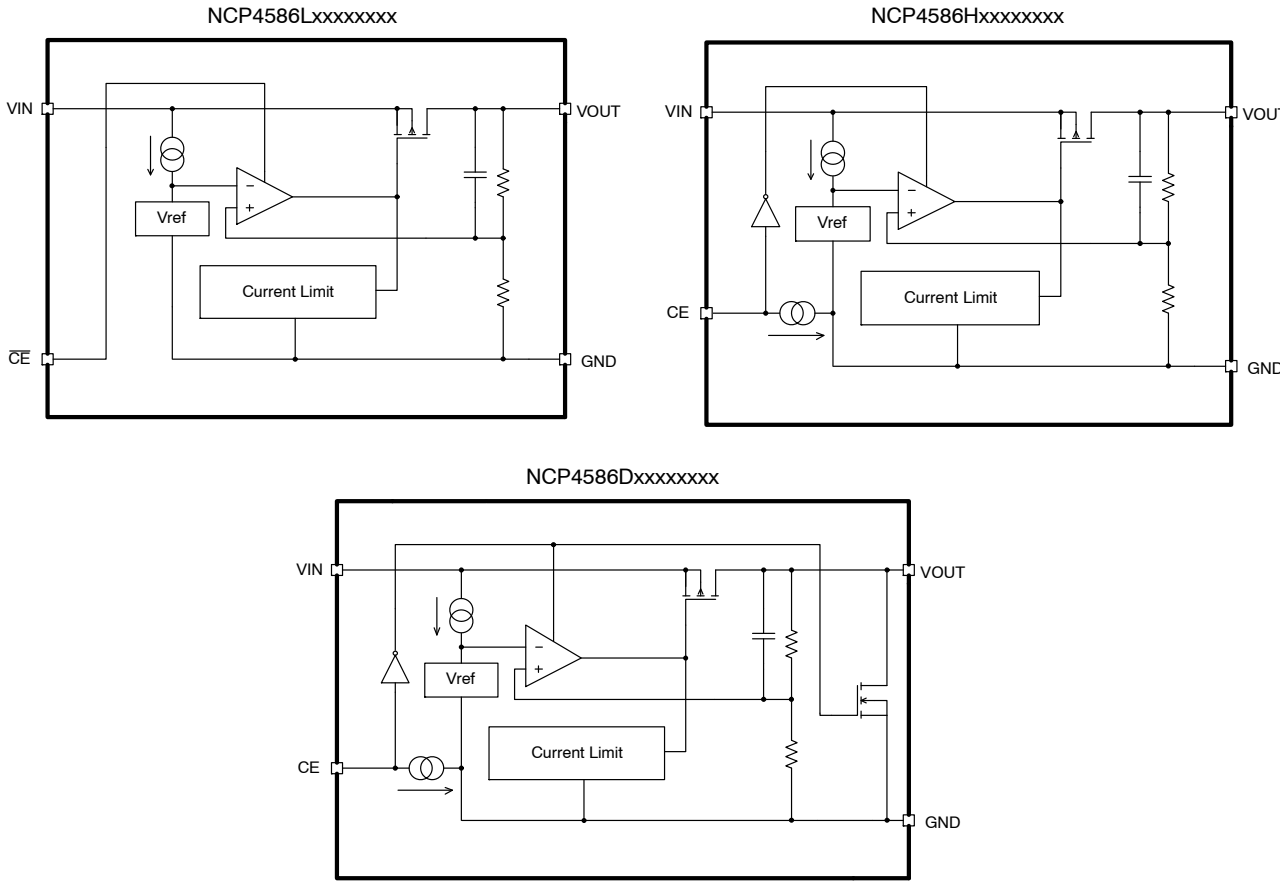


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. UDFN4	Pin No. SC82−AB	Pin No. SOT23−5	Pin Name	Description
4	4	1	VIN	Input pin
2	2	2	GND	Ground
3	1	3	$\overline{CE}$/CE	Chip enable pin (“L” active / “H” active)
1	3	5	VOUT	Output pin
–	–	4	NC	No connection

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	7	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	V_{CE}	−0.3 to 7	V
Output Current	I_{OUT}	200	mA
Power Dissipation UDFN4	P_D	400	mW
Power Dissipation SC−82AB		380	
Power Dissipation SOT23−5		420	
Maximum Junction Temperature	$T_{J(MAX)}$	+150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, UDFN4 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W
Thermal Characteristics, SOT23−5 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, SC 82AB Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	263	°C/W

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V or 2.5 V, whichever is greater; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 0.47 μF, unless otherwise noted. Typical values are at T_A = +25 °C.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.7		6.5	V
Output Voltage	T_A = +25 °C	V_{OUT} > 2 V	V_{OUT}	x0.99		x1.01	V
		$V_{OUT} \le 2$ V		−20		20	mV
	$-40°C \le T_A \le 85°C$	V_{OUT} > 2 V		x0.985		x1.015	V
		$V_{OUT} \le 2$ V		−30		30	mV
Output Voltage Temp. Coefficient	$T_A = -40$ to 85°C				±20		ppm/°C
Line Regulation	$V_{IN} = V_{OUT}$ + 0.5 V to 5 V		$Line_{Reg}$		0.02	0.10	%/V
Load Regulation	I_{OUT} = 1 mA to 150 mA		$Load_{Reg}$		10	30	mV
Dropout Voltage	I_{OUT} = 150 mA	1.2 V ≤ V_{OUT} < 1.5 V	V_{DO}		0.67	1.00	V
		1.5 V ≤ V_{OUT} < 1.7 V			0.54	0.81	
		1.7 V ≤ V_{OUT} < 2.0 V			0.46	0.68	
		2.0 V ≤ V_{OUT} < 2.5 V			0.41	0.60	
		2.5 V ≤ V_{OUT} < 4.0 V			0.32	0.51	
		4.0 V ≤ V_{OUT}			0.24	0.37	
Output Current			I_{OUT}	150			mA
Short Current Limit	V_{OUT} = 0 V		I_{SC}		40		mA
Quiescent Current	I_{OUT} = 0 mA		I_Q		38	58	μA
Standby Current	$V_{CE} = V_{IN}$ (L version), V_{CE} = 0 V(H and D version), T_A = 25°C		I_{STB}		0.1	1	μA
$\overline{CE}$/CE Pin Threshold Voltage	$\overline{CE}$ / CE Input Voltage “H”		V_{CEH}	1.0			V
	$\overline{CE}$ / CE Input Voltage “L”		V_{CEL}			0.4	
CE Pull Down Current	H and D version		I_{PD}		0.4		μA
Power Supply Rejection Ratio	$V_{IN} = V_{OUT}$ + 1 V or 3.0 V whichever is higher, I_{OUT} = 30 mA, f = 1 kHz		PSRR		80		dB
Output Noise Voltage	V_{OUT} = 1.2 V, I_{OUT} = 30 mA, f = 10 Hz to 100 kHz		V_N		30		μV_{rms}
Low Output N−ch Tr. On Resistance	D Version only, V_{IN} = 4 V, V_{CE} = 0 V		R_{LOW}		30		Ω

TYPICAL CHARACTERISTICS

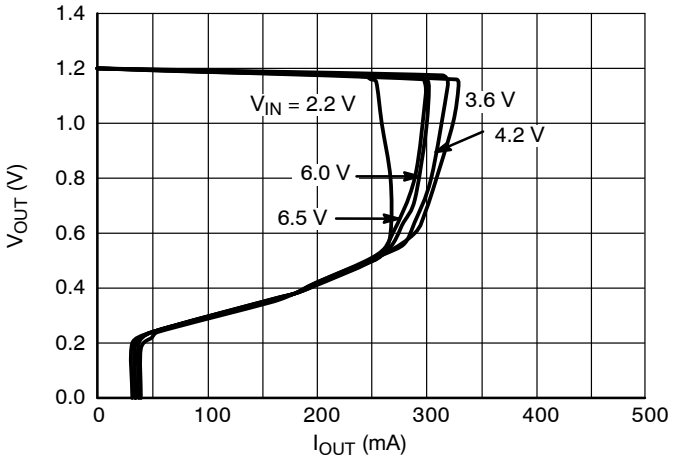


Figure 3. Output Voltage vs. Output Current 1.2 V Version (T_A = 25 °C)

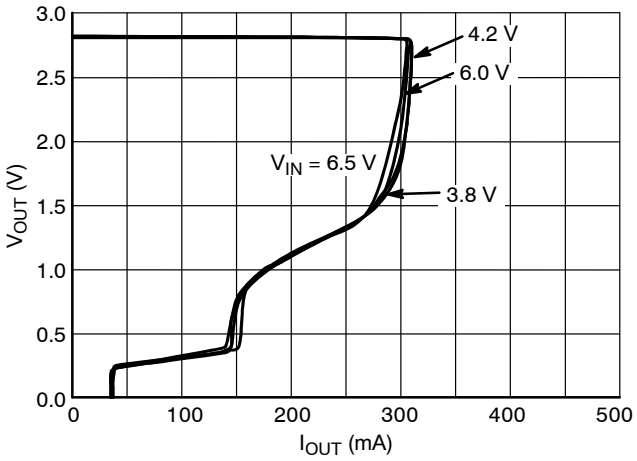


Figure 4. Output Voltage vs. Output Current 2.8 V Version (T_A = 25 °C)

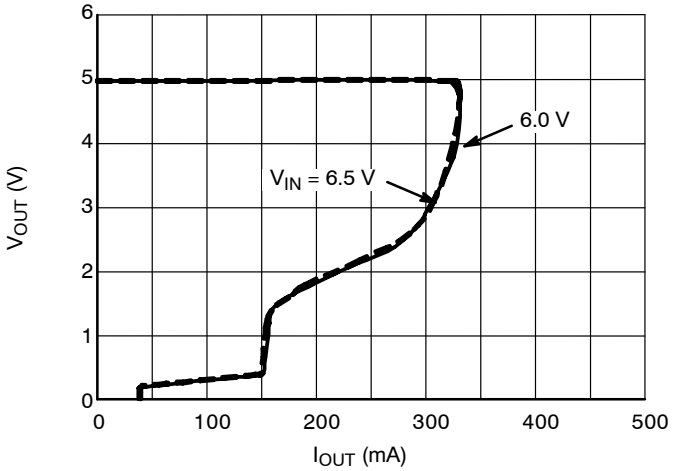


Figure 5. Output Voltage vs. Output Current 5.0 V version (T_A = 25°C)

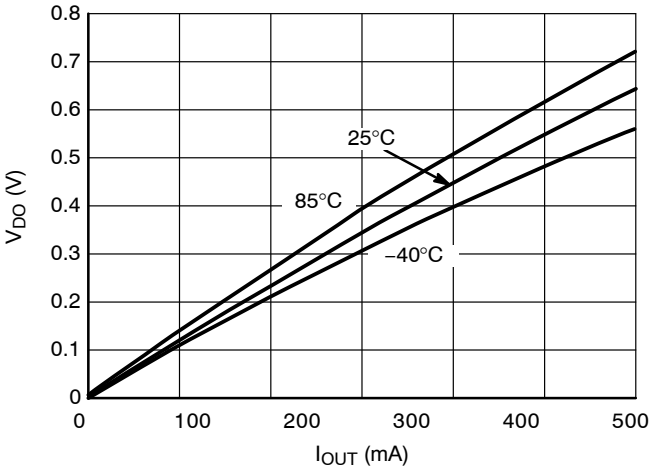


Figure 6. Dropout Voltage vs. Output Current 1.2 V version

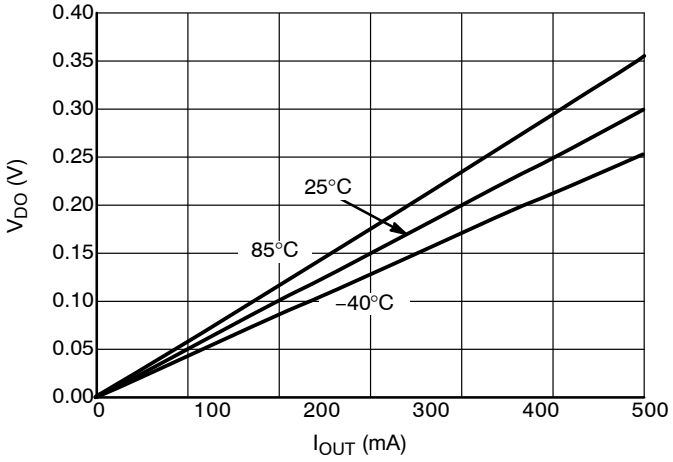


Figure 7. Dropout Voltage vs. Output Current 2.8 V Version

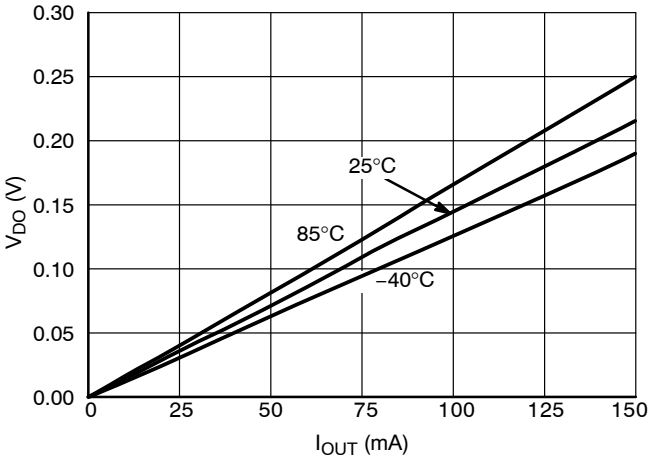


Figure 8. Dropout Voltage vs. Output Current 5.0 V Version

TYPICAL CHARACTERISTICS

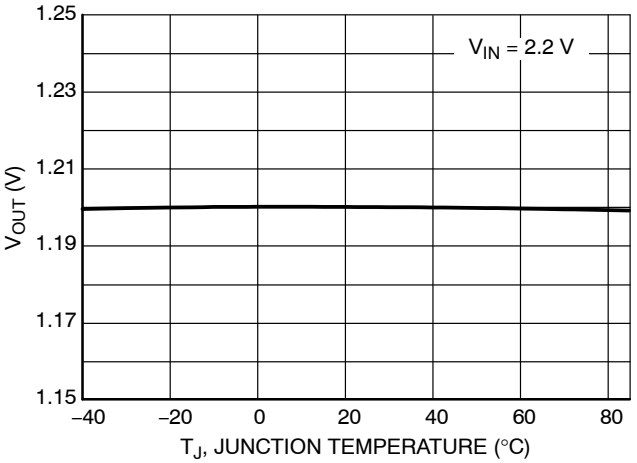


Figure 9. Output Voltage vs. Temperature, 1.2 V Version

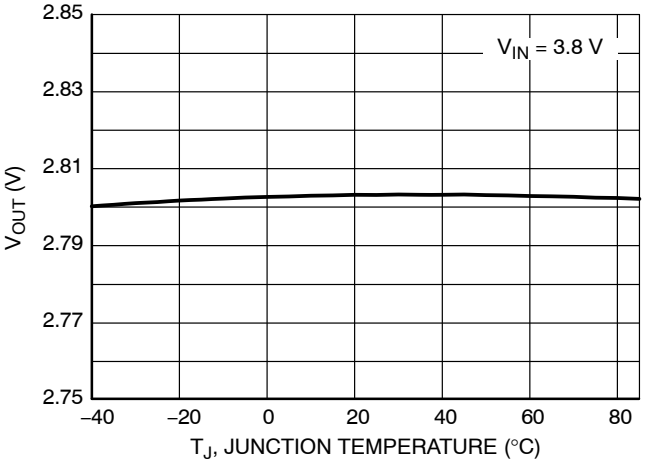


Figure 10. Output Voltage vs. Temperature, 2.8 V version

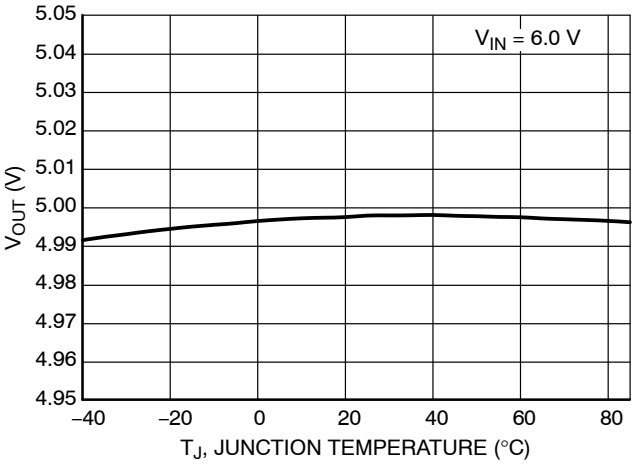


Figure 11. Output Voltage vs. Temperature, 5.0 V Version

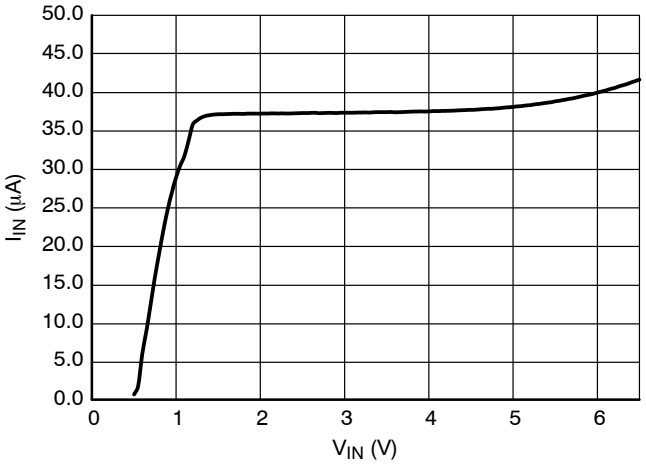


Figure 12. Supply Current vs. Input Voltage, 1.2 V Version

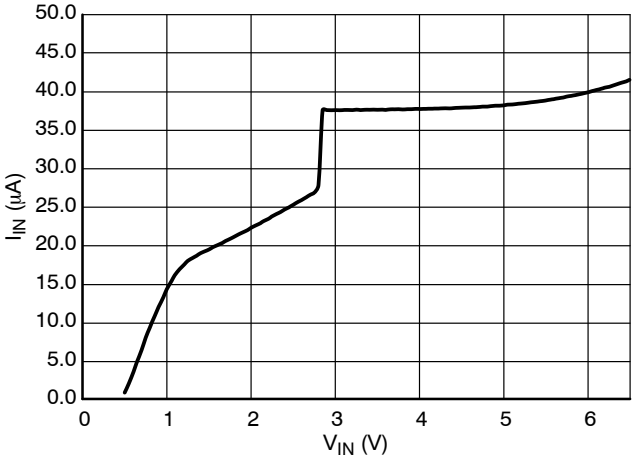


Figure 14. Supply Current vs. Input Voltage, 2.8 V Version

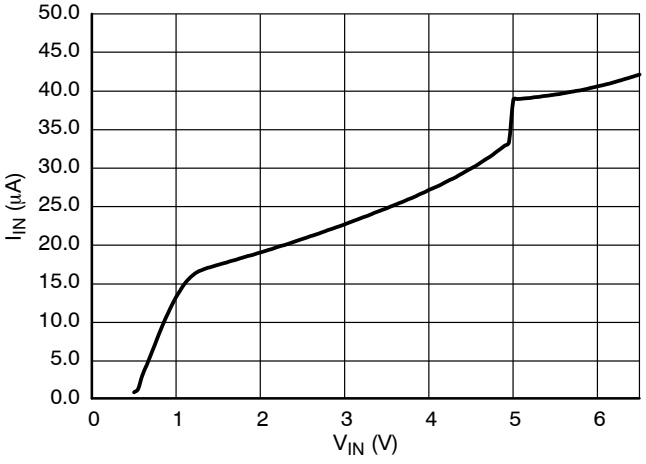


Figure 13. Supply Current vs. Input Voltage, 5.0 V version

TYPICAL CHARACTERISTICS

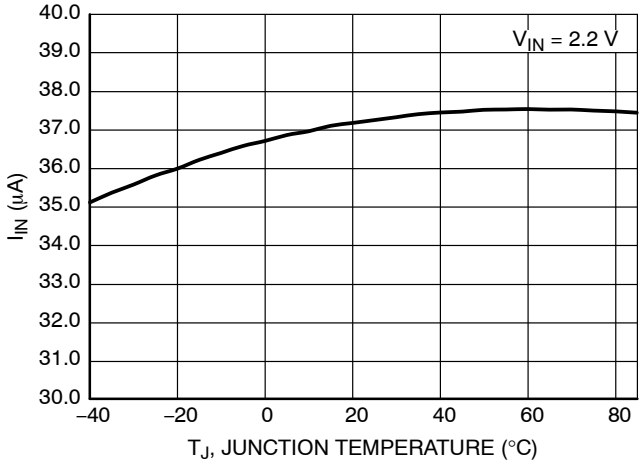


Figure 15. Supply Current vs. Temperature, 1.2 V Version

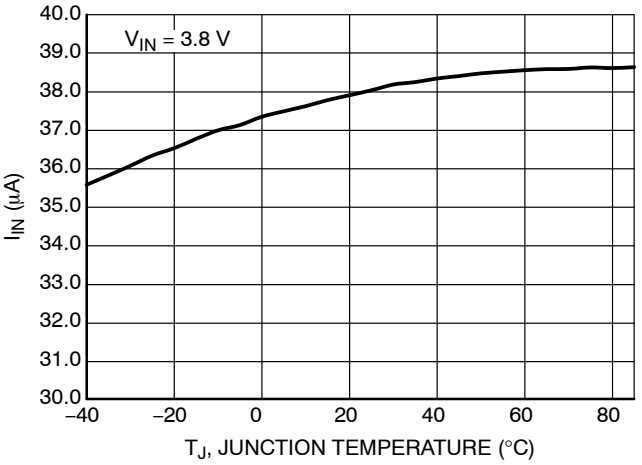


Figure 16. Supply Current vs. Temperature, 2.8 V Version

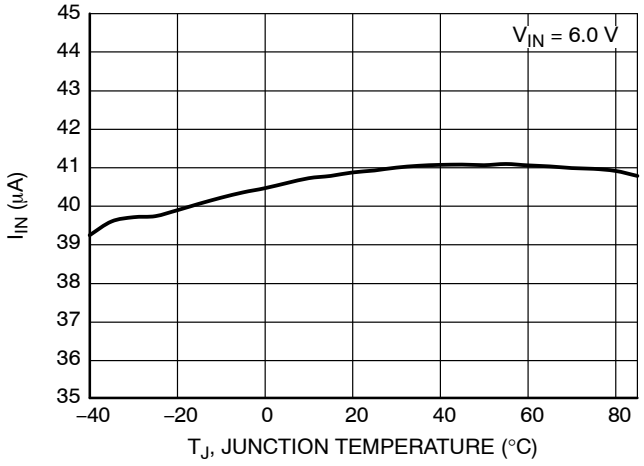


Figure 17. Supply Current vs. Temperature, 5.0 V Version

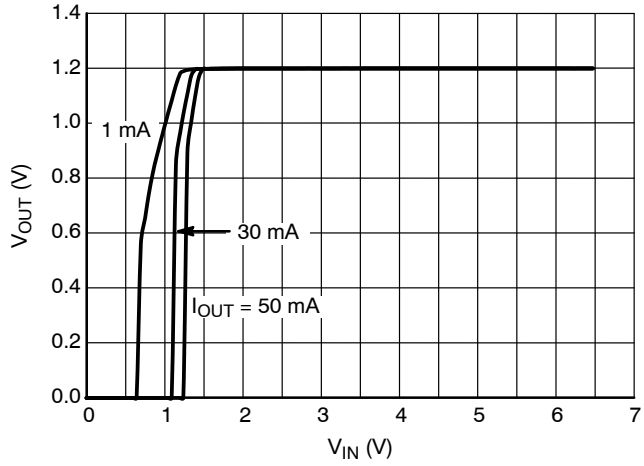


Figure 18. Output Voltage vs. Input Voltage, 1.2 V Version

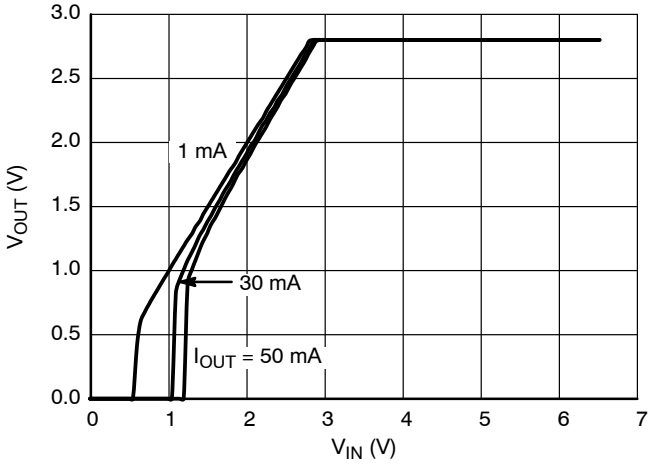


Figure 19. Output Voltage vs. Input Voltage, 2.8 V Version

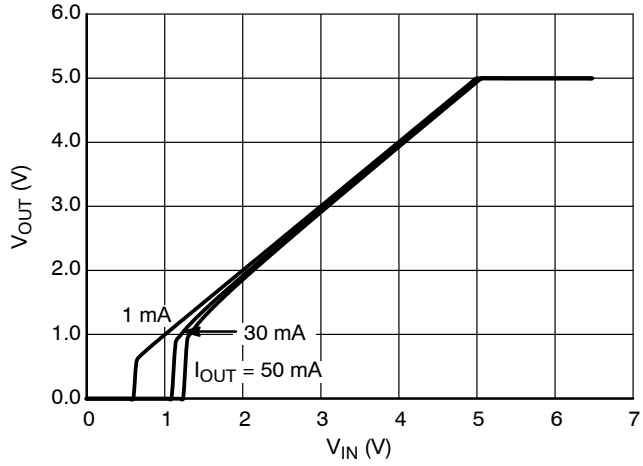


Figure 20. Output Voltage vs. Input Voltage, 5.0 V Version

TYPICAL CHARACTERISTICS

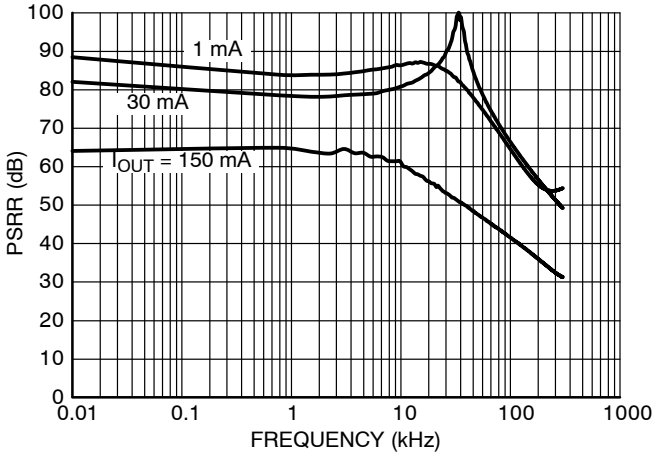


Figure 21. PSRR, 1.2 V Version

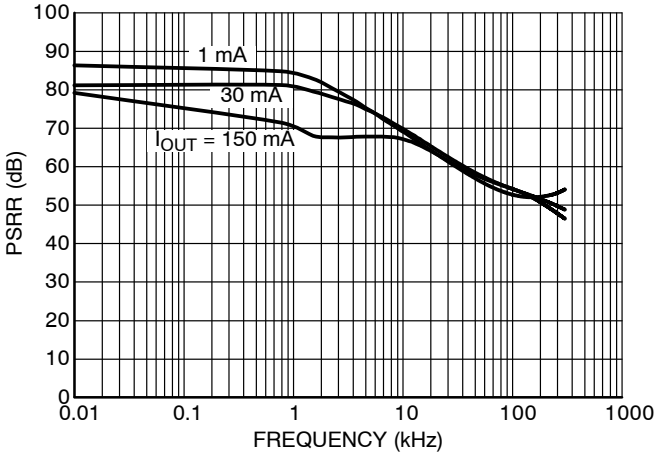


Figure 22. PSRR, 2.8 V Version

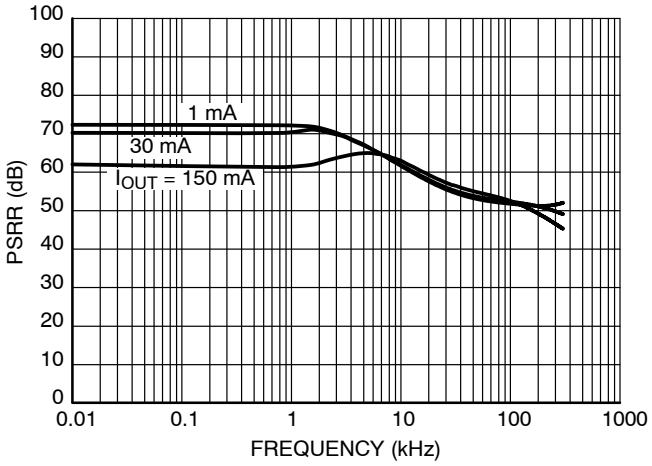


Figure 23. PSRR, 5.0 V Version

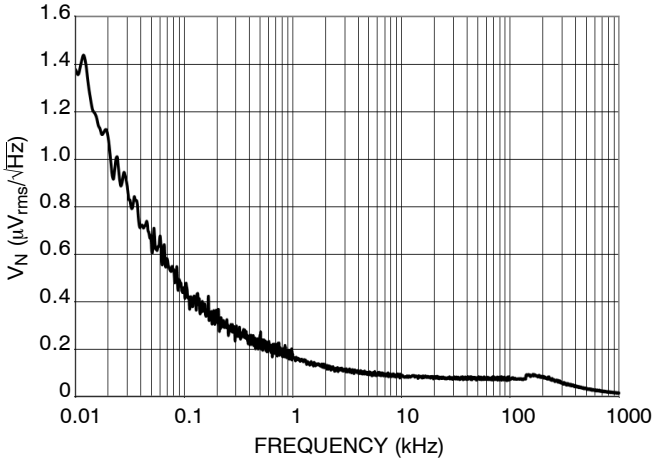


Figure 24. Output Voltage Noise, 1.2 V Version

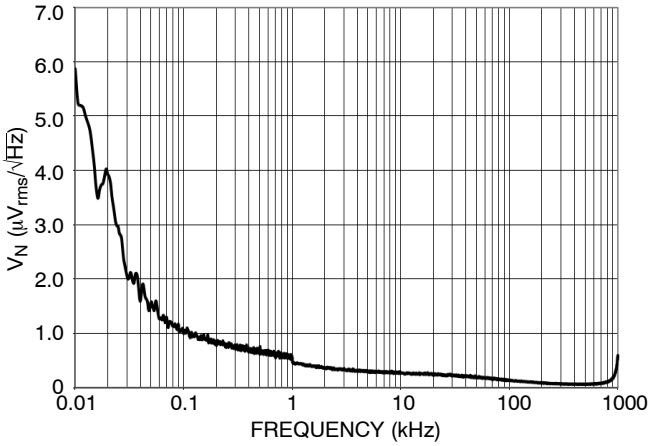


Figure 25. Output Voltage Noise, 2.8 V Version

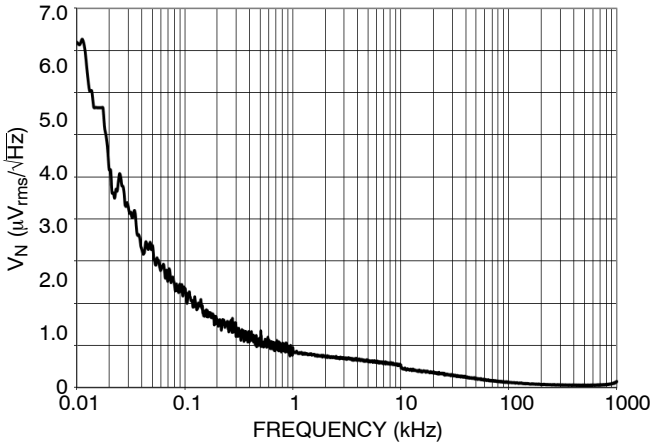


Figure 26. Output Voltage Noise, 5.0 V Version

TYPICAL CHARACTERISTICS

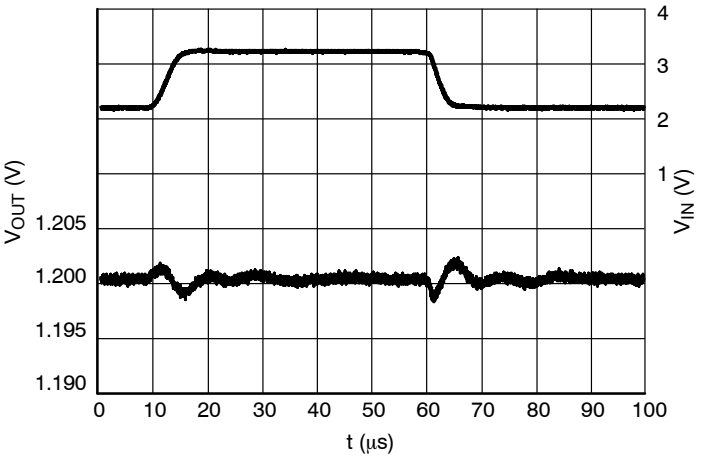


Figure 27. Line Transients, 1.2 V Version, t_R = t_F = 5 μs, I_{OUT} = 30 mA

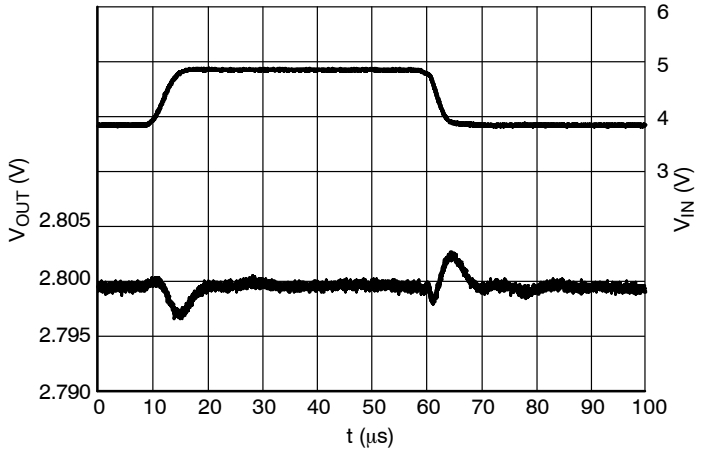


Figure 28. Line Transients, 2.8 V Version, t_R = t_F = 5 μs, I_{OUT} = 30 mA

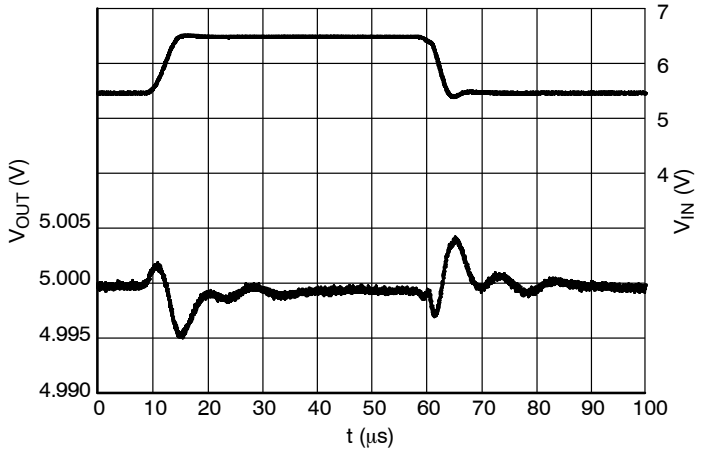


Figure 29. Line Transients, 5.0 V Version, t_R = t_F = 5 μs, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

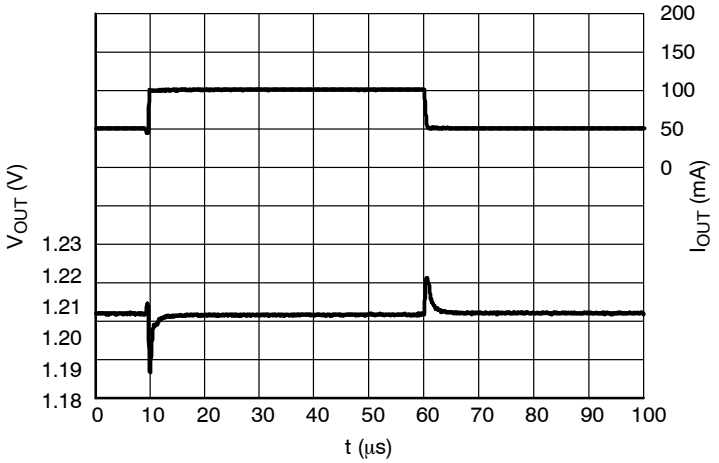


Figure 30. Load Transients, 1.2 V Version, I_{OUT} = 50 − 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 2.2 V

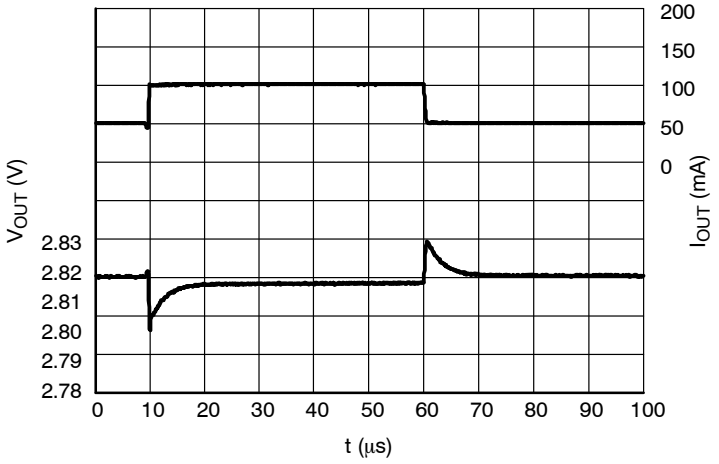


Figure 31. Load Transients, 2.8 V Version, I_{OUT} = 50 − 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 3.8 V

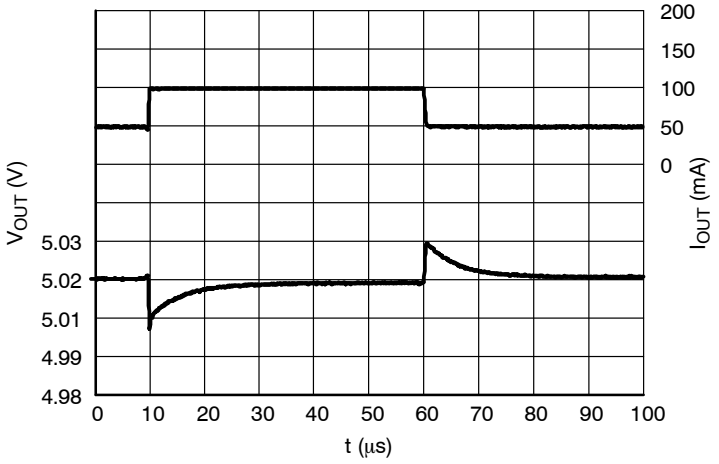


Figure 32. Load Transients, 5.0 V Version, I_{OUT} = 50 − 100 mA, $t_R = t_F$ = 0.5 μs, V_{IN} = 6.0 V

TYPICAL CHARACTERISTICS

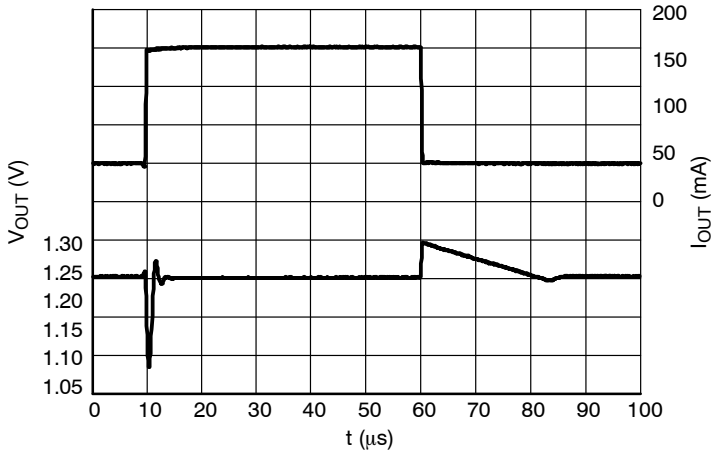


Figure 33. Load Transients, 1.2 V Version, I_{OUT} = 1 − 150 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.2 V

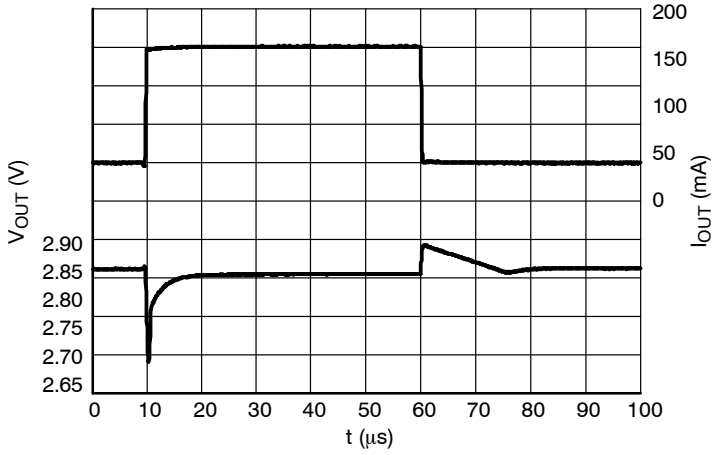


Figure 34. Load Transients, 2.8 V Version, I_{OUT} = 1 − 150 mA, t_R = t_F = 0.5 μs, V_{IN} = 3.8 V

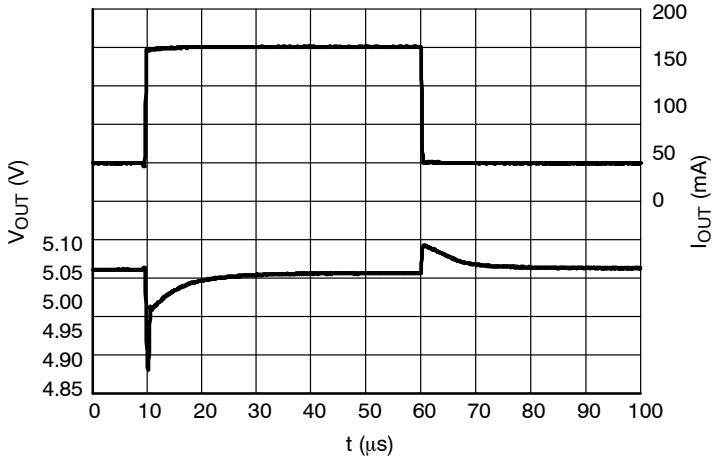


Figure 35. Load Transients, 5.0 V Version, I_{OUT} = 1 − 150 mA, t_R = t_F = 0.5 μs, V_{IN} = 6.0 V

TYPICAL CHARACTERISTICS

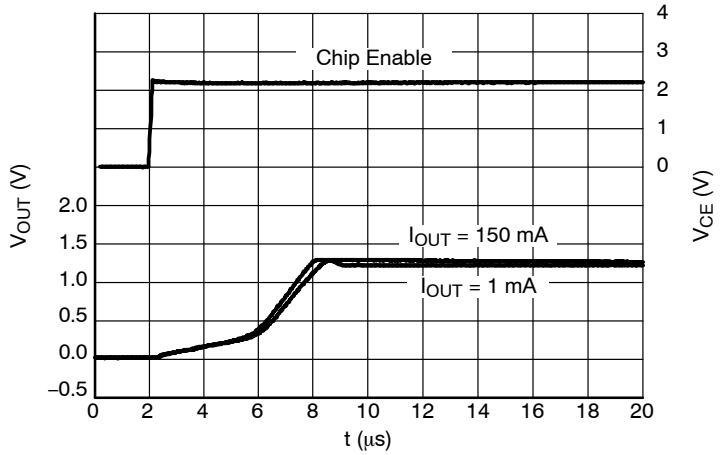


Figure 36. Start−up, 1.2 V Version, V_{IN} = 2.2 V

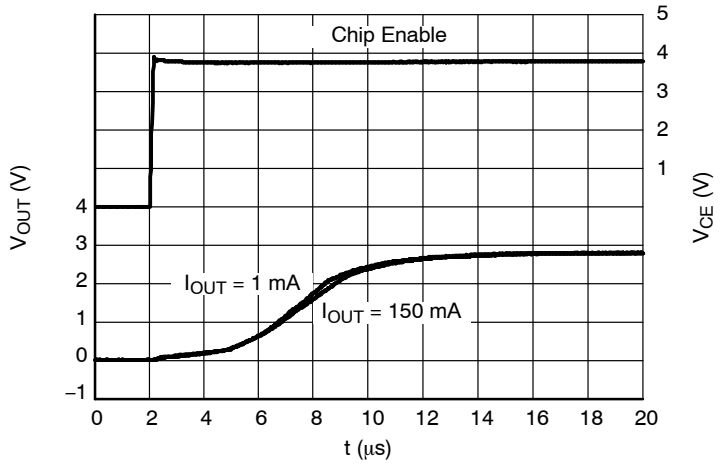


Figure 37. Start−up, 2.8 V Version, V_{IN} = 3.8 V

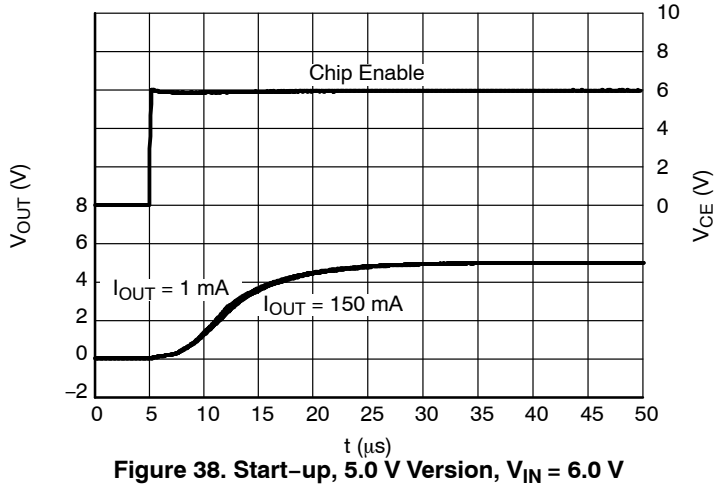


Figure 38. Start−up, 5.0 V Version, V_{IN} = 6.0 V

TYPICAL CHARACTERISTICS

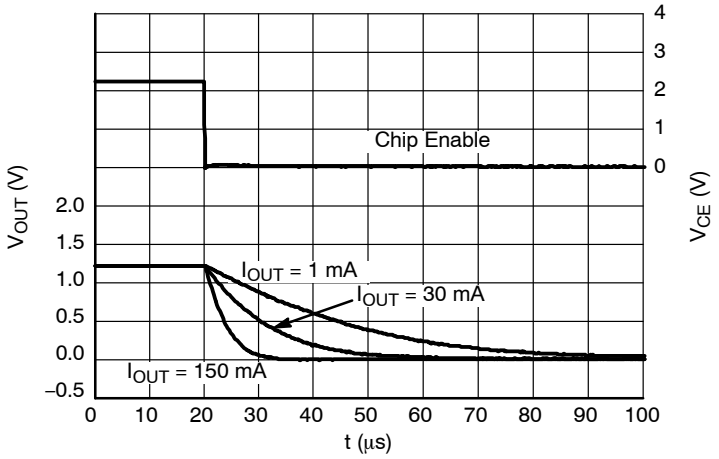


Figure 39. Shutdown, 1.2 V Version D, V_{IN} = 2.2 V

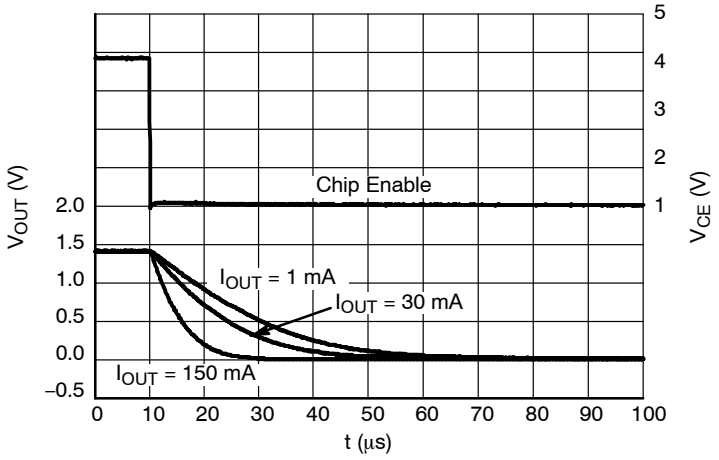


Figure 40. Shutdown, 2.8 V Version D, V_{IN} = 3.8 V

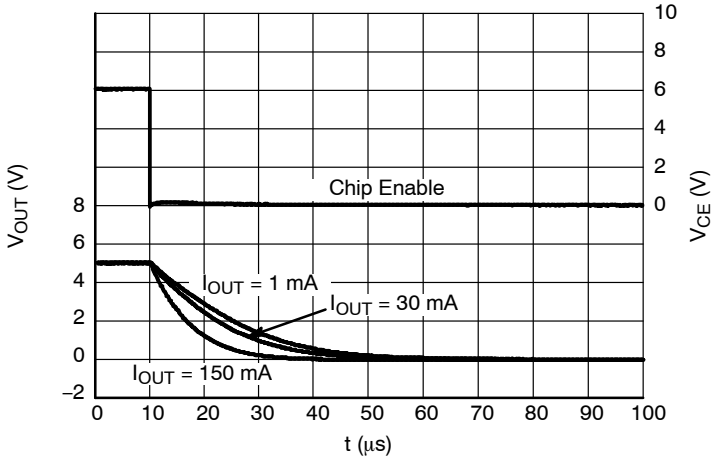


Figure 41. Shutdown, 5.0 V version D, V_{IN} = 6.0 V

APPLICATION INFORMATION

A typical application circuit for NCP4586 series is shown in Figure 42.

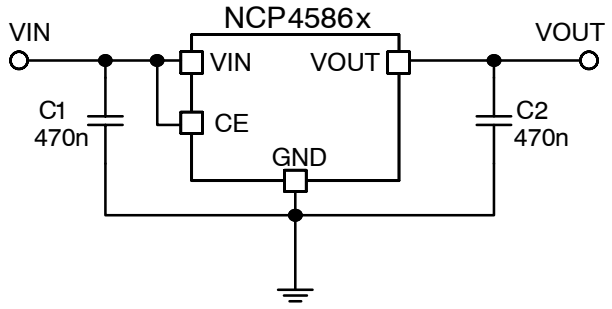


Figure 42. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 470 nF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4586. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 470 nF or larger ceramic output decoupling capacitor is sufficient to achieve stable operation of the IC. If a tantalum capacitor is used, and its ESR is high, loop oscillation may result. The capacitors should be connected as close as possible to the output and ground pins. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The Enable pin $\overline{CE}$ or CE may be used for turning the regulator on and off. Control polarity is dependent on version of IC. Active high or low versions are available; please see the ordering information table. The Enable pin has an internal pull down current source for versions H and D. If the enable function is not needed connect the $\overline{CE}$ pin to ground for version L or connect the CE pin to VIN for versions H and D.

Output Discharger

The D version includes a transistor between VOUT and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal

As power across the IC increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature rise for the part. That is to say, when the device has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

PCB Layout

Make VIN and GND line sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

ORDERING INFORMATION

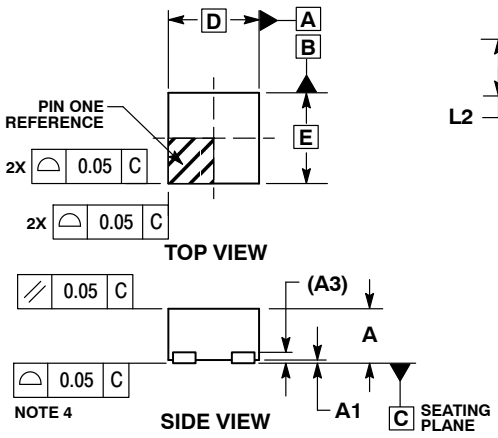
Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP4586DSQ12T1G	1.2 V	Enable High, Auto discharge	LA	SC82AB (Pb−Free)	3000 / Tape & Reel
NCP4586DSQ18T1G	1.8 V		LG		
NCP4586DSQ28T1G	2.8 V		MH		
NCP4586DSQ30T1G	3.0 V		NA		
NCP4586DSQ33T1G	3.3 V		ND		
NCP4586DSQ50T1G	5.0 V		QA		
NCP4586DMU12TCG	1.2 V		VA	UDFN4 (Pb−Free)	10000 / Tape & Reel
NCP4586DMU14TCG	1.4 V		VC		
NCP4586DMU15TCG	1.5 V		VD		
NCP4586DMU18TCG	1.8 V		VG		
NCP4586DMU25TCG	2.5 V		VQ		
NCP4586DMU28TCG	2.8 V		VT		
NCP4586DMU30TCG	3.0 V		VW		
NCP4586DMU33TCG	3.3 V		VZ		
NCP4586DMU50TCG	5.0 V		WS		
NCP4586DSN12T1G	1.2 V		H2A	SOT−23−5 (Pb−Free)	3000 / Tape & Reel
NCP4586DSN18T1G	1.8 V		H2G		
NCP4586DSN28T1G	2.8 V		H2T		
NCP4586DSN30T1G	3.0 V		H2W		
NCP4586DSN33T1G	3.3 V		H2Z		
NCP4586DSN50T1G	5.0 V		J2S		

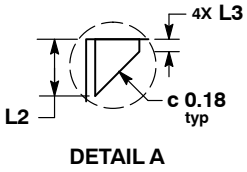
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

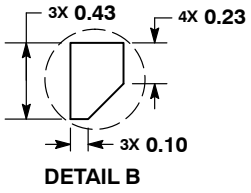
NOTE: To order other package and voltage variants, please contact your ON Semiconductor sales representative.

PACKAGE DIMENSIONS

UDFN4 1.0x1.0, 0.65P
CASE 517BR−01
ISSUE O

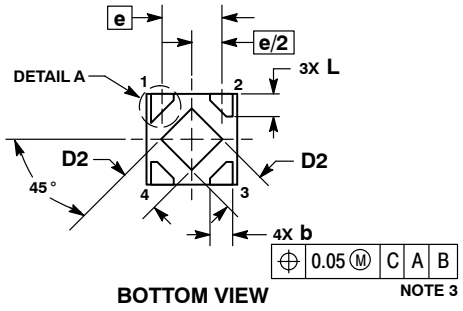




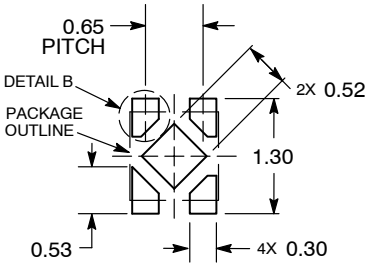


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.60
A1	0.00	0.05
A3	0.10 REF	
b	0.20	0.30
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.27	0.37
L3	0.02	0.12



RECOMMENDED MOUNTING FOOTPRINT*

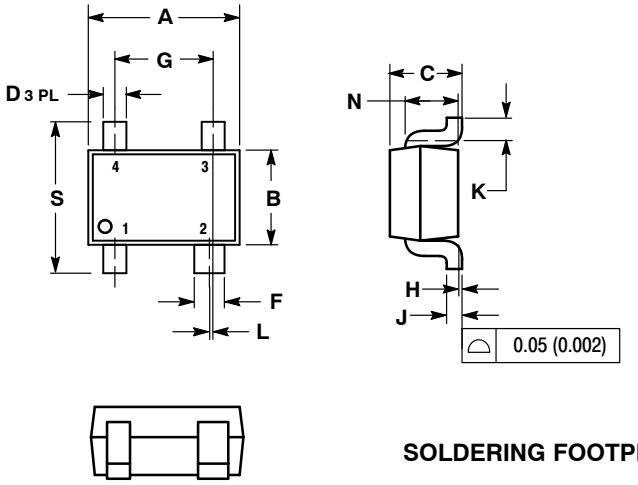


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

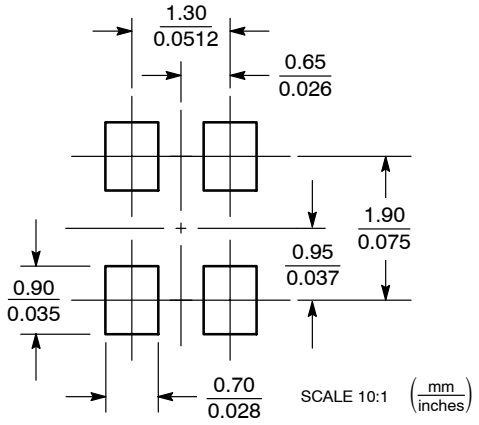
SC−82AB
CASE 419C−02
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. 419C−01 OBSOLETE. NEW STANDARD IS 419C−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.8	2.2	0.071	0.087
B	1.15	1.35	0.045	0.053
C	0.8	1.1	0.031	0.043
D	0.2	0.4	0.008	0.016
F	0.3	0.5	0.012	0.020
G	1.1	1.5	0.043	0.059
H	0.0	0.1	0.000	0.004
J	0.10	0.26	0.004	0.010
K	0.1	−−−	0.004	−−−
L	0.05 BSC		0.002 BSC	
N	0.2 REF		0.008 REF	
S	1.8	2.4	0.07	0.09

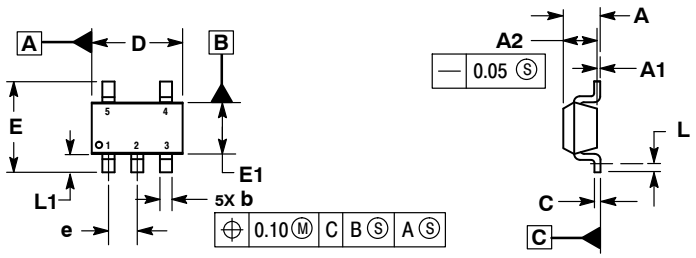
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

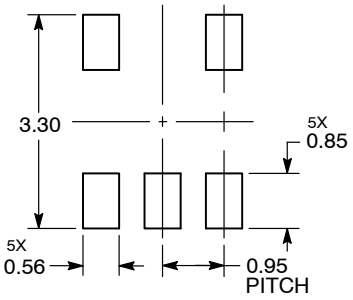
SOT−23 5−LEAD
CASE 1212−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Email: orderlit@onsemi.com

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