# PI74ALVCH16646

## 16-Bit Bus Transceiver and Register with 3-STATE Outputs

### Product Features

- PI74ALVCH16646 is designed for low voltage operation
- $V_{CC}$ = 2.3V to 3.6V
- Hysteresis on all inputs
- Typical $V_{OLP}$ (Output Ground Bounce)
  < 0.8V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot)
  < 2.0V at $V_{CC}$ = 3.3V, $T_A$ = 25°C
- Bus Hold retains last active bus state during 3-STATE, eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 300 mil wide plastic SSOP (V)

### Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The PI74ALVCH16646 is a 16-bit bus transceiver and register designed for 2.3V to 3.6V $V_{CC}$ operation. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate Clock (CLKAB or CLKBA) input. Four fundamental bus-management functions can be performed.

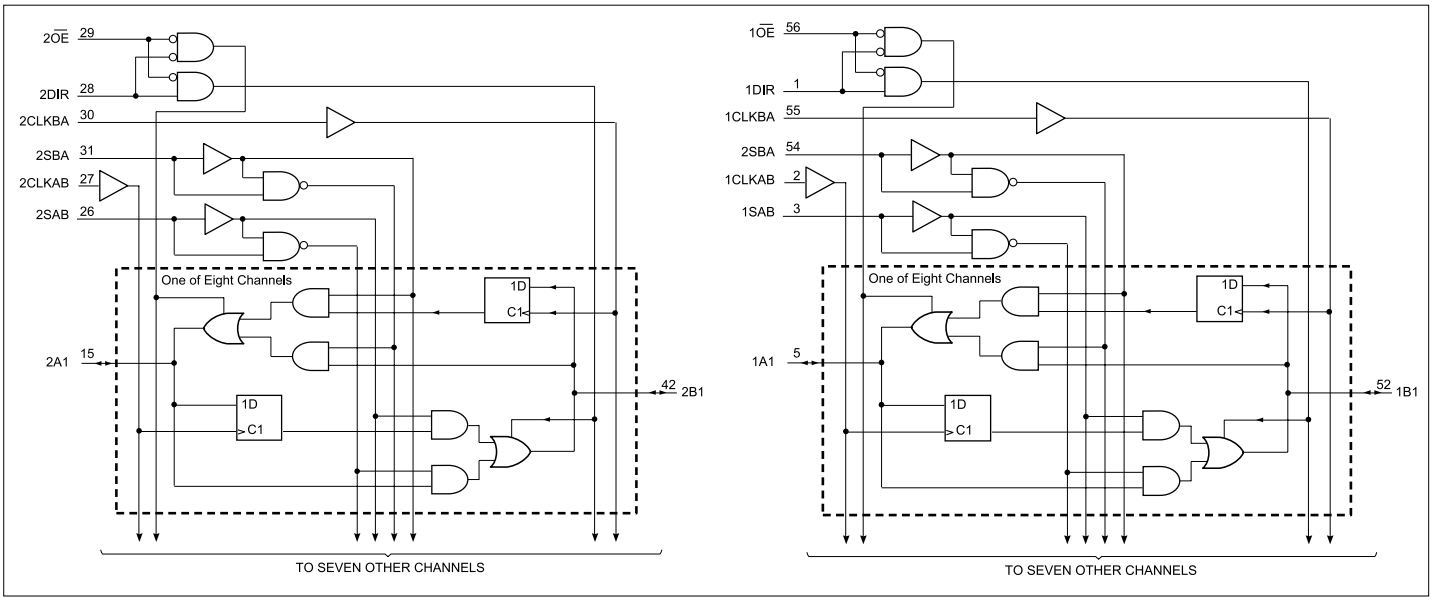
Output Enable ($\overline{OE}$) and Direction Control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The Select Control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. Circuitry used for Select Control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{OE}$ is LOW. In the isolation mode ($\overline{OE}$ HIGH), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

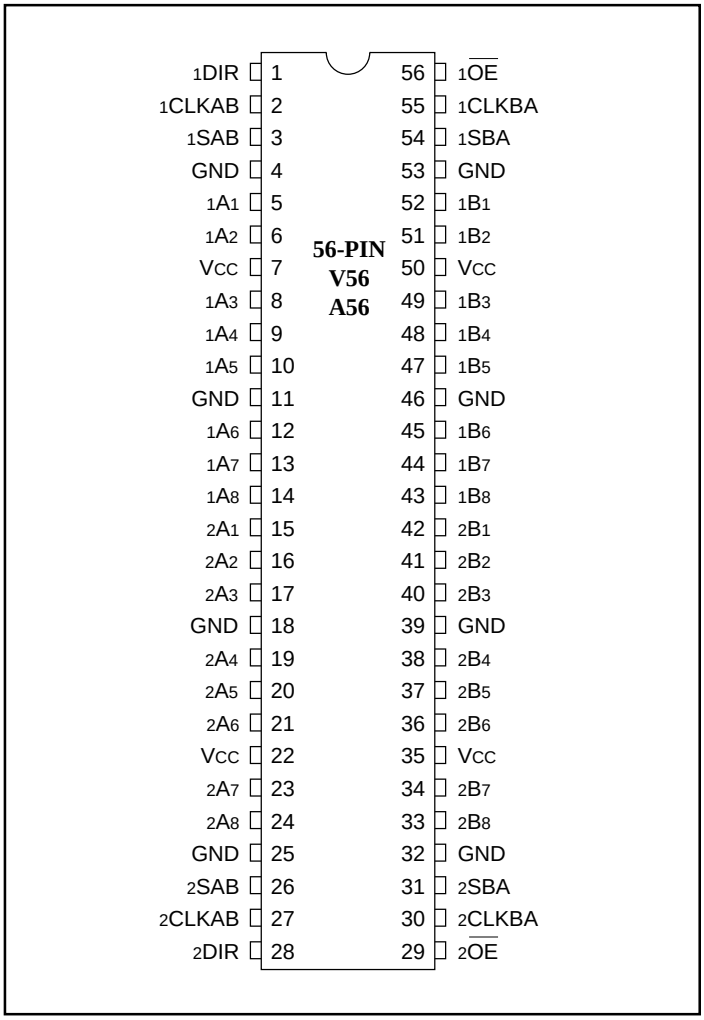
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

### Logic Block Diagram



## Product Pin Configuration




## Product Pin Description

| Pin Name | Description |
|---|---|
| x$\overline{OE}$ | Output Enable Inputs (Active LOW) |
| xDIR | Direction Control |
| xCLKAB, xCLKBA | Clock Pulse Inputs |
| xSAB, xSBA | Select Control Inputs |
| xAx | Data Register A Inputs<br>Data Register B Outputs |
| xBx | Data Register B Inputs<br>Data Register A Outputs |
| GND | Ground |
| $V_{CC}$ | Power |

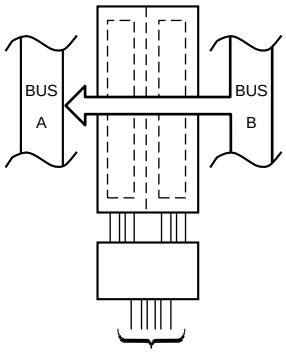
## Truth Table[2]

| | Inputs | | | | | | Data I/O | |
|---|---|---|---|---|---|---|---|---|
| **Function** | **x$\overline{OE}$** | **xDIR** | **xCLKAB** | **xCLKBA** | **xSAB** | **xSBA** | **xAx** | **xBx** |
| Store A, B Unspecified[1] | X | X | ↑ | X | X | X | Input | Unspecified[1] |
| Store B, A Unspecified[1] | X | X | X | ↑ | X | X | Unspecified[1] | Input |
| Isolation | H | X | H or L | H or L | X | X | Input Disable | Input Disable |
| Store A and B Data | H | X | ↑ | ↑ | X | X | Input | Input |
| Real Time A Data to B Bus | L | H | X | X | L | X | Input | Output |
| Stored A Data to B Bus | L | H | H or L | X | H | X | Input | Output |
| Real Time B Data to A Bus | L | L | X | X | X | L | Output | Input |
| Stored B Data to A Bus | L | L | X | H or L | X | H | Output | Input |

**Note:**

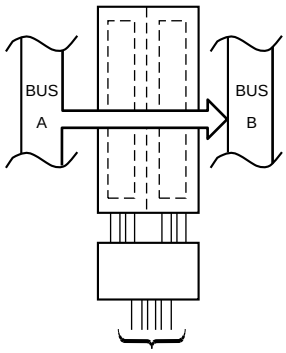
1. The data output functions may be enabled or disabled by various signals at the x$\overline{OE}$ or xDIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   ↑ = LOW-to-HIGH Transition

**REAL-TIME TRANSFER**
**BUS B TO A**



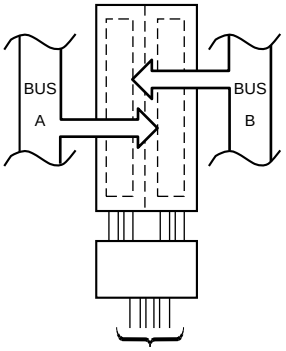

| xDIR | $\overline{\text{xOE}}$ | xCLKAB | xCLKBA | xSAB | xSBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS A TO B**



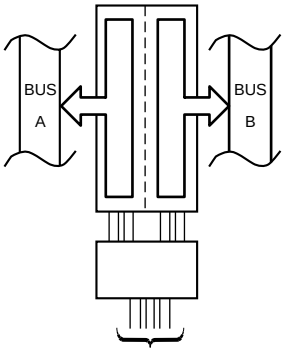

| xDIR | $\overline{\text{xOE}}$ | xCLKAB | xCLKBA | xSAB | xSBA |
|---|---|---|---|---|---|
| H | L | X | X | L | X |

**STORAGE FROM**
**A AND/OR B**




| xDIR | $\overline{\text{xOE}}$ | xCLKAB | xCLKBA | xSAB | xSBA |
|---|---|---|---|---|---|
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| X | H | ↑ | ↑ | X | X |

**TRANSFER STORES**
**DATA TO A AND/OR B**




| xDIR[1] | $\overline{\text{xOE}}$ | xCLKAB | xCLKBA | xSAB | xSBA |
|---|---|---|---|---|---|
| L | L | X | H or L | X | H |
| H | L | H or L | X | H | X |

**Note:**
1. Cannot transfer data to A bus and B bus simultaneously.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature with Power Applied | –40°C to +85°C |
| Input Voltage Range, $V_{IN}$ | –0.5V to $V_{CC}$ +4.6V |
| Output Voltage Range, $V_{OUT}$ | –0.5V to $V_{CC}$ +0.5V |
| DC Input Voltage | –0.5V to +5.0V |
| DC Output Current | 50 mA |
| Power Dissipation | 1.0W |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC Electrical Characteristics (Over the Operating Range, $T_A$ = –40°C to +85°C, $V_{CC}$ = 3.3V ±10%)

| Parameters | Description | Test Conditions[1] | Min. | Typ.[2] | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 2.3 | | 3.6 | V |
| $V_{IH}$[3] | Input HIGH Voltage | $V_{CC}$ = 2.3V to 2.7V | 1.7 | | | |
| | | $V_{CC}$ = 2.7V to 3.6V | 2.0 | | | |
| $V_{IL}$[3] | Input LOW Voltage | $V_{CC}$ = 2.3V to 2.7V | | | 0.7 | |
| | | $V_{CC}$ = 2.7V to 3.6V | | | 0.8 | |
| $V_{IN}$[3] | Input Voltage | | 0 | | $V_{CC}$ | |
| $V_{OUT}$[3] | Output Voltage | | 0 | | $V_{CC}$ | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = -100µA, $V_{CC}$ = Min. to Max. | $V_{CC}$ -0.2 | | | |
| | | $V_{IH}$ = 1.7V, $I_{OH}$ = -6mA, $V_{CC}$ = 2.3V | 2.0 | | | |
| | | $V_{IH}$ = 1.7V, $I_{OH}$ = -12mA, $V_{CC}$ = 2.3V | 1.7 | | | |
| | | $V_{IH}$ = 2.0V, $I_{OH}$ = -12mA, $V_{CC}$ = 2.7V | 2.2 | | | |
| | | $V_{IH}$ = 2.0V, $I_{OH}$ = -12mA, $V_{CC}$ = 3.0V | 2.4 | | | |
| | | $V_{IH}$ = 2.0V, $I_{OH}$ = -24mA, $V_{CC}$ = 3.0V | 2.0 | | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 100µA, $V_{IL}$ = Min. to Max. | | | 0.2 | |
| | | $V_{IL}$ = 0.7V, $I_{OL}$ = 6mA, $V_{CC}$ = 2.3V | | | 0.4 | |
| | | $V_{IL}$ = 0.7V, $I_{OL}$ = 12mA, $V_{CC}$ = 2.3V | | | 0.7 | |
| | | $V_{IL}$ = 0.8V, $I_{OL}$ = 12mA, $V_{CC}$ = 2.7V | | | 0.4 | |
| | | $V_{IL}$ = 0.8V, $I_{OL}$ = 24mA, $V_{CC}$ = 3.0V | | | 0.55 | |
| $I_{OH}$[3] | Output HIGH Current | $V_{CC}$ = 2.3V | | | -12 | mA |
| | | $V_{CC}$ = 2.7V | | | -12 | |
| | | $V_{CC}$ = 3.0V | | | -24 | |
| $I_{OL}$[3] | Output LOW Current | $V_{CC}$ = 2.3V | | | 12 | |
| | | $V_{CC}$ = 2.7V | | | 12 | |
| | | $V_{CC}$ = 3.0V | | | 24 | |

**DC Electrical Characteristics-Continued** (Over the Operating Range, $T_A$ = –40°C to +85°C, $V_{CC}$ = 3.3V ±10%)

| Parameters | Description | Test Conditions[1] | Min. | Typ.[2] | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IN}$ | Input Current | $V_{IN}$ = $V_{CC}$ or GND, $V_{CC}$ = 3.6V | | | ±5 | µA |
| $I_{IN}$ (HOLD) | Input Hold Current | $V_{IN}$ = 0.7V, $V_{CC}$ = 2.3V | 45 | | | |
| | | $V_{IN}$ = 1.7V, $V_{CC}$ = 2.3V | -45 | | | |
| | | $V_{IN}$ = 0.8V, $V_{CC}$ = 3.0V | 75 | | | |
| | | $V_{IN}$ = 2.0V, $V_{CC}$ = 3.0V | -75 | | | |
| | | $V_{IN}$ = 0 to 3.6V, $V_{CC}$ = 3.6V | | | ±500 | |
| $I_{OZ}$ | Output Current (3-STATE Outputs) | $V_{OUT}$ = $V_{CC}$ or GND, $V_{CC}$ = 3.6V | | | ±10 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 3.6V, $I_{OUT}$ = 0µA, $V_{IN}$ = GND or $V_{CC}$ | | | 40 | |
| $\Delta I_{CC}$ | Supply Current per Input @ TTL HIGH | $V_{CC}$ = 3.0V to 3.6V One Input at $V_{CC}$ - 0.6V Other Inputs at $V_{CC}$ or GND | | | 750 | |
| $C_I$ | Control Inputs | $V_{IN}$ = $V_{CC}$ or GND, $V_{CC}$ = 3.3V | | 3 | | pF |
| | Data Inputs | | | 6 | | |
| $C_O$ | Outputs | $V_O$ = $V_{CC}$ or GND, $V_{CC}$ = 3.3V | | 7 | | |

**Notes:**
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient and maximum loading.
3. Unused Control Inputs must be held HIGH or LOW to prevent them from floating.

## Timing Requirements

| Parameters | Description | | Conditions[1] | $V_{CC}$ = 2.5V ±0.2V | | $V_{CC}$ = 2.7V | | $V_{CC}$ = 3.3V ±0.3V | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| $F_{CLOCK}$ | Clock Frequency | | $C_L$ = 50pF $R_L$ = 500Ω | 0 | 150 | 0 | 150 | 0 | 150 | MHz |
| $t_W$ | Pulse Duration | CLKAB or CLKBA HIGH or LOW | | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{SU}$ | Setup Time | A Before CLKAB↑ or B Before CLKBA↑ | | 1.6 | | 1.7 | | 1.4 | | |
| $t_H$ | Hold Time | A After CLKAB↑ or B After CLKBA↑ | | 0.6 | | 0.4 | | 0.7 | | |

## Switching Characteristics over Operating Range[1]

| Parameters | From (INPUT) | To (OUTPUT) | Conditions[1] | $V_{CC}$ = 2.5V ±0.2V | | $V_{CC}$ = 2.7V | | $V_{CC}$ = 3.3V ±0.3V | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| $f_{MAX}$ | | | $C_L$ = 50pF<br>$R_L$ = 500Ω | 150 | | 150 | | 150 | | MHz |
| $t_{PD}$ | A or B | B or A | | 1.0 | 4.8 | | 4.5 | 1.0 | 3.9 | ns |
| $t_{PD}$ | CLKAB or CLKBA | A or B | | | 5.6 | | 5.2 | | 4.5 | |
| $t_{PD}$ | SAB or SBA | | | | 6.8 | | 6.4 | | 5.3 | |
| $t_{EN}$ | OE | | | | 6.5 | | 6.2 | | 5.1 | |
| $t_{DIS}$ | OE | | | 1.8 | 5.7 | | 5.0 | 1.4 | 4.7 | |
| $t_{EN}$ | DIR | | | 1.0 | 7.8 | | 6.2 | 1.0 | 5.1 | |
| $t_{DIS}$ | DIR | | | 1.7 | 6.5 | | 6.0 | 1.1 | 5.3 | |
| | **Description** | | | | | | | | | |
| $\Delta t/\Delta v$[3] | Input Transition Rise or Fall | | | 0 | 10 | 0 | 10 | 0 | 10 | ns/V |

**Notes:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Recommended operating condition.

## Operating Characteristics, $T_A$ = 25°C

| Parameter | | Test Conditions | $V_{CC}$ = 2.5V ±0.2V | $V_{CC}$ = 3.3V ±0.3V | Units |
|---|---|---|---|---|---|
| | | | Typ. | | |
| $C_{PD}$ Power Dissipation Capacitance | Outputs Enabled | $C_L$ = 50pF, f = 10 MHz | 39 | 43 | pF |
| | Outputs Disabled | | 10 | 12 | |