CS3011
CS3012

Precision Low-voltage Amplifier; DC to 1 kHz

Features

- Low Offset: 10 µV Max
- Low Drift: 0.05 µV/°C Max
- Low Noise
  - 12 nV/√Hz @ 0.5 Hz
  - 0.1 to 10 Hz = 250 nVp-p
  - 1/f corner @ 0.08 Hz
- Open-loop Voltage Gain
  - 300 dB Typ
  - 200 dB Min
- Rail-to-rail Output Swing
- Slew Rate: 2 V/µs

Applications

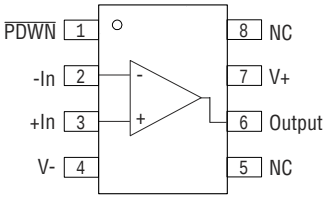
- Thermocouple/Thermopile Amplifiers
- Load Cell and Bridge Transducer Amplifiers
- Precision Instrumentation
- Battery-powered Systems

Description

The CS3011 single amplifier and the CS3012 dual amplifier are designed for precision amplification of low-level signals and are ideally suited to applications that require very high closed-loop gains. These amplifiers achieve excellent offset stability, super-high open-loop gain, and low noise over time and temperature. The devices also exhibit excellent CMRR and PSRR. The common mode input range includes the negative supply rail. The amplifiers operate with any total supply voltage from 2.7 V to 6.7 V (±1.35 V to ±3.35 V).

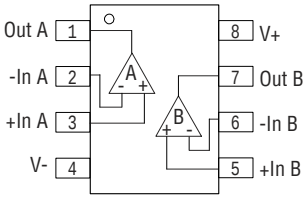
Pin Configurations

CS3011

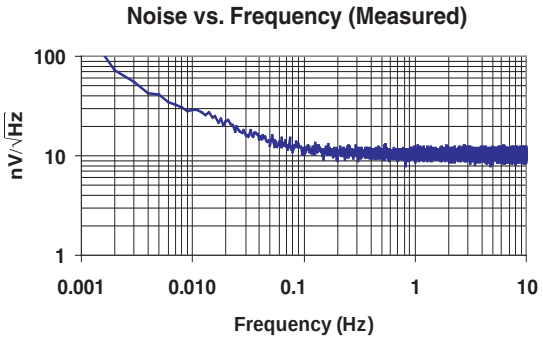


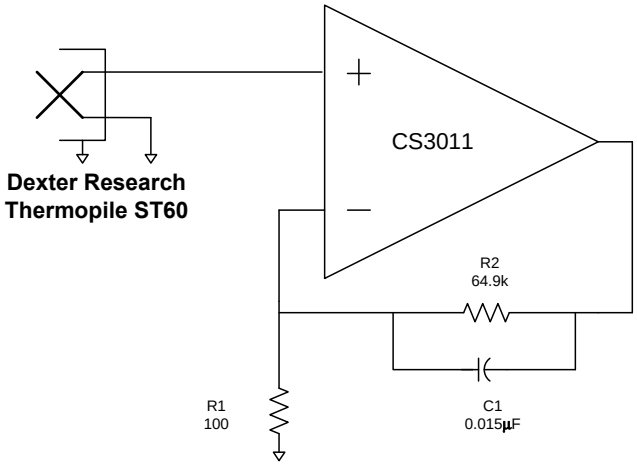
8-lead SOIC

CS3012



8-lead SOIC





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ELECTRICAL CHARACTERISTICS

V+ = +5 V, V- = 0V, VCM = 2.5 V (Note 1)

Parameter			CS3011/CS3012 Min	Typ	Max	Unit
Input Offset Voltage	(Note 2)	•	-	-	±10	µV
Average Input Offset Drift	(Note 2)	•	-	±0.01	±0.05	µV/ºC
Long Term Input Offset Voltage Stability				(Note 3)		
Input Bias Current	T_A = 25º C	 •	- -	±50 -	- ±1000	pA
Input Offset Current	T_A = 25º C	 •	- -	±100 -	- ±2000	pA
Input Noise Voltage Density	R_S = 100 Ω, f_0 = 1 Hz R_S = 100 Ω, f_0 = 1 kHz		- -	12 12		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
Input Noise Voltage	0.1 to 10 Hz		-	250		nV_{p-p}
Input Noise Current Density	f_0 = 1 Hz		-	100		$fA/\sqrt{Hz}$
Input Noise Current	0.1 to 10 Hz		-	1.9		pA_{p-p}
Input Common Mode Voltage Range		•	-0.1	-	(V+)-1.25	V
Common Mode Rejection Ratio (dc)	(Note 4)	•	115	120	-	dB
Power Supply Rejection Ratio		•	120	136	-	dB
Large Signal Voltage Gain	R_L = 2 kΩ to V+/2 (Note 5)	•	200	300	-	dB
Output Voltage Swing	R_L = 2 kΩ to V+/2 R_L = 100 kΩ to V+/2	•	+4.7	- +4.99	-	V V
Slew Rate	R_L = 2 k, 100 pF			2	-	V/µs
Overload Recovery Time			-	600	-	µs
Supply Current	CS3011 CS3012 $\overline{PWDN}$ active (CS3011 Only) (Note 6)	• • •	-	0.9 1.7	1.4 2.4 15	mA mA µA
$\overline{PWDN}$ Threshold	(Note 6)	•	(V+) -1.0			
Start-up Time	(Note 7)	•	-	9	12	ms

Notes:
1. Symbol "•" denotes specification applies over -40 to +85 ° C.
2. This parameter is guaranteed by design and laboratory characterization. Thermocouple effects prohibit accurate measurement of these parameters in automatic test systems.
3. 1000-hour life test data @ 125 °C indicates randomly distributed variation approximately equal to measurement repeatability of 1 µV.
4. Measured within the specified common mode range limits.
5. Guaranteed within the output limits of (V+ -0.3 V) to (V- +0.3 V). Tested with proprietary production test method.
6. $\overline{PWDN}$ input has an internal pullup resistor to V+ of approximately 800 kΩ and is the major source of current consumption when $\overline{PWDN}$ is active (low).
7. The device has a controlled start-up behavior due to its complex open loop gain characteristics. Start-up time applies to when supply voltage is applied or when $\overline{PDWN}$ is released.

ABSOLUTE MAXIMUM RATINGS

Parameter		Min T	yp	Max	Unit
Supply Voltage	[(V+) - (V-)]			6.8	V
Input Voltage		V- -0.3		V+ +0.3	V
Storage Temperature Range			-65	+150	ºC

2. TYPICAL PERFORMANCE PLOTS

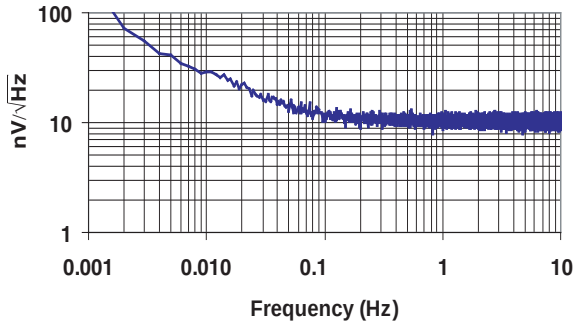


Figure 1. Noise vs. Frequency (Measured)

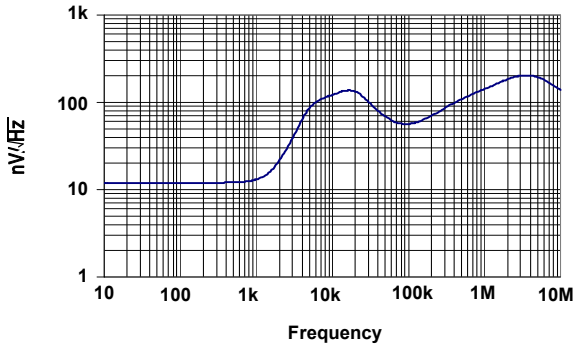


Figure 2. Noise vs. Frequency

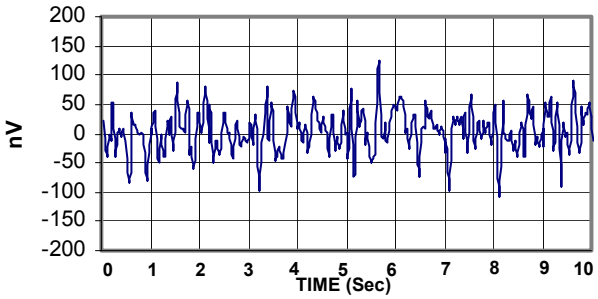


Figure 3. 0.01 Hz to 10 Hz Noise

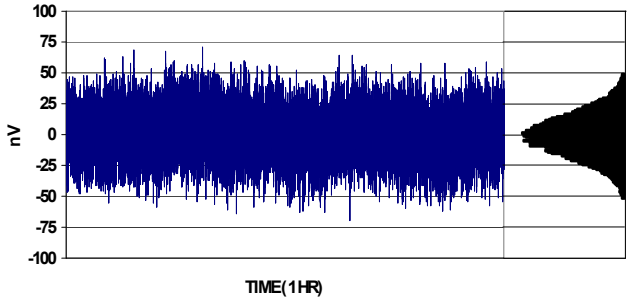


Figure 4. Offset Voltage Stability (DC to 3.2 Hz)

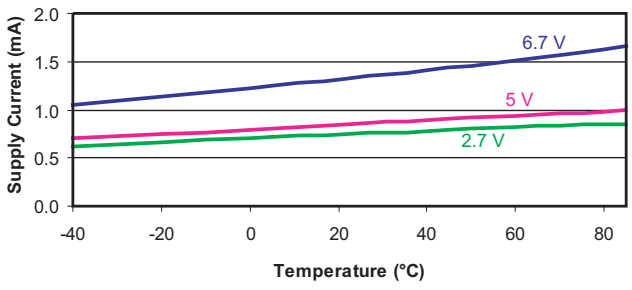


Figure 5. Supply Current vs. Temperature, CS3011

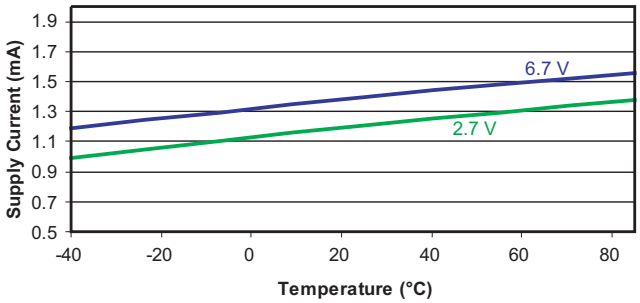


Figure 6. Supply Current vs. Temperature, CS3012

Typical Performance Plots (Cont.)

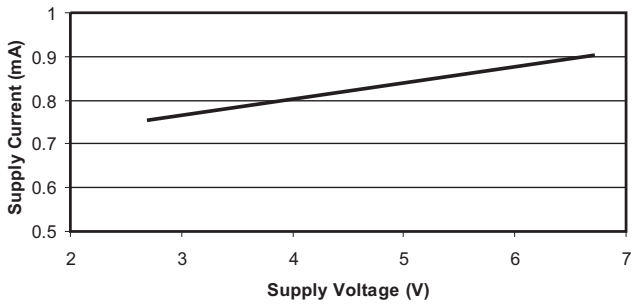


Figure 7. Supply Current vs. Voltage, CS3011

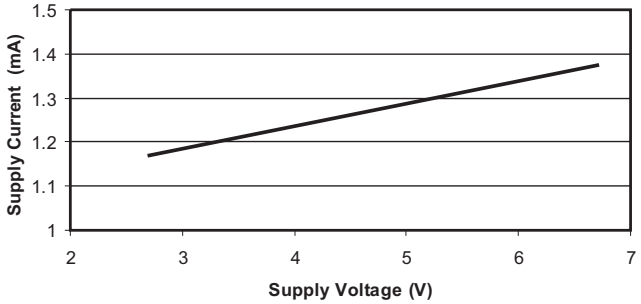


Figure 8. Supply Current vs. Voltage, CS3012

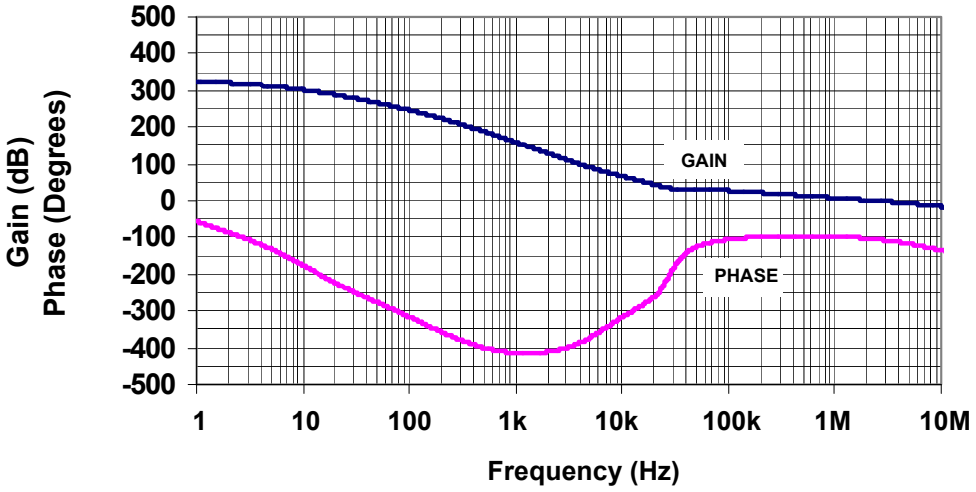


Figure 9. Open Loop Gain and Phase vs Frequency

Typical Performance Plots (Cont.)

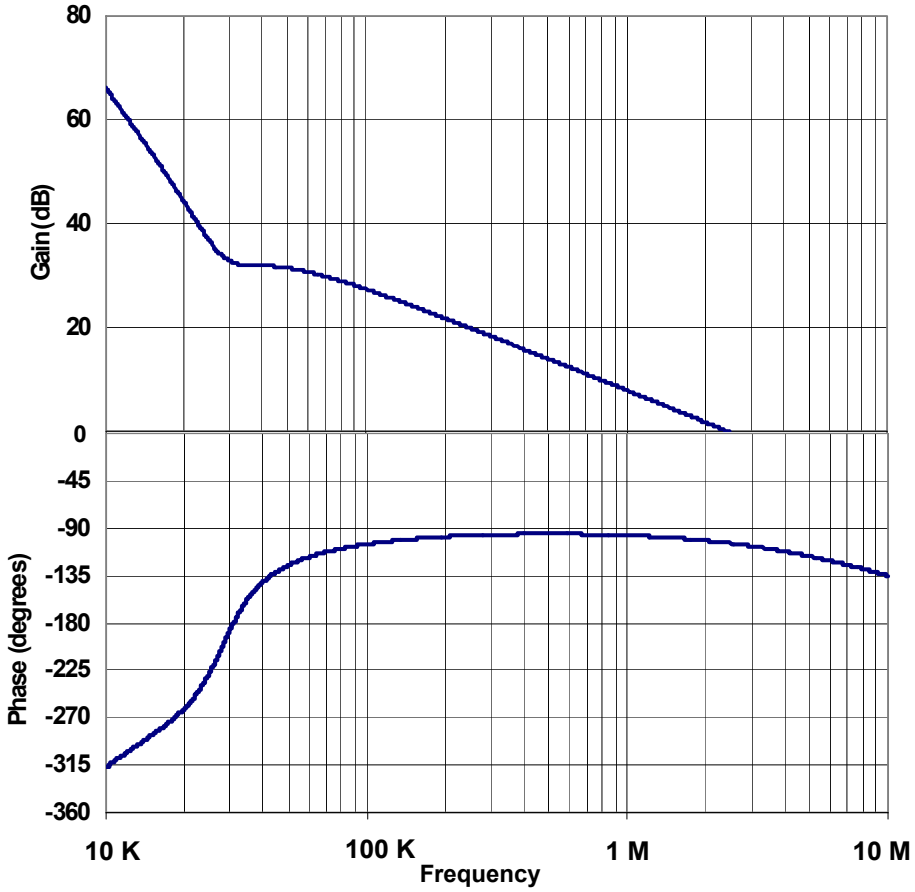


Figure 10. Open Loop Gain and Phase vs Frequency (Expand-

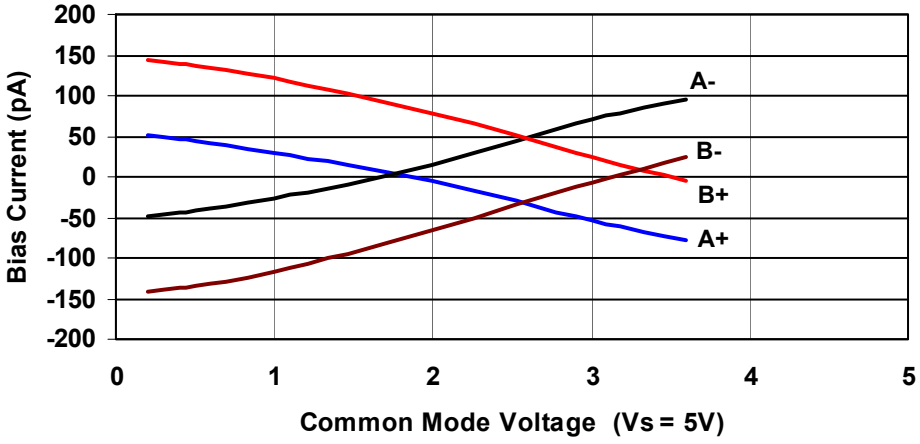


Figure 11. Input Bias Current vs Common Mode Voltage (CS3012)

Typical Performance Plots (Cont.)

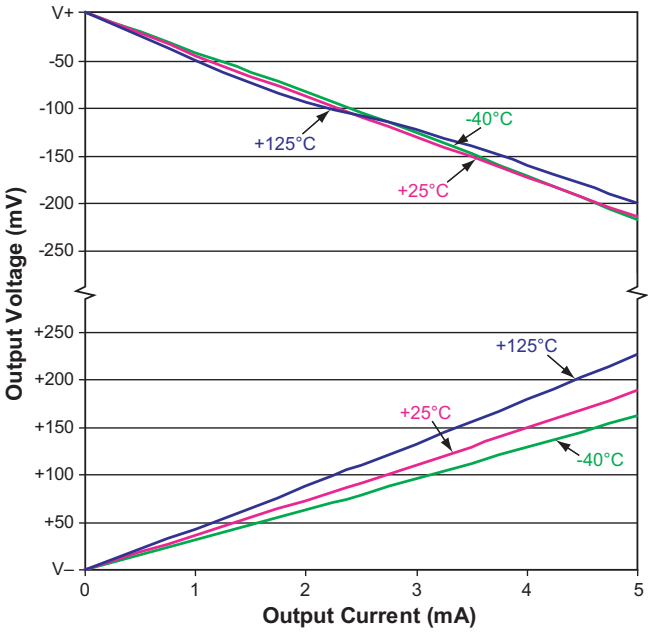


Figure 12. Voltage Swing vs. Output Current (2.7 V)

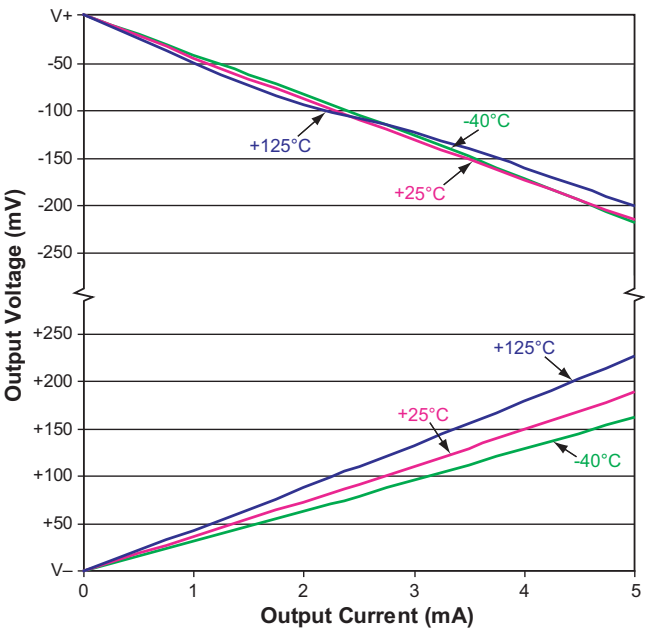


Figure 13. Voltage Swing vs. Output Current (5 V)

3. CS3011/CS3012 OVERVIEW

The CS3011/CS3012 amplifiers are designed for precision measurement of signals from DC to 1 kHz when operating from a supply voltage of +2.7 V to +6.7 V (±1.35 to ±3.35 V). The amplifiers are designed with a patented architecture that utilizes multiple amplifier stages to yield very high open loop gain at frequencies of 1 kHz and below. The amplifiers yield low noise and low offset drift while consuming relatively low supply current. An increase in noise floor above 1 kHz is the result of intermediate stages of the amplifier being operated at very low currents. The amplifiers are intended for amplifying small signals with large gains in applications where the output of the amplifier can be band-limited to frequencies below 1 kHz.

3.1 Open Loop Gain and Phase Response

Figure 14 illustrates the open loop gain and phase response of the CS3011/CS3012. The gain slope of the amplifier is about –100 dB/decade between 500 Hz and 30 kHz and transitions to –20 dB/decade between 30 kHz and its unity gain crossover frequency at about 2.4 MHz. Phase margin at unity gain is about 70 degrees; gain margin is about 20 dB.

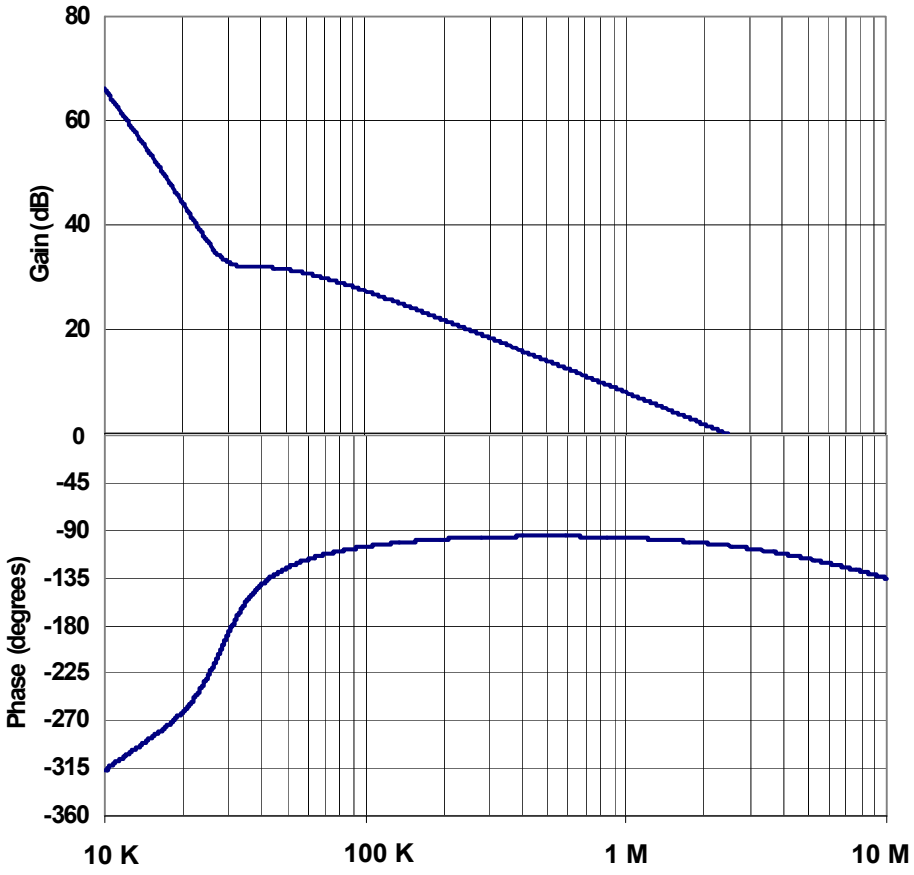


Figure 14. CS3011/CS3012 Open Loop Gain and Phase Response

3.2 Open Loop Gain and Stability Compensation

3.2.1 Discussion

The CS3011 and CS3012 achieve ultra-high open loop gain. Figure 15 illustrates the amplifier in a non-inverting gain configuration. The open loop gain and phase plots indicate that the amplifier is stable for closed-loop gains less than 50 V/V. For a gain of 50, the phase margin is between 40° and 60° depending upon the loading conditions. As shown in Figure 16 on page 11, the op amp has an input capacitance at the + and – signal inputs of typically 50 pF. This capacitance adds an additional pole in the loop gain transfer function at a frequency of $f = 1/(2\pi R^*C_{in})$ where R is the parallel combination of R1 and R2 (R1 || R2). A higher value for R produces a pole at a lower frequency, thus reducing the phase margin. R1 is recommended to be less than or equal to 100 ohms, which results in a pole at 30 MHz or higher. If a higher value of R1 is desired, a compensation capacitor (C2) should be added in parallel with R2. C2 should be chosen such that $R2^*C2 \geq R1^*C_{in}$.

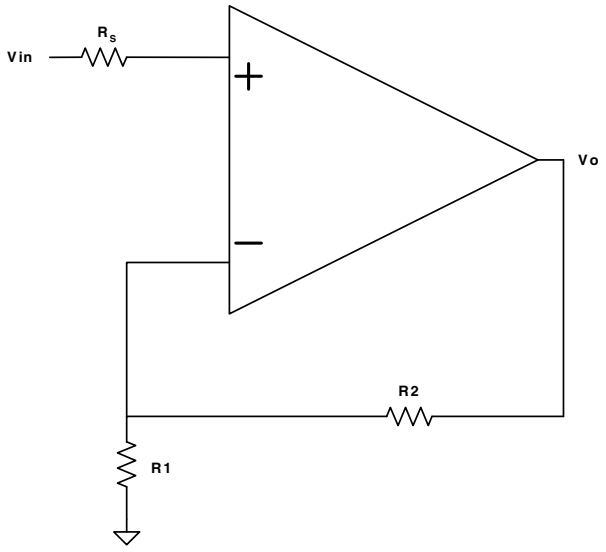


Figure 15. Non-Inverting Gain Configuration

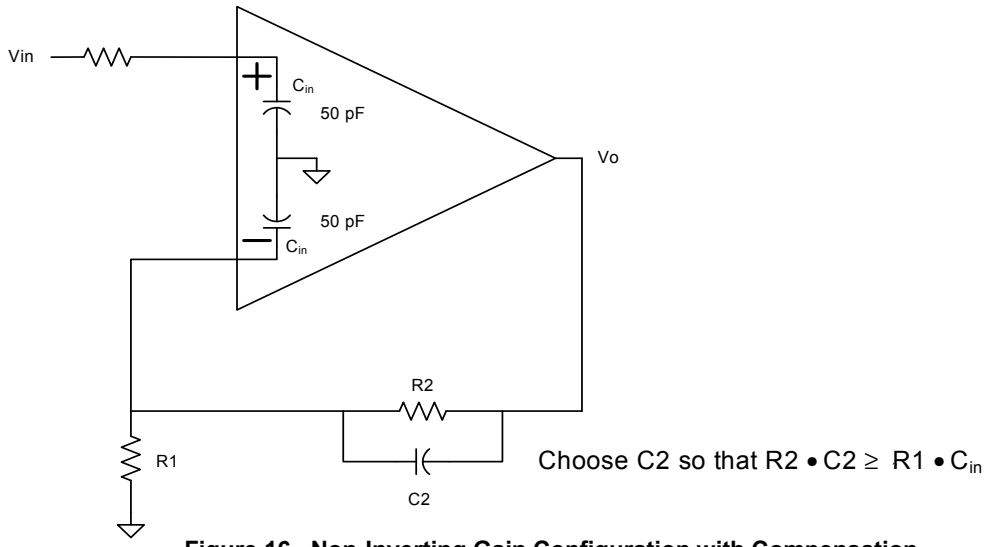


Figure 16. Non-Inverting Gain Configuration with Compensation

The feedback capacitor C2 is required for closed-loop gains greater than 50 V/V. The capacitor introduces a pole and a zero in the loop gain transfer function.

$$T = \frac{-\left(1 + \frac{s}{z_1}\right)}{\left(1 + \frac{s}{p_1}\right)} A_{ol}$$

$$P_1 = \frac{1}{2\pi(R_1 \| R_2)C_2} \cong \frac{1}{2\pi(R_1 C_2)} \qquad \text{for} \qquad R_2 \gg R_1$$

$$Z_1 = \frac{1}{2\pi(A \times R_1)C_2} \qquad \text{where} \qquad |A| = \frac{R_2}{R_1}$$

$$Z_1 = \frac{1}{2\pi(R_2)C_2}$$

This indicates that the separation of the pole and the zero is governed by the closed loop gain. It is required that the zero falls on the steep slope (–100 dB/decade) of the loop gain plot so that there is some gain higher than 0 dB (typically 20 dB) at the hand-over frequency (the frequency at which the slope changes from – 100 dB/decade to –20 dB/decade).

The loop gain plot shown in Figure 17 illustrates the unity gain configuration, and indicates how this is modified when using the amplifier in a higher gain configuration with compensation. If it is configured for higher gain, for example, 60 dB, the x-axis will move up by 60 dB (line B). Capacitor C2 adds a zero and a pole. The modified plot indicates the effects of introducing the pole and zero due to capacitor C2. The pole can be located at any frequency higher than the hand-over frequency, the zero has to be at a frequency lower than the hand-over frequency so as to provide adequate gain margin. The separation between the pole and the zero is governed by the closed loop gain. The zero (z_1) occurs at the intersection of the –100 dB/decade and –80 dB/decade slopes. The point X in the figure should be at closed loop gain plus 20 dB gain margin. The value for C2 = 1/(2πR1p1). Using p1 = 500 kHz works very well and is independent of gain. As the closed loop gain is changed, the zero location is also modified if R1 remains fixed. Capacitor C2 can be increased in value to limit the amplifier's rising noise above 1 kHz.

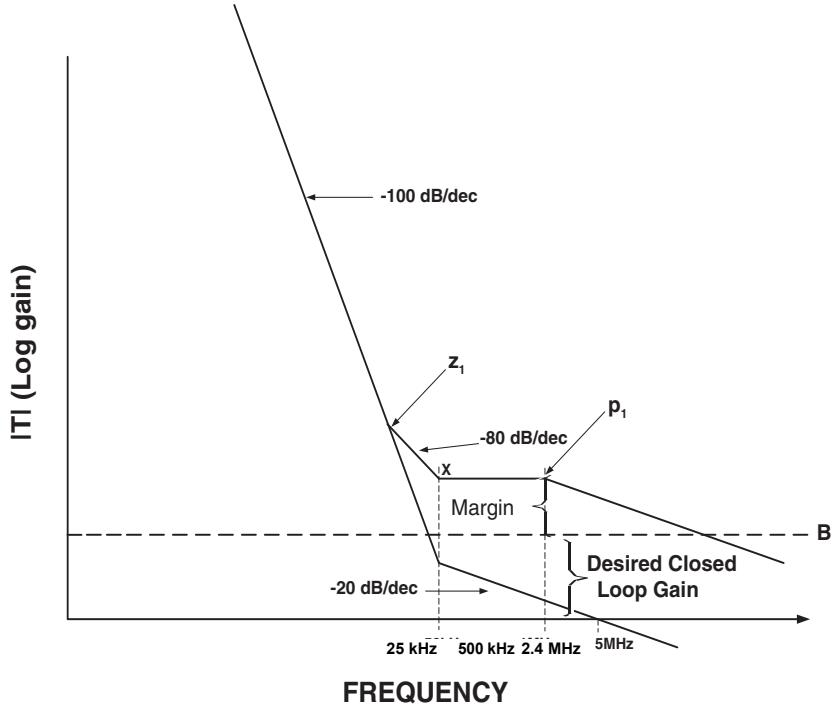


Figure 17. Loop Gain Plot: Unity Gain and with Pole-Zero Compensation

3.2.2 *Gain Calculations Summary and Recommendations*

Condition #1: |Av| ≤ 50 and R1 ≤ 100 Ω

The Opamp is inherently stable for |Av| ≤ 50 and R1 ≤ 100 Ω. No C2 compensation capacitor across R2 is required.

- |Av| = 1 configuration has 70° phase margin and 20 dB gain margin.
- |Av| = 50 configuration has phase margin between 40° for C_{LOAD} ≤ 100 pF and 60° for C_{LOAD} = 0 pF.

Condition #2: |Av| ≤ 50 and R1 > 100 Ω

Compensation capacitor C2 across R2 is required. Calculate C2 using the following formula:

- C2 ≥ (R1 • C_{in}) / R2, where Cin = 50 pF

Condition #3: |Av| > 50

Compensation capacitor C2 across R2 is required. Calculate and verify a value for C2 using the following steps.

Calculate the Compensation Capacitor Value:

1) Calculate a value for C2 using the following formula:

   C2 = 1 / [2π (R1||R2) • P1], where P1 = 1 MHz

To simplify the calculation, set the pole of the filter to P1 = 1 MHz. P1 must be set higher than the opamp's internal 50 kHz crossover frequency.

2) Calculate a second value for C2 using the following formula:

   C2 ≥ (R1 • C_{in}) / R2, where Cin = 50 pF

3) Use the larger of the two values calculated in steps 1 & 2.

Verify the Opamp Compensation:

Verify the opamp compensation using the open-loop gain and phase response Bode plot in Figure 14. Plot the calculated closed loop gain transfer function and verify the following design criteria are met:

- Pole P1 > opamp internal 50 kHz crossover frequency
  - P1 = 1 / [2π (R1||R2) • C2], where P1 = 1 MHz
  - To simplify the calculation, set the pole to P1 = 1 MHz.
- Z1 < opamp internal 50 kHz crossover frequency
  - Z1 = 1 / (2π R2 • C2)
- Gain margin above the open-loop gain transfer function is required. A gain margin of +20 dB above the open loop gain transfer function is optimal.

3.3 Powerdown (PDWN)

The CS3011 single amplifier provides a powerdown function on pin 1. If this pin is left open the amplifier will operate normally. If the powerdown is asserted low, the amplifier enters a powered down state. There is a pull-up resistor (approximately 800 kohm) inside the amplifier from pin 1 to the V+ supply. The current through this pull-up resistor is the main source of current drain in the powerdown state.

3.4 Applications

The CS3011 and CS3012 amplifiers are optimum for applications that require high gain and low drift. Figure 18 illustrates a thermopile amplifier with a gain of 650 V/V. The thermopile outputs only a few millivolts when subjected to infrared radiation. The amplifier is compensated and bandlimited by C1 in combination with R2.

Figure 19 on page 14 illustrates a load cell bridge amplifier with a gain of 768 V/V. The load cell is excited with +5 V and has a 1 mV/V sensitivity. Its full scale output signal is amplified to produce a fully differential ±3.8 V into the CS5510/12 A/D converter. This circuit operates from +5 V.

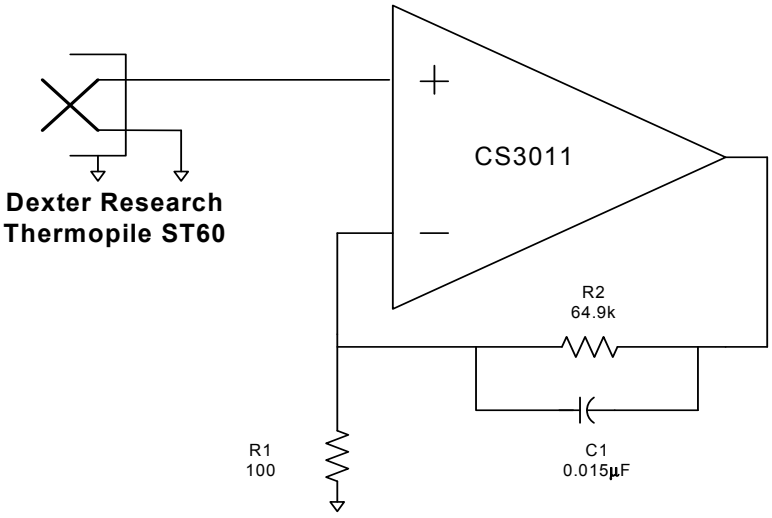


Figure 18. Thermopile Amplifier with a Gain of 650 V/V

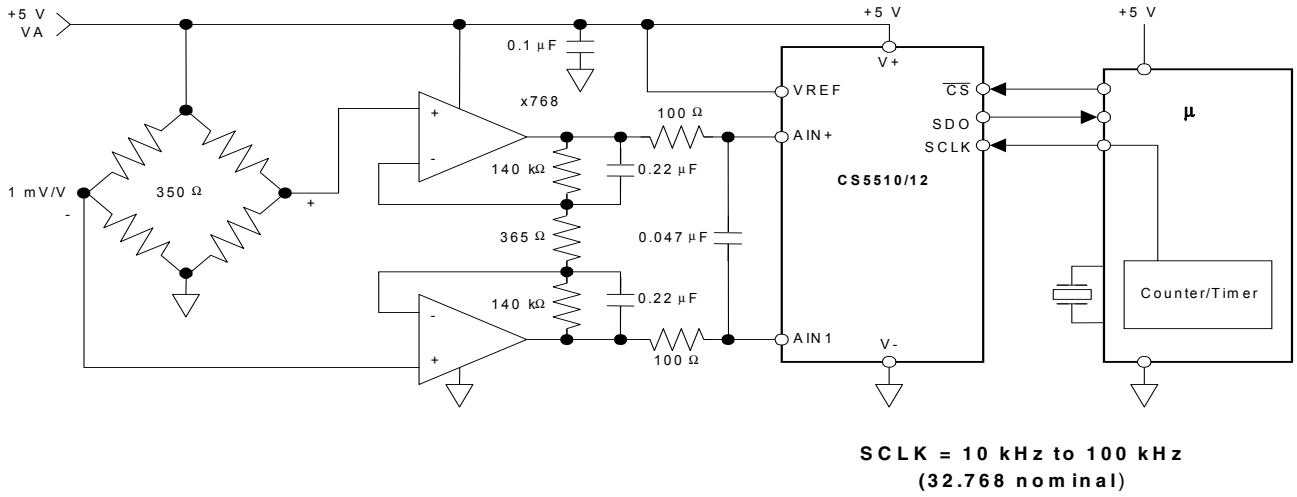


Figure 19. Load Cell Bridge Amplifier and A/D Converter

4. ORDERING INFORMATION

Model	Temperature	Package
CS3011-ISZ	-40 to +85 °C	8-pin SOIC, Lead Free
CS3012-ISZ		

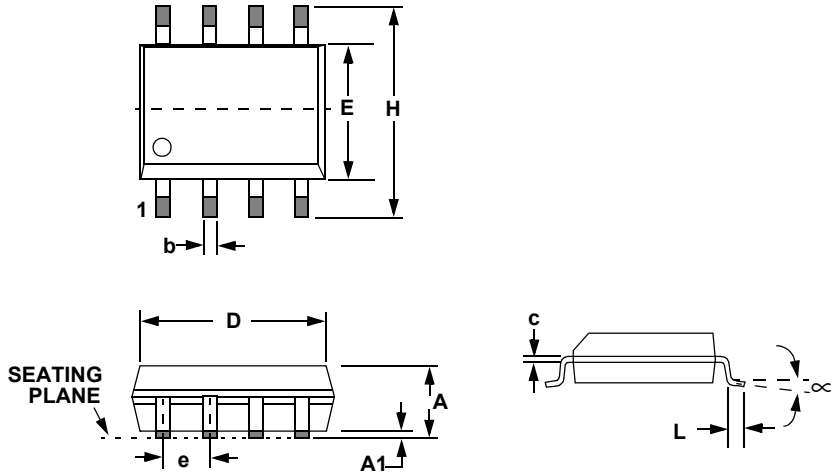
5. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS3011-ISZ	260 °C	2	365 Days
CS3012-ISZ			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

6. PACKAGE DRAWING

8L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A 0.0	53	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

JEDEC # : MS-012

7. REVISION HISTORY

Revision	Date	Changes
F2	SEP 2004	Added lead-free device ordering information.
F3	AUG 2005	Added MSL specifications. Updated legal notice. Added leaded (Pb) devices.
F4	AUG 2006	Updated *Typical Performance Plots*. Removed Powerdown feature.
F5	NOV 2007	Added additional information regarding open-loop and gain stability compensation.
F6	JUL 2009	Removed lead-containing SOICs from ordering information.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com