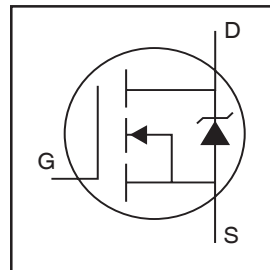


# IRFB4215

HEXFET® Power MOSFET

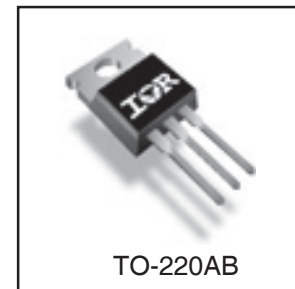
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Optimized for SMPS Applications



$V_{DSS} = 60V$
$R_{DS(on)} = 9.0m\Omega$
$I_D = 115A^{(8)}$

## Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.



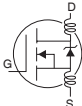
## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	115 <sup>(8)</sup>	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	81	
$I_{DM}$	Pulsed Drain Current <sup>(1)(7)</sup>	360	
$P_D @ T_C = 25^\circ C$	Power Dissipation	270	W
	Linear Derating Factor	1.8	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_{AR}$	Avalanche Current <sup>(1)</sup>	85	A
$E_{AR}$	Repetitive Avalanche Energy <sup>(1)</sup>	18	mJ
dv/dt	Peak Diode Recovery dv/dt <sup>(3)(7)</sup>	4.7	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

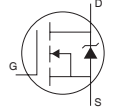
## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.56	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.066	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	9.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 54A ④ ⑦
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	61	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 54A ④ ⑦
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 48V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	170	nC	I <sub>D</sub> = 64A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	39		V <sub>DS</sub> = 48V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	59		V <sub>GS</sub> = 10V, See Fig. 6 and 13 ⑦
t <sub>d(on)</sub>	Turn-On Delay Time	—	22	—	ns	V <sub>DD</sub> = 30V
t <sub>r</sub>	Rise Time	—	160	—		I <sub>D</sub> = 64A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	77	—		R <sub>G</sub> = 6.2Ω
t <sub>f</sub>	Fall Time	—	110	—		V <sub>GS</sub> = 10V, See Fig. 10 ④ ⑦
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	4080	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	840	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	180	—		f = 1.0MHz, See Fig. 5 ⑦
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	1080 ⑤	220 ⑥		mJ

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	115 ⑧	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	360		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 90A, V <sub>GS</sub> = 0V ④ ⑦
t <sub>rr</sub>	Reverse Recovery Time	—	78	120	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 64A
Q <sub>rr</sub>	Reverse Recovery Charge	—	250	380	nC	di/dt = 100A/μs ④ ⑦
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T<sub>J</sub> = 25°C, L = 60μH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 85A, V<sub>GS</sub> = 10V (See Figure 12)
- ③ I<sub>SD</sub> ≤ 90A, di/dt ≤ 250A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ This is a typical value at device destruction and represents operation outside rated limits.
- ⑥ This is a calculated value limited to T<sub>J</sub> = 175°C.
- ⑦ This is tested with same test conditions as the existing data sheet
- ⑧ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

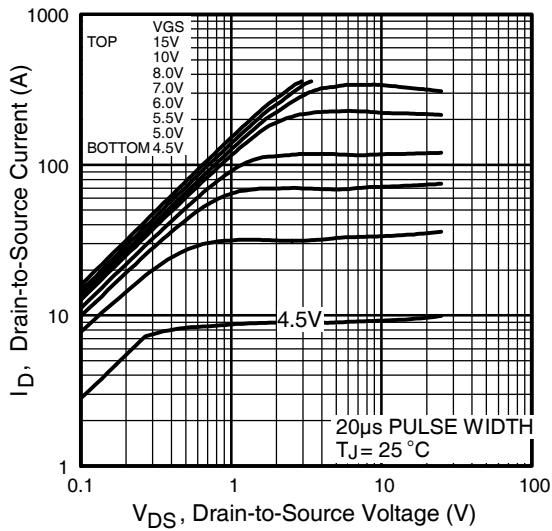


Fig 1. Typical Output Characteristics

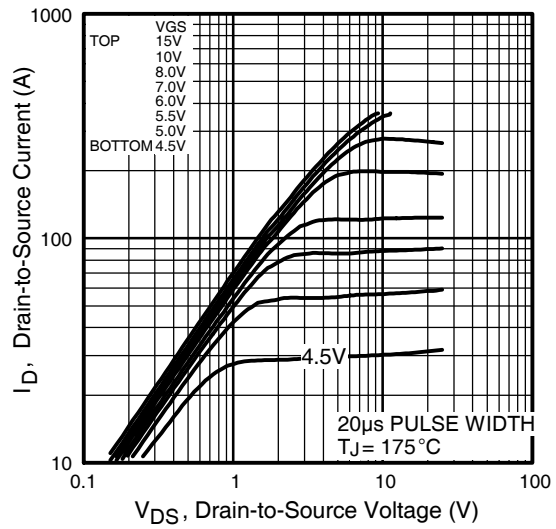


Fig 2. Typical Output Characteristics

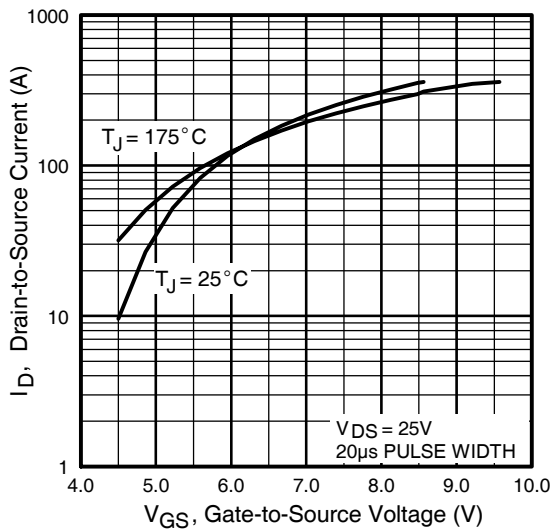


Fig 3. Typical Transfer Characteristics

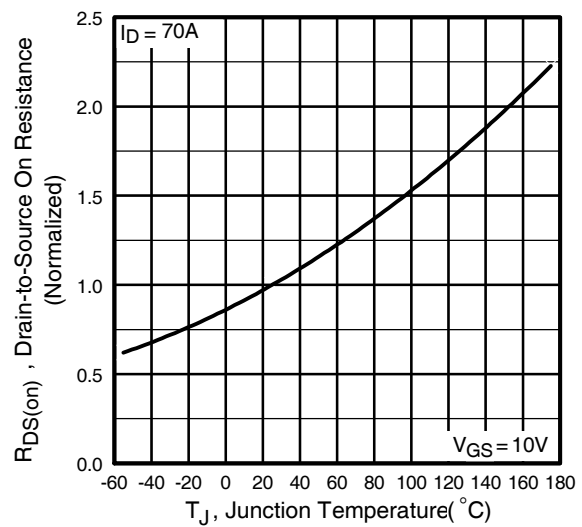
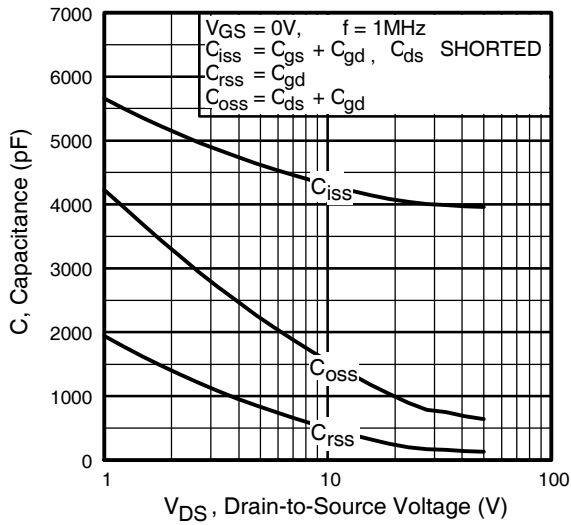
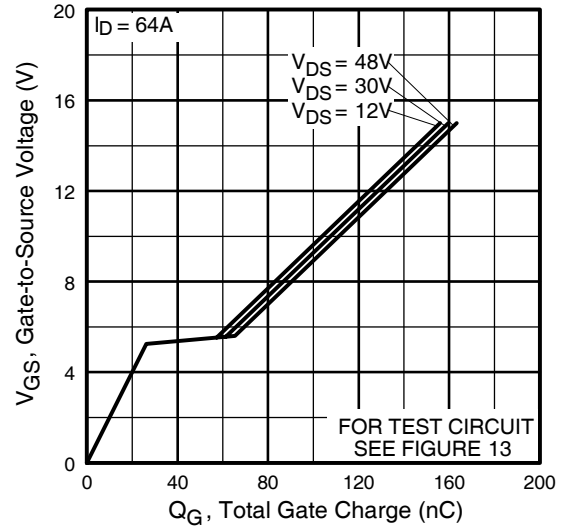


Fig 4. Normalized On-Resistance Vs. Temperature

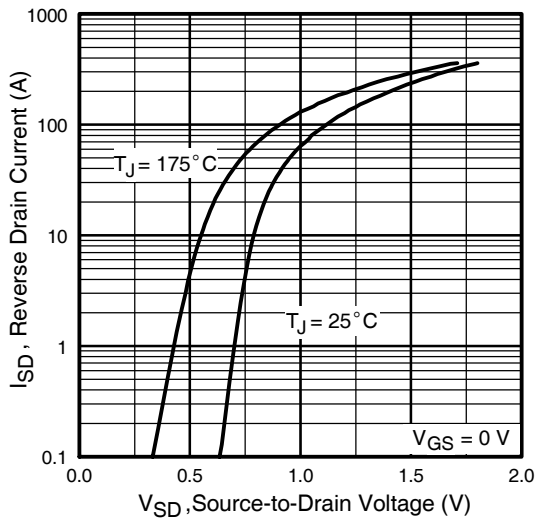
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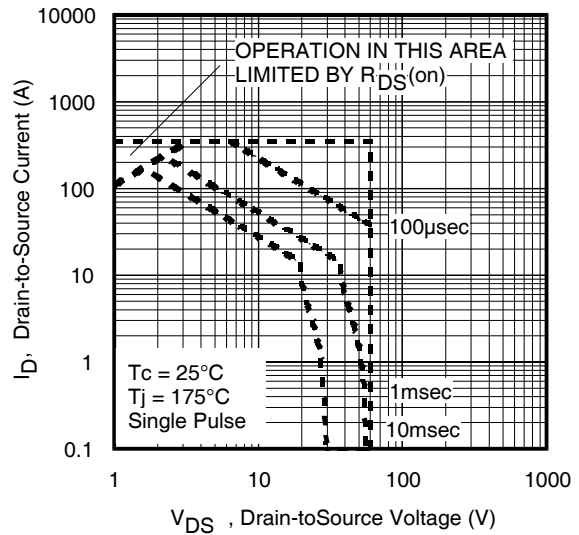
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

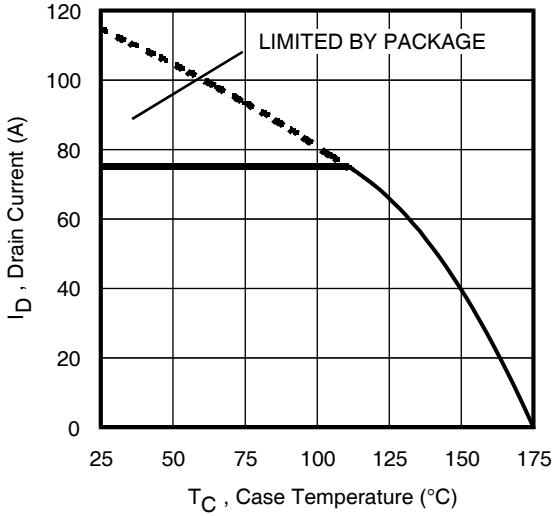


Fig 9. Maximum Drain Current Vs. Case Temperature

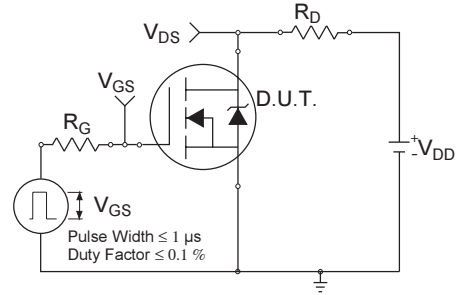


Fig 10a. Switching Time Test Circuit

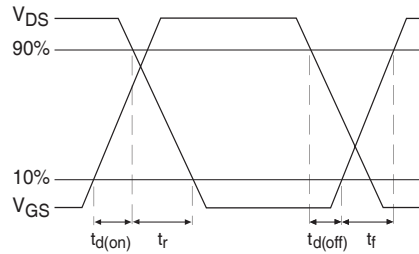


Fig 10b. Switching Time Waveforms

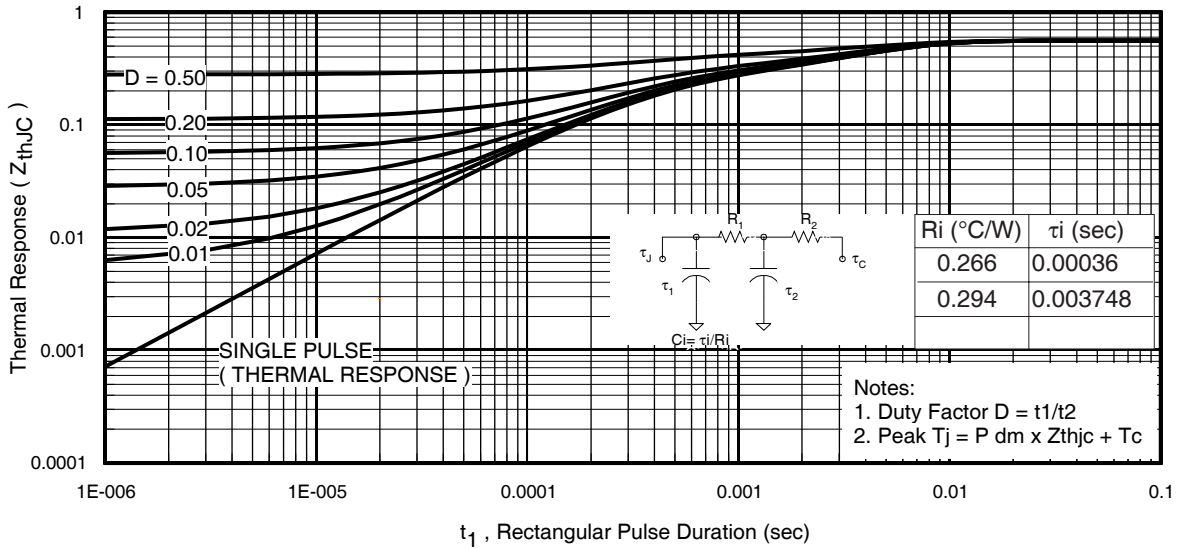
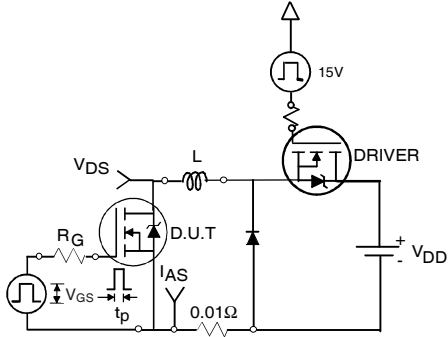
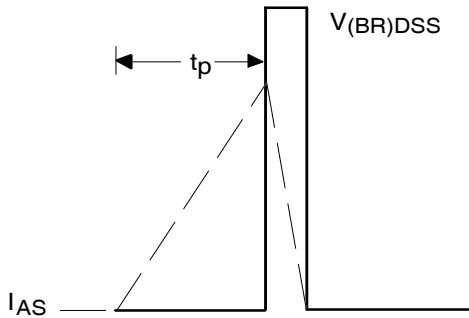


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

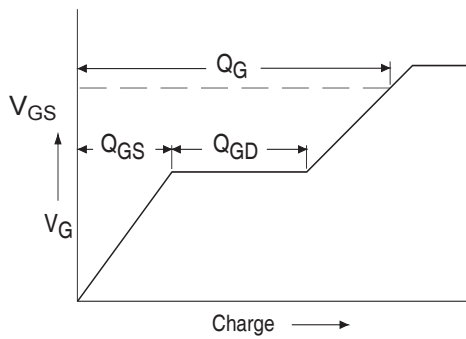
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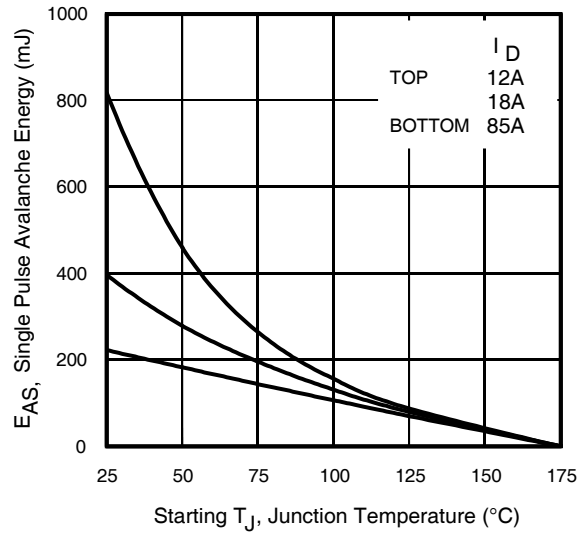
**Fig 12a.** Unclamped Inductive Test Circuit



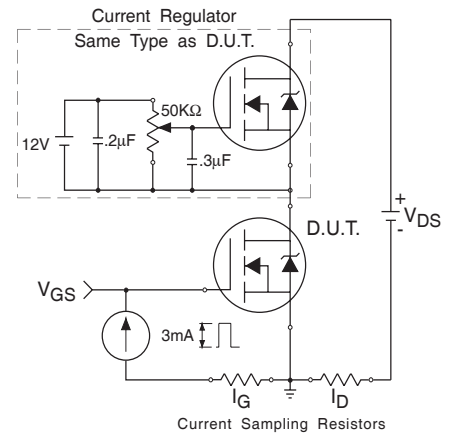
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

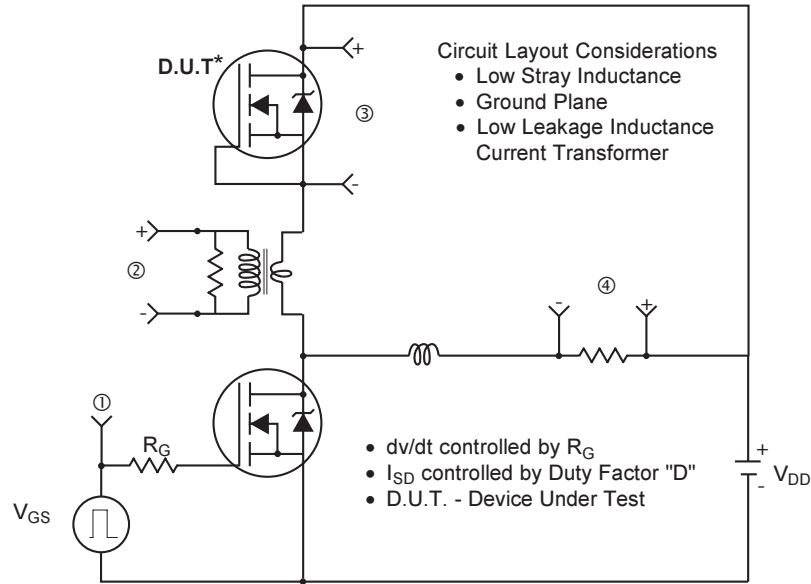


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

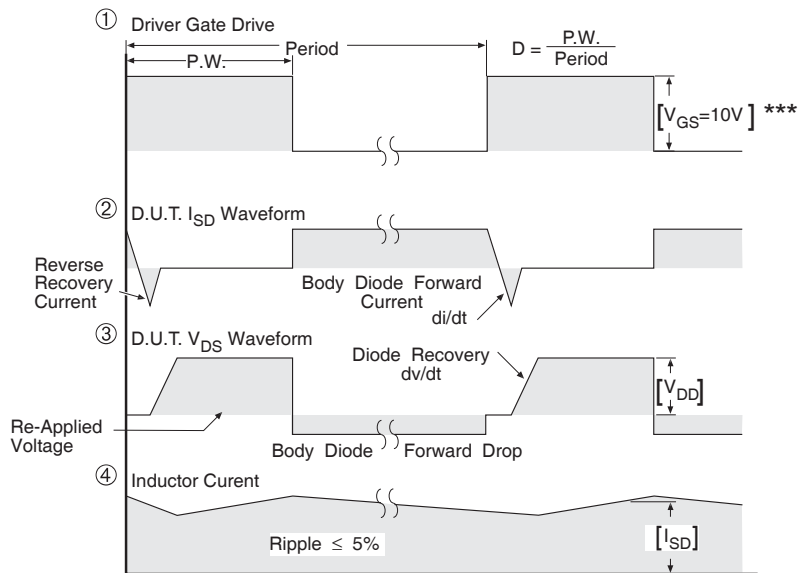


**Fig 13b.** Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

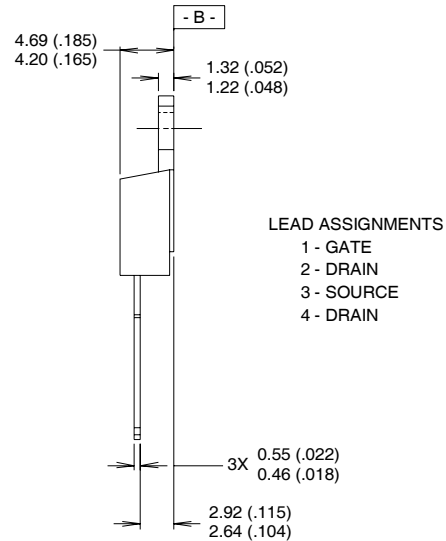
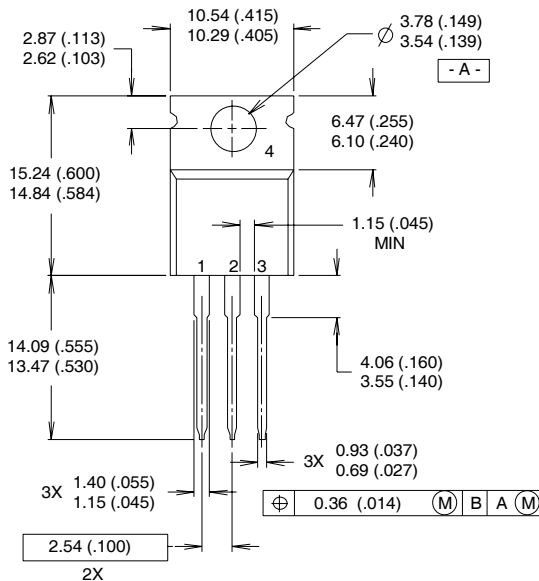
Fig 14. For N-channel HEXFET® power MOSFETs

# IRFB4215

International  
**IR** Rectifier

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

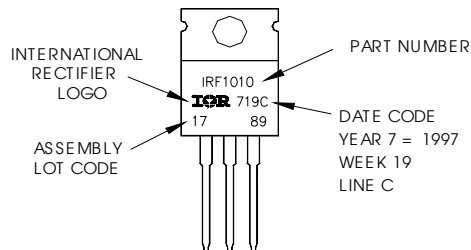


### NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



TO-220AB packages are not recommended for Surface Mount Application.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Automotive [Q101] market.  
 Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
 TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>