MAX3601

Laser Driver for Projectors

General Description

The MAX3601 laser driver for pico projectors supports video imaging with red, blue, and green lasers. Each output includes two 8-bit digital-to-analog converters (DACs) with programmable gain and up to 400mA driving capability per channel. DAC A has a full-scale current up to 320mA, while DAC B has full-scale current up to 80mA. All three channels can be combined into a single channel with up to 1.2A drive capability.

Maxim's patented technology allows pulsed current to operate lasers efficiently while reducing speckle. This feature operates from the video data clock. The driver is available in a 3.0mm x 3.5mm, 42-bump wafer-level package for commercial applications and a 5mm x 5mm, 40-pin TQFN package for industrial and automotive applications.

Applications

RGB Pico Laser Projector

Laser Light Source for LCOS Projectors

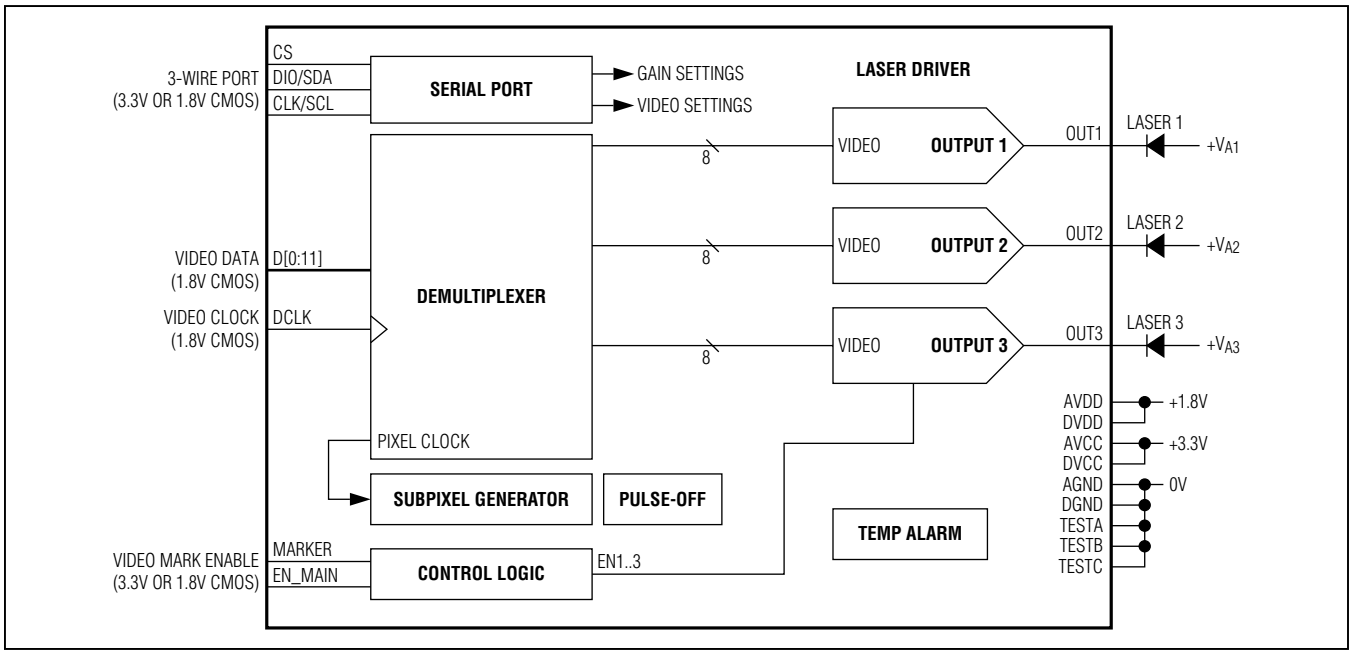
High-Current LED or Laser Pulse Generator

Ordering Information appears at end of data sheet.

Benefits and Features

- **Integrates Three Current-Output Laser Drivers**
  - **Compatible with Most Red, Blue, and Green Lasers**
  - **8-Bit Video DACs, DC to 167MHz operation**
  - **Patented Pulsing Feature Reduces Laser Speckling**
  - **1ns Output Switching Time**
  - **Pulse Switching Speed Enhancer**
- **Minimizes PCB Area with Functional Integration**
  - **SPI or I²C Serial Port Control**
  - **1.8V to 3.3V Operation**
  - **8-Bit Gain Adjustment**
  - **Programmable Pulse Current**
  - **42-Bump WLP (3.0mm x 3.5mm) and 40-Pin TQFN (5mm x 5mm) Packages**
  - **Integrated Temperature Sensor**
- **Low Power Requirements**
  - **< 80mW for Black Video Images**
  - **Output Disable Using Video Marker**
  - **Output Voltage Sensor**
- **Laser Enable Function Supports Safety Compliance**

Simplified Functional Diagram



For related parts and recommended products to use with this part, refer to: www.maximintegrated.com/MAX3601.related

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6444; Rev 3; 3/15

MAX3601

Laser Driver for Projectors

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AVDD to DVDD.....-0.3V to +0.3V
AVCC to DVCC.....-0.3V to +0.3V
AGND to DGND .....-0.3V to +0.3V
OUT_ to DGND.....-0.3V to +8.4V
OUT_ Current
  Continuous.....400mA
  Peak (t < 1µs).....800mA
D0–D11, DCLK, TESTC to DGND..... -0.3V to lower of +2.2V or (V_{DVDD} + 0.3V)
CLK/SCL, DIO/SDA, CS, EN_MAIN, MARKER, TESTA, TESTB to DGND .....-0.3V to lower of +4.0V or (V_{DVCC} + 0.3V)
D0–D11, DCLK, SCL, SDA, CS, EN_MAIN, MARKER Current ..... -50mA to +50mA
Continuous Power Dissipation
  TQFN (T_A = +85°C, derate 35.7mW/°C above +85°C)..2320mW
  WLP (T_A = +70°C, derate 28.5mW/°C above +70°C)..2200mW
Junction Temperature .....+150°C
Operating Temperature Range
  TQFN ..... -40°C to +105°C
  WLP ..... 0°C to +70°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (soldering, 10s; TQFN only).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
  Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W
  Junction-to-Ambient Thermal Resistance (θ_{JA}) .....28°C/W
WLP
  Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING CONDITIONS						
Output Voltage	V_{OUT}	Output enabled	0.5	0.6	7.5	V
POWER SUPPLY (Note 3, Figure 4)						
+1.8V Supply Current	I_{AVDD_DIS}	EN_MAIN low or SP_EN = 1		0.01	(1)	µA
	I_{AVDD}	SP_EN High		5	7	mA
	I_{DVDD1}	SP_EN = 0		0.02	(0.03)	mA/MHz
		SP_EN = 1, f_{PO} = 75MHz		0.1	(0.2)	
	I_{DVDD_G1A}	Video dependency DAC A		1.1	(1.5)	µA/(MHz x ΔCODE
	I_{DVDD_G1B}	Video dependency DAC B		0.5	(0.6)	
	I_{DVDD}	Maximum digital supply current f_{PIXEL} = 150MHz, f_{PO} = 75MHz			(45)	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
+3.3V Supply Current	I_{AVCC}	Core analog			1.5	1.8	mA
	I_{DVCC_DIS}	ENA_ = ENB_ = 0			0.01	0.1	
	I_{DVCC_G1A}	GA_ = 0x00 (per channel)			3.4	4.8	
	I_{DVCC_G2A}	GA_ = 0xFF (per channel)			8.2	9.1	
	I_{DVCC_G1B}	GB_ = 0x00 (per channel)			1.2	1.6	
	I_{DVCC_G2B}	GB_ = 0xFF (per channel)	MAX3601C		2.5	2.8	
			MAX3601G		2.5	3.3	
	I_{AVCC}	Maximum analog supply current GA_= GB_ = 0xFF, ENA_ = ENB_ = 1	MAX3601C			(37.6)	
			MAX3601G			(39.1)	
Pulse-Off Assist Current (Note 4)	I_{CCD_G1}	PHS_= 0			5	(10)	µA/MHz
	I_{CCD_G2}	f_{PO} = f_{POH} = 75MHz, f_{PIXEL}= 150MHz, C_L = 0pF, V_{OUT_MIN} = 0.8V to 1.8V			2.3	(4.6)	
Power In MAX3601 Driver (Note 5)		Outputs off, clock stopped			0.2		mW
		0% video			< 83	(100)	
		27% video			130		
		100% video			270		
		27% video with pulse-off			150		
		27% video with pulse-off assist			160		
Typical Output Sensitivity to Supply Voltage (Note 6)		I_{OUT}/V_{AVDD}			1		%/V
		I_{OUT}/V_{DVDD}			1	(3)	
		I_{OUT}/V_{AVCC}			2	(17)	
		I_{OUT}/V_{DVCC}			2.2	(6)	
VIDEO DAC (8-Bit, Note 7)							
Maximum Conversion Rate				150	160	(250)	Msps
Settling Time	t_S	Within 12 LSBs (GAIN = 0x0F to 0xFF)			6.7	(12)	ns
		Within 3 LSBs (GAIN = 0xFF)			12	(25)	
		Within 1 LSB (GAIN = 0xFF)			23	(34)	
Rise/Fall Time		20% to 80%			1.5	(2.5)	ns
Offset Error (GSA_ = GSB+ = 0xFF, ENA_ = ENB_ = 1)	OS_ER	0V ≤ V_{OUT} ≤ V_{AVCC} + 0.5V			1.0	24	µA
		V_{OUT} = 7.5V		(1.0)	10.5	37	
Resistor ROUT1	R_{OUT1}	V_{OUT} = 7.5V, see Figure 12		(290)	400	(490)	kΩ
Video INL (Notes 8 and 9)		Code > 0x1F		(-15)		(15)	LSB
INL Drift (Notes 8 and 9)		0x1F < GAIN < 0xFF, 0°C < T_J < +125°C V_{OUT_MIN} = 0.6V to 1.6V			1.5	(3)	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Video DNL (GAIN = 0x0F to 0xFF) (Note 8)		Guaranteed monotonic		(-1)		(+1)	LSB
Propagation Delay (Delay = PD1 + PD2)		PD1			2		Pixel clocks
		PD2			11		ns
Propagation Delay Variation				(-1)		(+1)	ns
Transfer of V_{OUT} to I_{OUT} (Note 5)		f < 50kHz, V_{OUT} > 0.9V			0.2	(1)	%/V
		f < 1MHz, V_{OUT} > 0.6V			6	(10)	
		f < 1MHz, V_{OUT} > 0.5V			12	(15)	
Output Capacitance (CODE_A = CODE_B = 0x00)	C_{DVR}	V_{OUT} = 0.6V			260		pF
		V_{OUT} = 1.1V			125		
		V_{OUT} = 2.0V			100		
PULSE OFF ASSIST							
Rise Time		20% to 80%, $V_{A\_}$ = 1.0V, C_L = 0pF, PHS_ = 3, VIDEO = 0x00			1.6	(3)	ns
Incremental Resistance PH_= 0xFFFF		PHS_= 3,			8		Ω
		PHS_= 2			16		
		PHS_= 1			32		
		PHS_= 0			64		
Compliance Voltage	V_{O_POH}	Relative to V_{AVCC}, I_{OUT} = 1mA (T_A = 0 to +125°C)				(-0.8)	V
		T_A = -40°C to +125°C				(-0.9)	
OUTPUT GAIN (VIDEO_ = 0xFF)							
Resolution					8		Bits
Current at OUT		GA_= 0x00, GB_= 0x00			0.01	(1)	mA
		GA_= 0xFF, GB_= 0x00	MAX3601C	280	320	400	
			MAX3601G, T_A = +25°C to +105°C	275	320	400	
			MAX3601G, T_A < +25°C	260	320	400	
		GA_= 0x00, GB_= 0xFF	MAX3601C	69	80	100	
			MAX3601G, T_A = +25°C to +105°C	68	80	100	
			MAX3601G, T_A < +25°C	60	80	100	
		GA_= 0xFF, GB_= 0xFF	MAX3601C	(349)	400	(500)	
			MAX3601G	(320)	400	(500)	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPLIANCE ALARM							
VSET DAC Resolution		4 bit		(70)	80	(90)	mV
VSET DAC Range		VSET_ = 0x0		0.32	0.4	0.48	V
		VSET_ = 0xF		1.4	1.6	1.8	
Filter 1 Time Constant					1		ns
Filter 2 Time Constant					2.7		ns
TEMPERATURE ALARM							
Temperature Range				(5)		(150)	°C
Temperature Accuracy		T_J = +20°C to +125°C		(-10)		(10)	°C
Temperature Resolution		T_J = +20°C to +125°C		(2.25)	2.5	(2.75)	°C/LSB
LOGIC I/O (DIO/SDA, CLK/SCL, CS, MARKER, EN_MAIN)							
Input Low Voltage	V_{IL2}	Test condition				0.4	V
Input High Voltage	V_{IH2}	Test condition		1.45			V
Input High Threshold		Relative to V_{DVDD}		(50)	60	(70)	%
Input Low Threshold		Relative to V_{DVDD}		(40	50	(60)	%
Input Hysteresis		Relative to V_{DVDD}		(5)			%
Input Current		DIO/SDA, CLK/SCL		-10	±0.2	+10	µA
Input Resistance	R_{EN_MAIN}	EN_MAIN to DGND		50	100	200	kΩ
	R_{MARKER}	MARKER to DVDD		50	100	200	
	R_{CS}	CS to DGND		50	100	200	
Input Capacitance					1		pF
Disable Time	t_{DIS}	EN_MAIN or MARKER to I_{OUT} falling			0.1	1	µs
Enable Settling Time Constant	t_{EN}	EN_MAIN rising or MARKER rising			0.5	1.5	µs
DIO/SDA Low Voltage		$I_{DIO/SDA}$ = 16mA			0.1	0.4	V
VIDEO DATA INPUTS							
Maximum Frequency	f_{DCLK_MAX}			150	> 160		MHz
DCLK Duty Cycle		f_{DCLK} > 100MHz		(45)		(55)	%
DCLK High Time		Relative to 2/f_{DCLK}		(-0.5)		(+0.5)	ns
Video Input Setup Time	t_{SU}	Operating condition		1			ns
Video Input Hold Time	t_H	Operating condition	MAX3601C	0.25			ns
			MAX3601G	0.35			
Input Switching Time		10% to 90%, operating condition			1.2		ns
Input Low Voltage	V_{IN-L}					0.5 x V_{DVDD} - 0.1	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IN-H}		0.5 x V_{DVDD} + 0.1			V
Input Threshold		Relative to V_{DVDD}		50		%
Input Hysteresis				0.1		V
Input Current			-10	<±1	+10	µA
Data Input Capacitance	C_D			1		pF
SUBPIXEL GENERATOR						
Pixel Clock Frequency Range		Subpixel generator active	24	150	(250)	MHz
Minimum Pulse Width		1 subpixel			(2)	ns
Subpixel Timing Accuracy		T_{PODM} - T_{POD}	(-1)		(+1)	ns
PLL Bandwidth			(1200)	2000	(3100)	kHz
I²C TIMING						
Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between START and STOP	t_{BUF}		1.3			µs
HOLD Time for a START Condition	t_{HD_STA}		0.6			µs
Setup Time Repeated START Condition	t_{SU_STA}		0.6			µs
SCL Low Time	t_{LOW}		1.3			µs
SCL High Time	t_{HIGH}		0.6			µs
SDA Hold Time	t_{HD_DAT}		0.1		0.6	µs
SDA Setup Time	t_{SU_DAT}		0.1			µs
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
Pulse Width of Suppressed Spikes	t_{SP}			0.05		µs
SPI TIMING						
SPI Clock Cycle	t_{CLK}		83			ns
SCL High Pulse Width	t_{WH}		41.5			ns
SCL Low Pulse Width	t_{WL}		41.5			ns
SCL Rise/Fall Time	t_{RF}	At f_{CLK} = 12MHz		16		ns
SCL Setup Time	t_{CLKS}		8			ns
CS Setup/Hold Time	$t_{CS,}$		32			ns
CS Recovery Time	t_{CR}		50			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write Data Setup Time	t_{DS}		16			ns
Write Data Hold Time	t_{DH}		16			ns
Read Data Delay Time	t_{RD}				34	ns
DIO Output Switching Time	t_{ZR}	R_{DIO} = 390Ω, C_{DIO} = 20pF		11	(16)	ns
DIO Output Disable Time	t_{RZ}	MAX3601C			34	ns
		MAX3601G			36	
DIO Conflict Avoid Time	t_{ZZ}		0			ns
POWER-ON RESET (Figure 27)						
V_{AVDD},V_{DVDD} On Threshold	$2V_{POR+}$			1.32	(1.6)	V
V_{AVDD},V_{DVDD} Off Threshold	$2V_{POR-}$		(1)	1.28		V
V_{DVCC},V_{DVCC} On Threshold	$3V_{POR+}$			2.5	(2.8)	V
V_{AVCC},V_{DVCC} Off Threshold	$3V_{POR-}$		(2.2)	2.4		V

Note 2: Parameters measured using circuit of Figure 1. R_S, C_S, C_L = open, unless otherwise noted. Parameters in parentheses ( ) are provided for guidance, but are not tested or guaranteed.

Note 3: Power Consumption Calculations:

$$I_{DVDD}(mA) = I_{DVDD}(mA/MHz) \times f_{PIXEL}(MHz) + \sum_{N=1}^{3}\left[ENA_N \times I_{DVDD_{G1A}}(mA/MHz) \times \Delta CODE_{A_N} + ENB_N \times I_{DVDD_{G1B}}(mA/MHz) \times \Delta CODE_{B_N}\right] + f_{PIXEL}(MHz)$$

$$I_{DVCC}(mA) = \sum_{N=1}^{3}\left[ENA_N \times I_{DVCCD_{G1A}} + \left(I_{DVCC_{G2A}} - I_{DVCC_{G1A}}\right) \times \frac{GA_N}{255} + ENB_N \times I_{DVCC_{G1B}} + \left(I_{DVCC_{G2B}} - I_{DVCC_{G1B}}\right) \times \frac{GB_N}{255}\right]$$

where:
N = OUTPUT 1,2,3, f_{PIXEL} is the pixel clock frequency (MHz), ENA_ and ENB_ are the DAC enable signals with value 0 or 1, ΔCODE is the average number of video code changes per pixel (0 to 255). If the Pulse-Off feature is used 1 time per pixel, ΔCODE = 2x Average Video Code Value. If Pulse-Off is used 2 times per pixel, ΔCODE = 4x Average Video Code Value (Figure 3).

Note 4: Pulse-Off Assist Current Calculation:

$$I_{DVCCD} \approx \sum_{N=1}^{3}\left[\left(I_{DVCC_{G1}} + C_{OUTN} \times \Delta V_{OUTN}\right) \times f_{PON}\right]$$

where:
N = Output 1,2,3, C_{OUTN} is the total capacitance at OUTN (MAX3601 output capacitance + external capacitance), ΔV_{OUTN} is the resulting voltage change at OUTN, f_{PON} is the frequency of pulse-events in MHz. f_{PON} is generally equal to the pixel clock, but could be lower or higher, depending on the pulse-off duty cycle and number of pulse-off events per pixel.

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{AVCC} = V_{DVCC} = 2.9V to 3.5V, T_A = T_{MIN} to T_{MAX}, T_J < +125°C, EN_MAIN and MARKER high, V_{OUT} ≥ 0.7V, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, T_J = +85°C. Consumer grade parts are tested at T_A = +70°C. Automotive grade parts are tested at T_A = +105°C. Minimum and maximum specifications are guaranteed by design, characterization and/or production test.)(Note 2)

Note 5: Power Estimation Conditions:
For each output, DAC A is enabled, DAC B is off, VIDEO = 27% data as shown in Figure 2, f_{PIXEL} = 150MHz. Vertical Image Duty cycle is 70%, and the MARKER signal is used to reduce power during vertical flyback.
The load emulates:
Red Laser on OUT1: 4I + 2.3V
Green Laser on OUT2: 8I + 3.8V
Blue Laser on OUT3: 16I + 3.5V

	PARAMETER	VIDEO	GAIN1 (mA)	GAIN2 (mA)	GAIN3 (mA)	V_{OUT} @I_{PEAK}	VA1 (V)	VA2 (V)	VA3 (V)	PO_EN	POC	POM_	PHM_
1	0% Video	00h	200	180	70	0.6V	3.7	5.9	5.2	0	0	0	0
2	27% Video	27%	200	180	70	0.6V	3.7	5.9	5.2	0	0	0	0
3	100% Video	FFh	200	180	70	0.6V	3.7	5.9	5.2	0	0	0	0
4	Pulse-Off	27%	300	270	105	0.8V	4.3	6.8	6.0	1	4h	FF00h	0
5	With Pulse-off Assist	27%	300	270	105	0.8V	4.3	6.8	6.0	1	4h	FF00h	FF00h

Note 6: Transfer from supply to I_{OUT} measured with 100mV_{P-P} sine wave applied at the supply.

$$T = \frac{f'I_{OUT}}{I_{OUT}} \times \frac{100\%}{f'V}$$

with units %/V. I_{OUT} = 325mA, T_J ≤ +110°C, f_{OUT} = 60Hz to 1MHz. Typical values are at 10kHz, maximum value at 1MHz typical corner.

Note 7: AC Parameters characterized with a video pattern of 0x00 to 0xFF, GAIN = 0xFF, 0x3F, 0x1F, 0x0F. All combinations of output VIDEO DACs: DAC A only, DAC B only, DAC A and DAC B. An external filter network (R_S, C_S) or digital filter may be used to reduce ringing.

Note 8: $$1lsb = \frac{I_{OUT(CODE=0xFF)} - I_{OUT(CODE=0x00)}}{255}$$

Note 9: Integral nonlinearity (INL) is measured as: [I_{OUT} - Least Squares approximation of current].

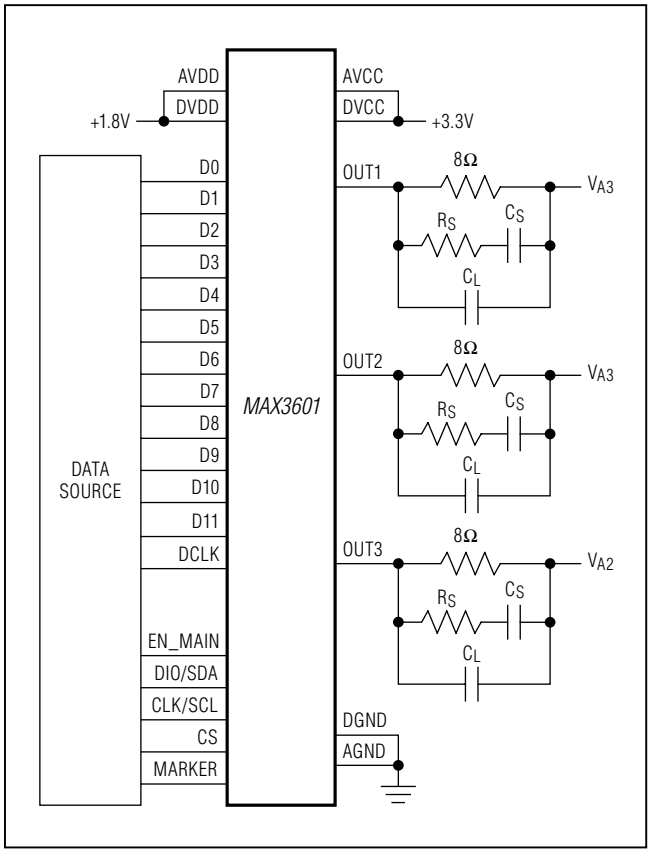


Figure 1. Test Circuit

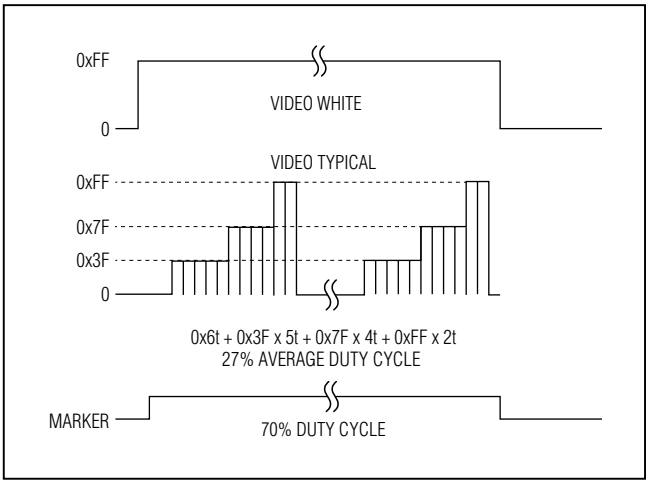


Figure 2. Video Test Pattern

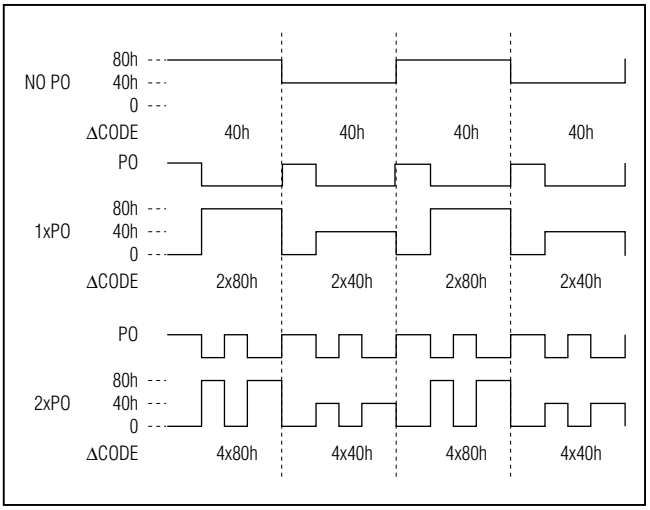


Figure 3. ΔCode Example

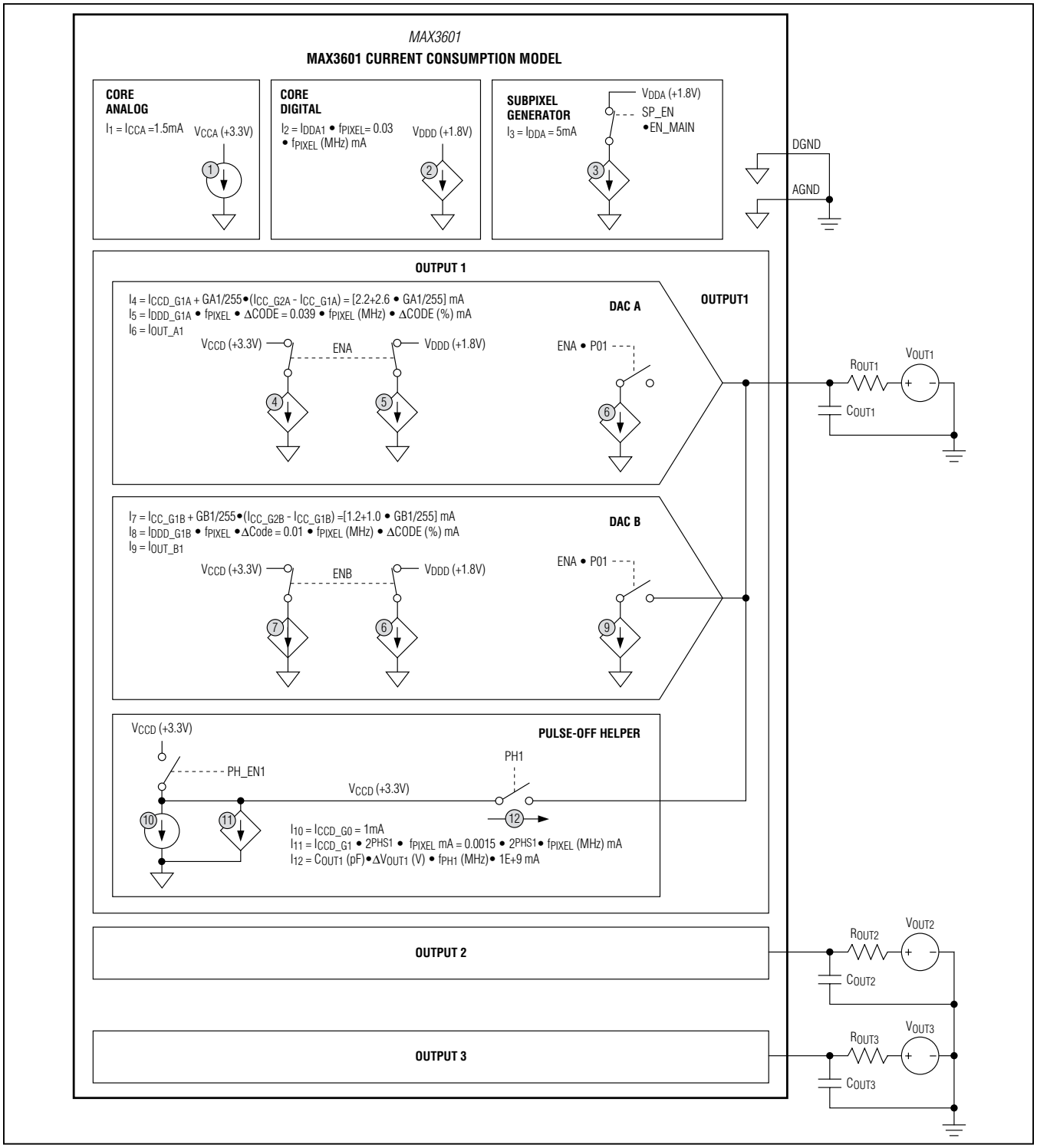
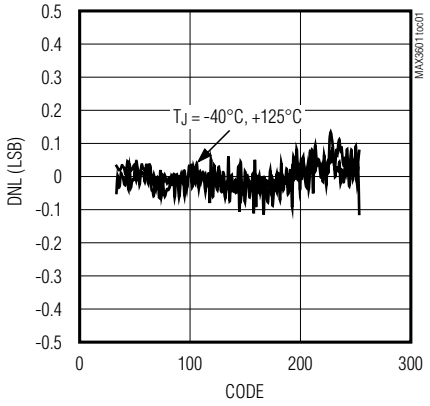


Figure 4. Power-Supply Calculations

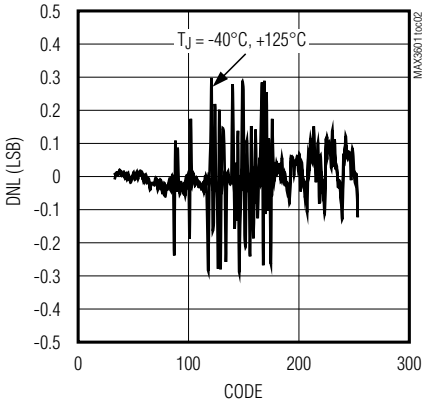
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, V_{OUT} = 0.7V, R_L = 8Ω, EN_MAIN high, T_A =+25°C, unless otherwise noted.)

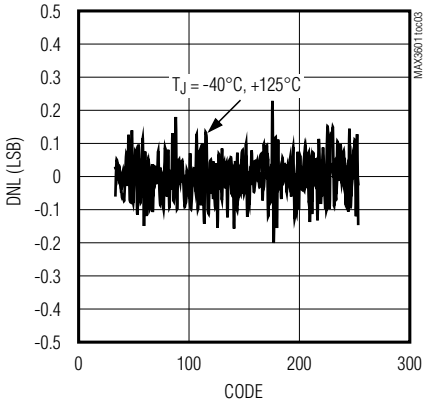
VIDEO DNL DAC A (GAIN = 0x20)



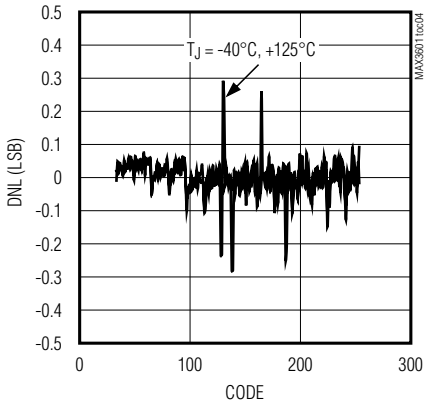
VIDEO DNL DAC A (GAIN = 0xFF)



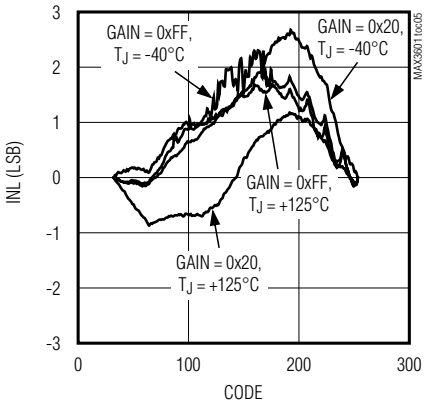
VIDEO DNL DAC B (GAIN = 0x20)



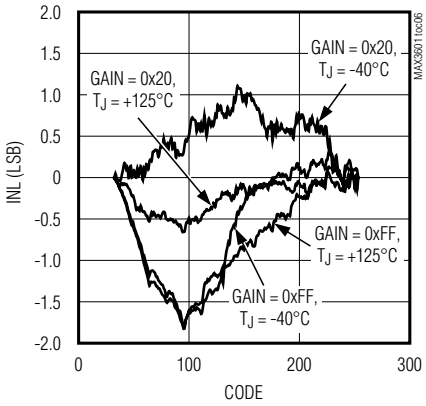
VIDEO DNL DAC B (GAIN = 0xFF)



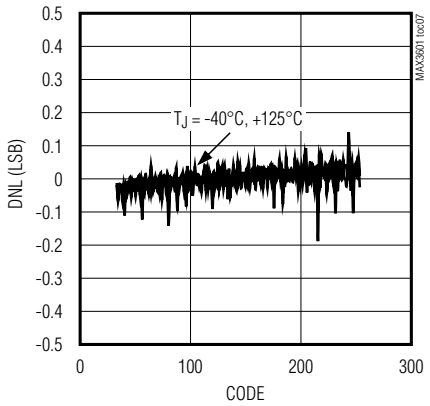
VIDEO INL DAC A



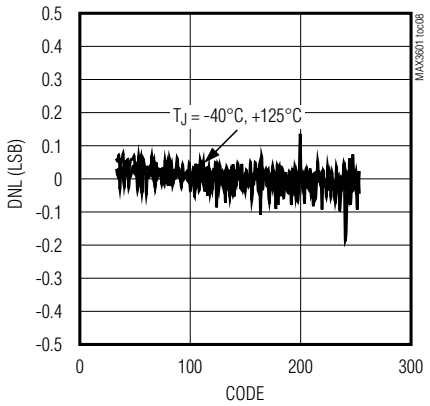
VIDEO INL DAC B



GAIN DNL DAC A (OFFSET = 0xFF)



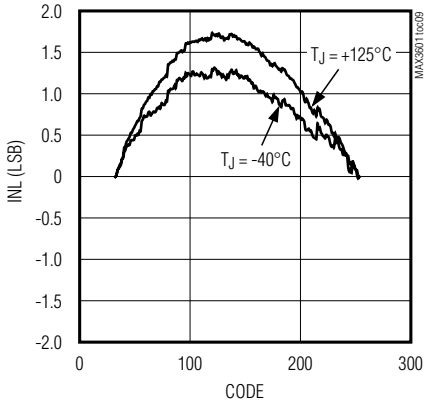
GAIN DNL DAC B (OFFSET = 0xFF)



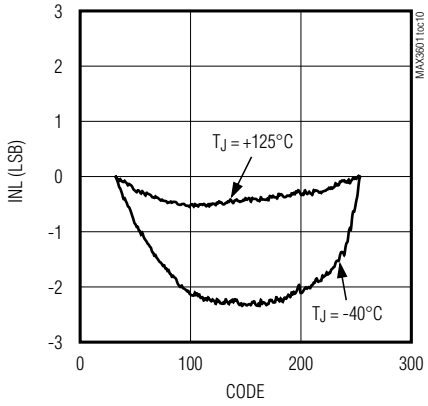
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, V_{OUT} = 0.7V, R_L = 8Ω, EN_MAIN high, T_A =+25°C, unless otherwise noted.)

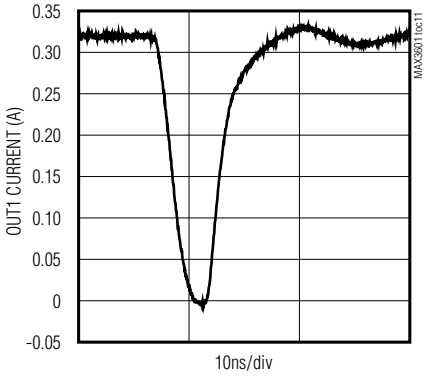
GAIN INL DAC A (OFFSET = 0xFF)



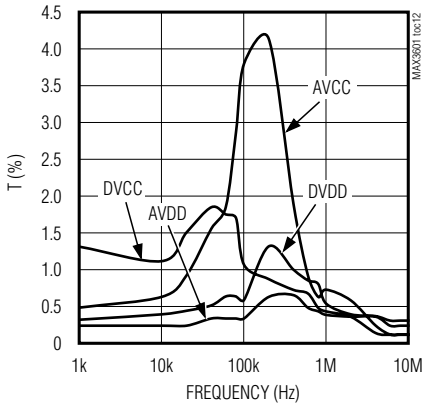
GAIN INL DAC B (OFFSET = 0xFF)



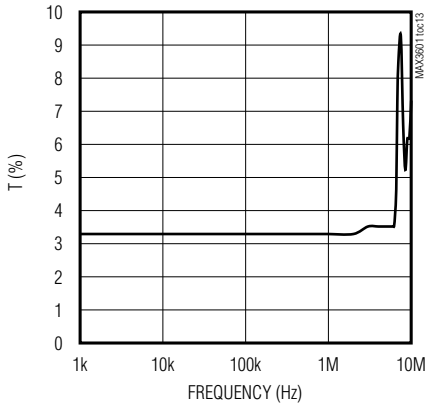
OUT1 PULSE OFF



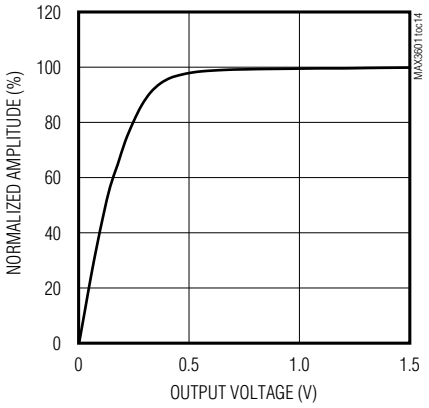
POWER-SUPPLY TRANSFER TO I_{OUT} (GAIN = OFFSET = 0xFF)



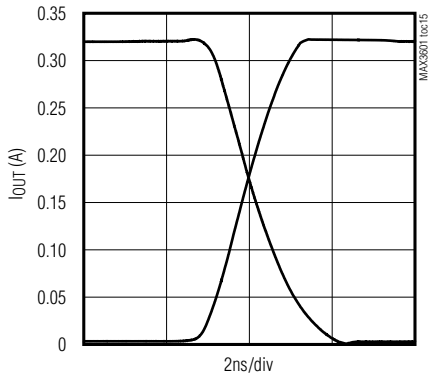
V_A TRANSFER TO I_{OUT} (GAIN = OFFSET = 0xFF)



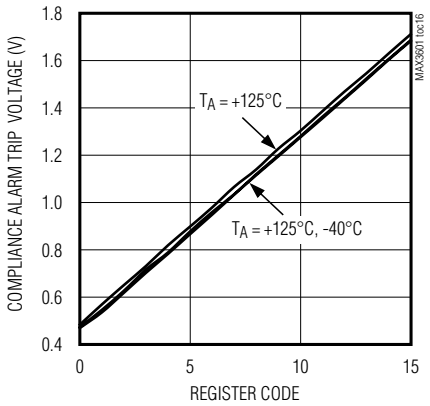
NORMALIZED OUTPUT CURRENT vs. OUTPUT VOLTAGE



I_{OUT} RISE AND FALL TRANSIENT



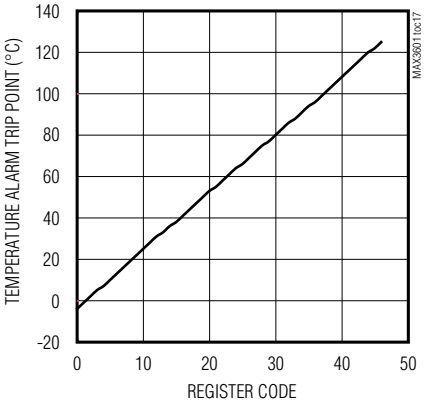
OUT_ COMPLIANCE ALARM TRIP VOLTAGE vs. REGISTER CODE



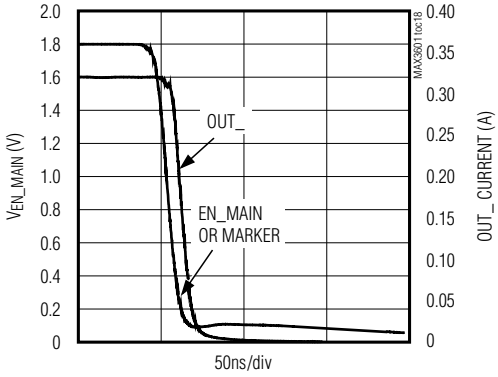
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.8V, V_{AVCC} = V_{DVCC} = 3.3V, V_{OUT} = 0.7V, R_L = 8Ω, EN_MAIN high, T_A =+25°C, unless otherwise noted.)

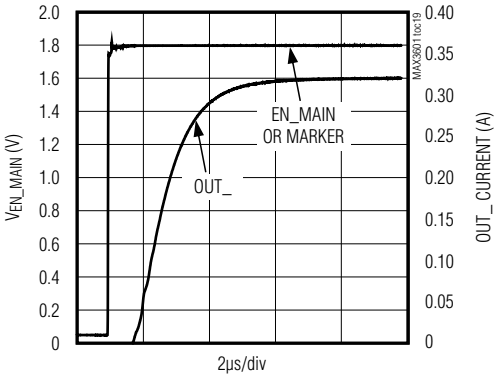
TEMPERATURE ALARM TRIP POINT vs. REGISTER CODE



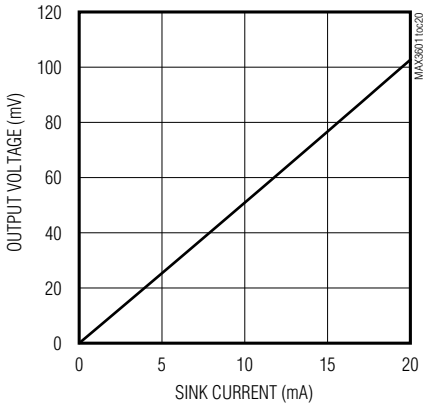
OUT_ DISABLE TIME



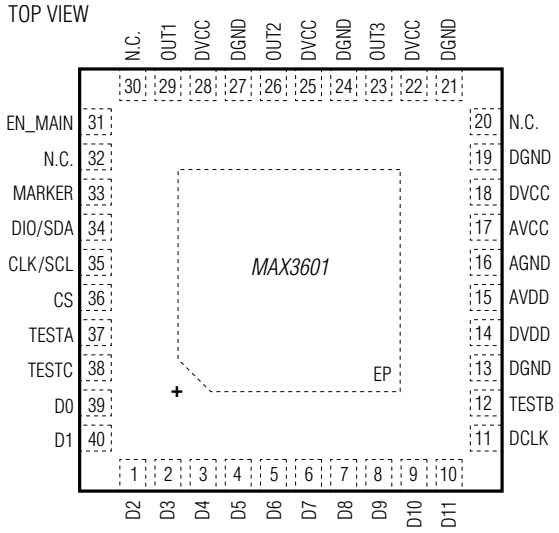
OUT_ ENABLE TIME



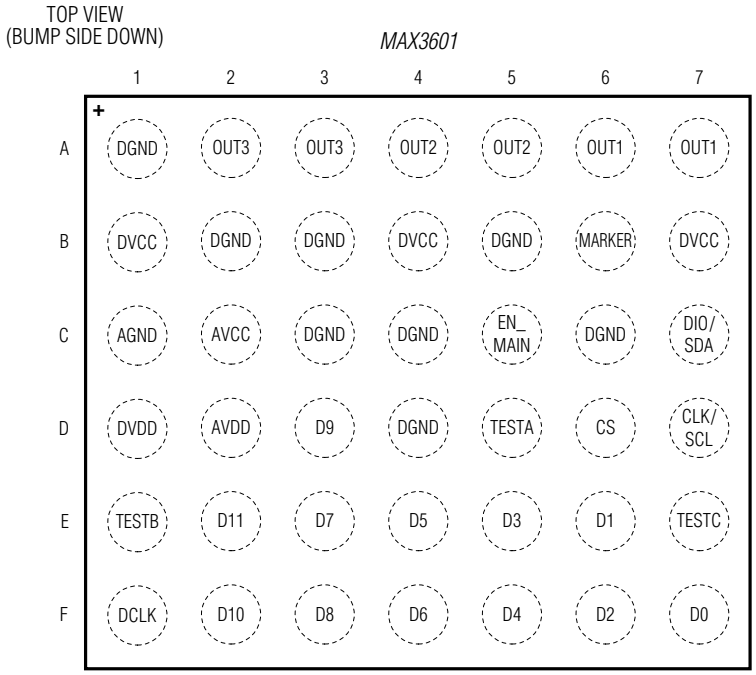
SDA LOW VOLTAGE vs. SDA SINK CURRENT



Pin/Bump Configurations

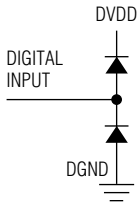


THIN QFN
(5mm x 5mm)

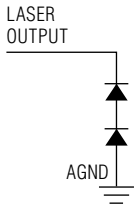
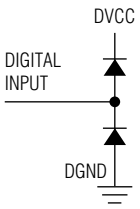
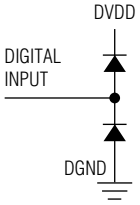


WLP
(3.5mm x 3.0mm)

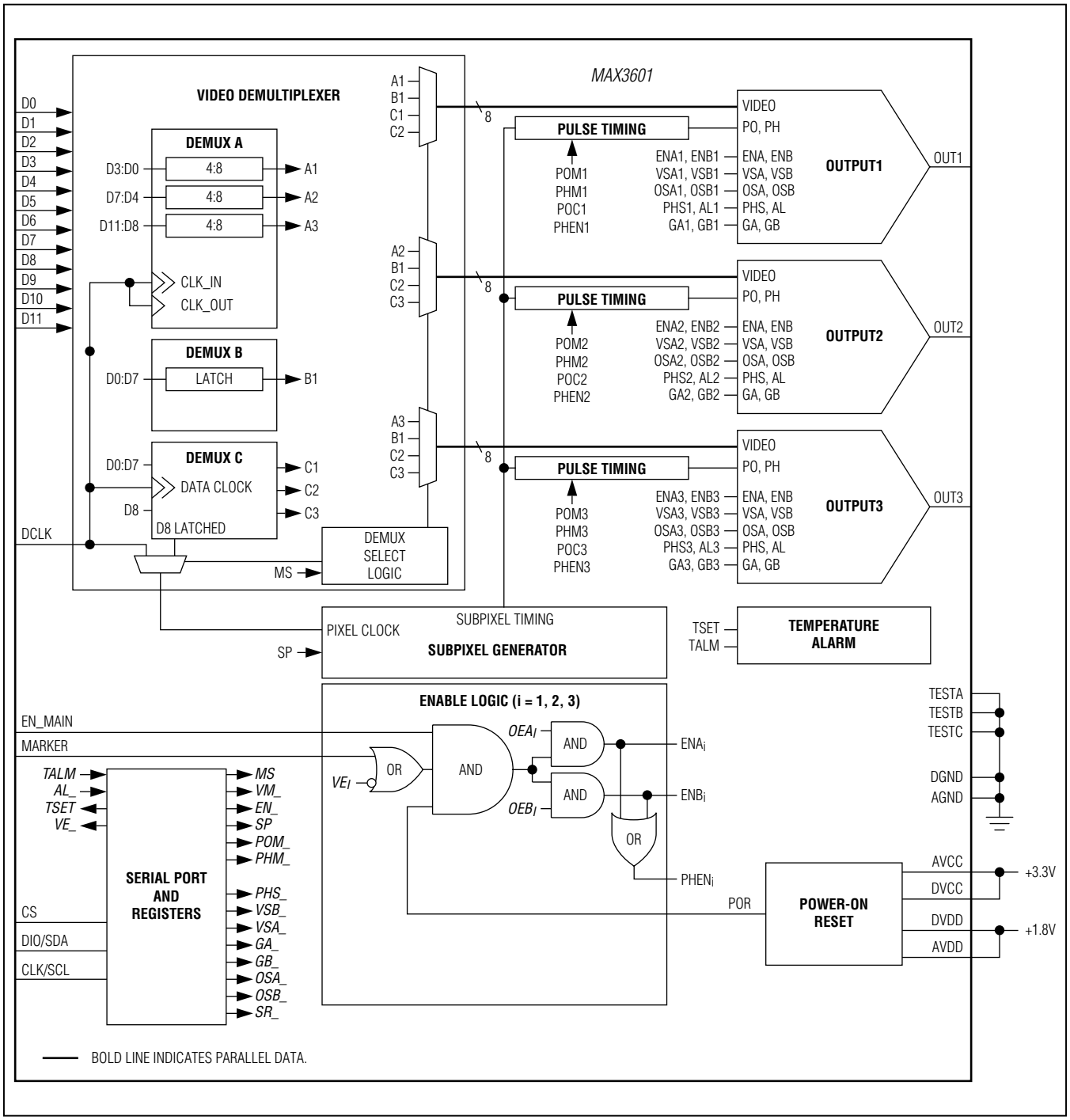
Pin/Bump Description

PIN		NAME	FUNCTION	EQUIVALENT INPUT SCHEMATIC
TQFN-EP	WLP			
1	F6	D2	Synchronous Video Data Inputs	
2	E5	D3		
3	F5	D4		
4	E4	D5		
5	F4	D6		
6	E3	D7		
7	F3	D8	Synchronous Video Data Input. In DEMUX C mode, D8 functions as the pixel clock.	
8	D3	D9	Synchronous Video Data Inputs	
9	F2	D10		
10	E2	D11	Synchronous Video Data Input, MSB	
11	F1	DCLK	Video Clock Input	
12, 37, 38	D5, E1, E7	TESTA, TESTB, TESTC	Test Pins. Connect to DGND.	—
13, 19, 21, 24, 27	A1, B2, B3, B5, C3, C4, C6, D4	DGND	Digital Ground. Connect to 0V.	—
14	D1	DVDD	1.8V Digital Power Supply. Bypass DVDD to DGND with 0.1µF and 0.01µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.	—
15	D2	AVDD	1.8V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.01µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.	—
16	C1	AGND	Analog Ground. Connect to 0V.	—
17	C2	AVCC	3.3V Analog Power Supply. Bypass AVCC to AGND with 0.1µF and 0.01µF capacitors as close as possible to the device with the smaller capacitor closest to AVCC.	—
18, 22, 25, 28	B1, B4, B7	DVCC	3.3V Digital Power Supply. Bypass DVCC to DGND with 0.1µF and 0.01µF capacitors (1 pair per pin) as close as possible to the device with the smaller value capacitor closest to DVCC.	—
20, 30, 32	—	N.C.	No Connection. There is no connection from the package to the IC.	—

Pin/Bump Description (continued)

PIN		NAME	FUNCTION	EQUIVALENT INPUT SCHEMATIC
TQFN-EP	WLP			
23	A2, A3	OUT3	Connection for Laser 3. Leave OUT3 unconnected if unused.	
26	A4, A5	OUT2	Connection for Laser 2. Leave OUT2 unconnected if unused.	
29	A6, A7	OUT1	Connection for Laser 1. Leave OUT1 unconnected if unused.	
31	C5	EN_MAIN	Laser Enable Input with 100kΩ Pulldown to DGND. Set EN_MAIN = high to enable OUT1–OUT3.	
33	B6	MARKER	Video Marker Input with 100kΩ Pullup to DVDD	
34	C7	DIO/SDA	SPI and I²C Serial Data Input/Output	
35	D7	CLK/SCL	SPI and I²C Serial Clock Input	
36	D6	CS	SPI Chip Select with 100kΩ Pulldown to DGND. Connect CS to DVDD for I²C mode. Set CS = low on power-up for SPI mode.	
39	F7	D0	Synchronous Video Data Input, LSB	
40	E6	D1	Synchronous Video Data Input	
—	—	EP	Exposed Pad (TQFN Only). EP is internally connected to DGND. The EP **must** be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.	—

Functional Diagram



Detailed Description

The laser driver for projectors supports video imaging with red, blue, and green lasers. Each output includes two 8-bit video/offset DACs with programmable gain and offset.

Video Demultiplexer

The Video Demultiplexer supports three video formats and pixel clock configurations. The video format and demultiplexer are selected by the MUX select register (MS) as shown in Table 7.

Demux A

Demux A converts 4-bit input with DDR clock to 8-bit data with pixel clock. Input data must be formatted as shown in Figure 5. Four MSBs are latched on the rising edge of DCLK, and four LSBs are latched on the falling edge of DCLK.

Demux B

Demux B latches an 8-bit video input on the rising edge of clock. The same video is sent to all outputs.

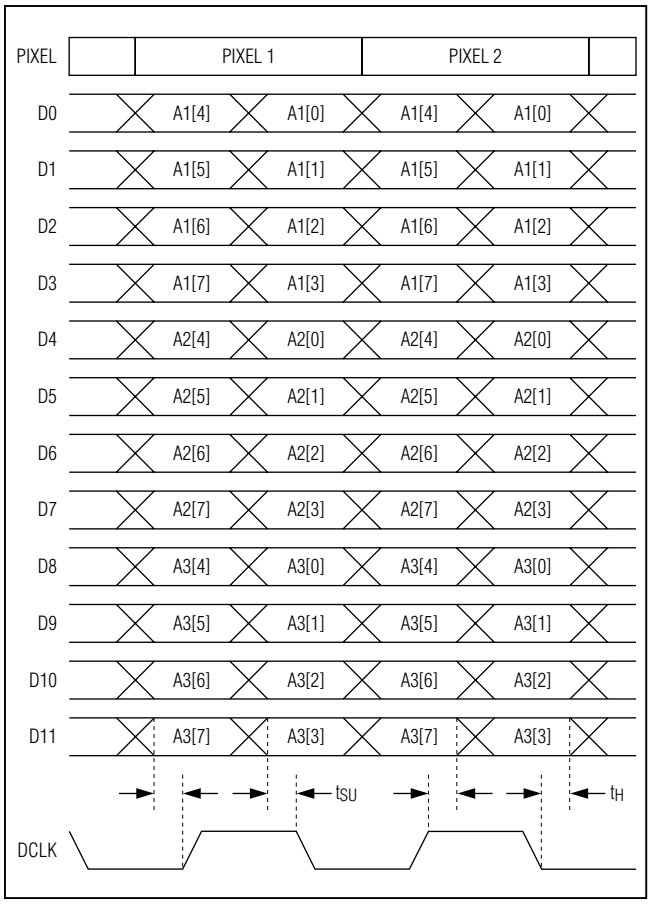


Figure 5. Video Demultiplexer A Input Waveform

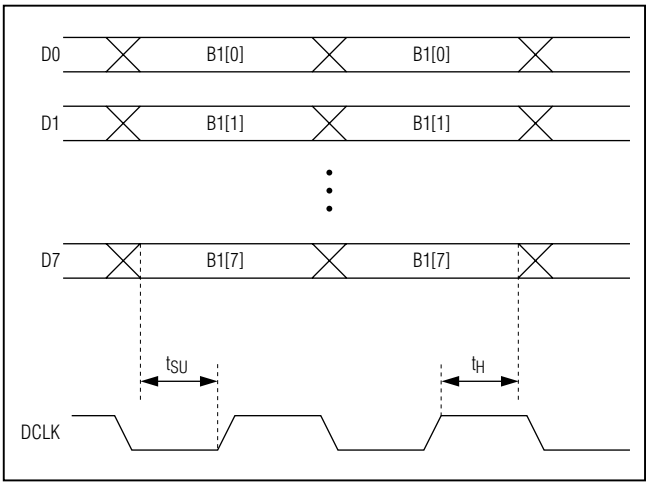


Figure 6. Video Demultiplexer B Input Waveform

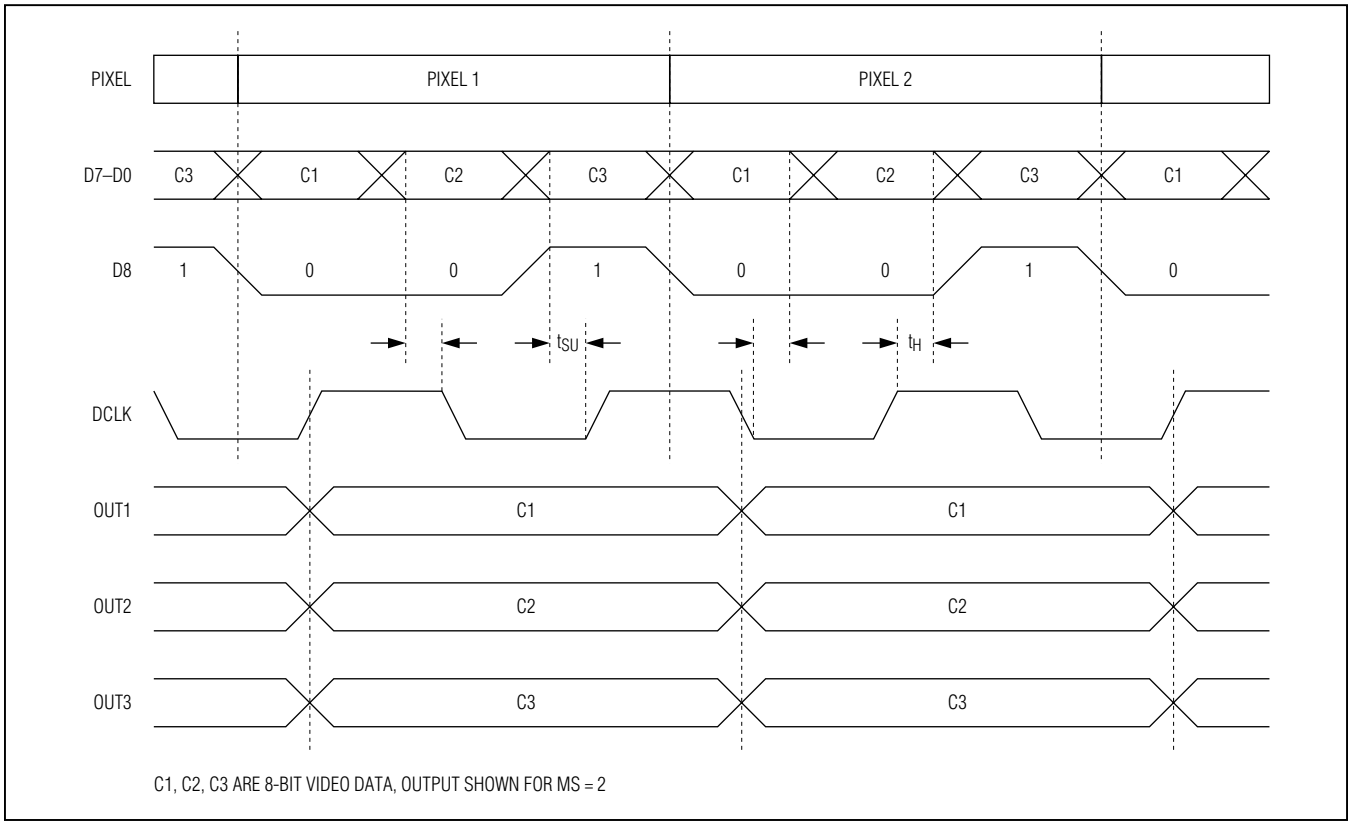


Figure 7. Video C Demultiplexer Input Waveform

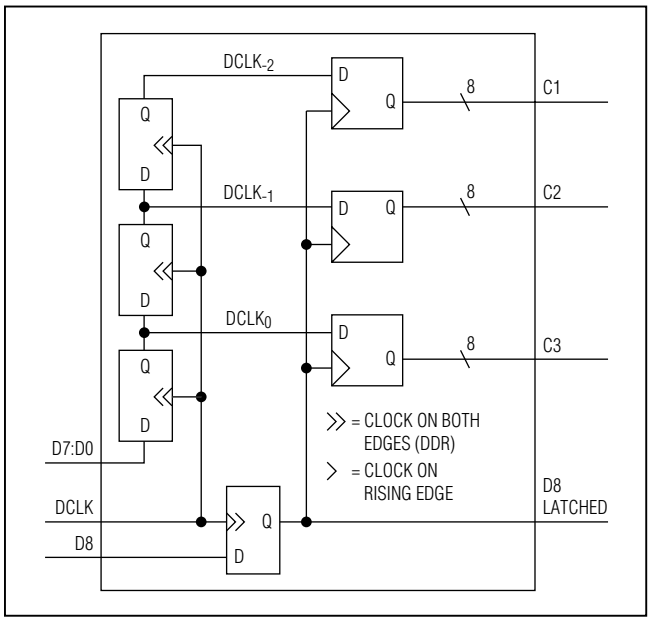


Figure 8. Video C Demultiplexer

Demux C

Demux C is compatible with the data format of the MAX3600. Data for the three outputs is multiplexed in time and uses a DDR clock.

Pulse Timing Generator

The Pulse Timing generator creates phases of the pixel clock called subpixels (Figure 9). The subpixel timing signals enable laser current output pulsing for use with despeckling the laser light. Each output of the laser driver can have different pulse widths or multiple pulses. If unused, disable the subpixel generator (D0 of register 0x0B) for additional power savings.

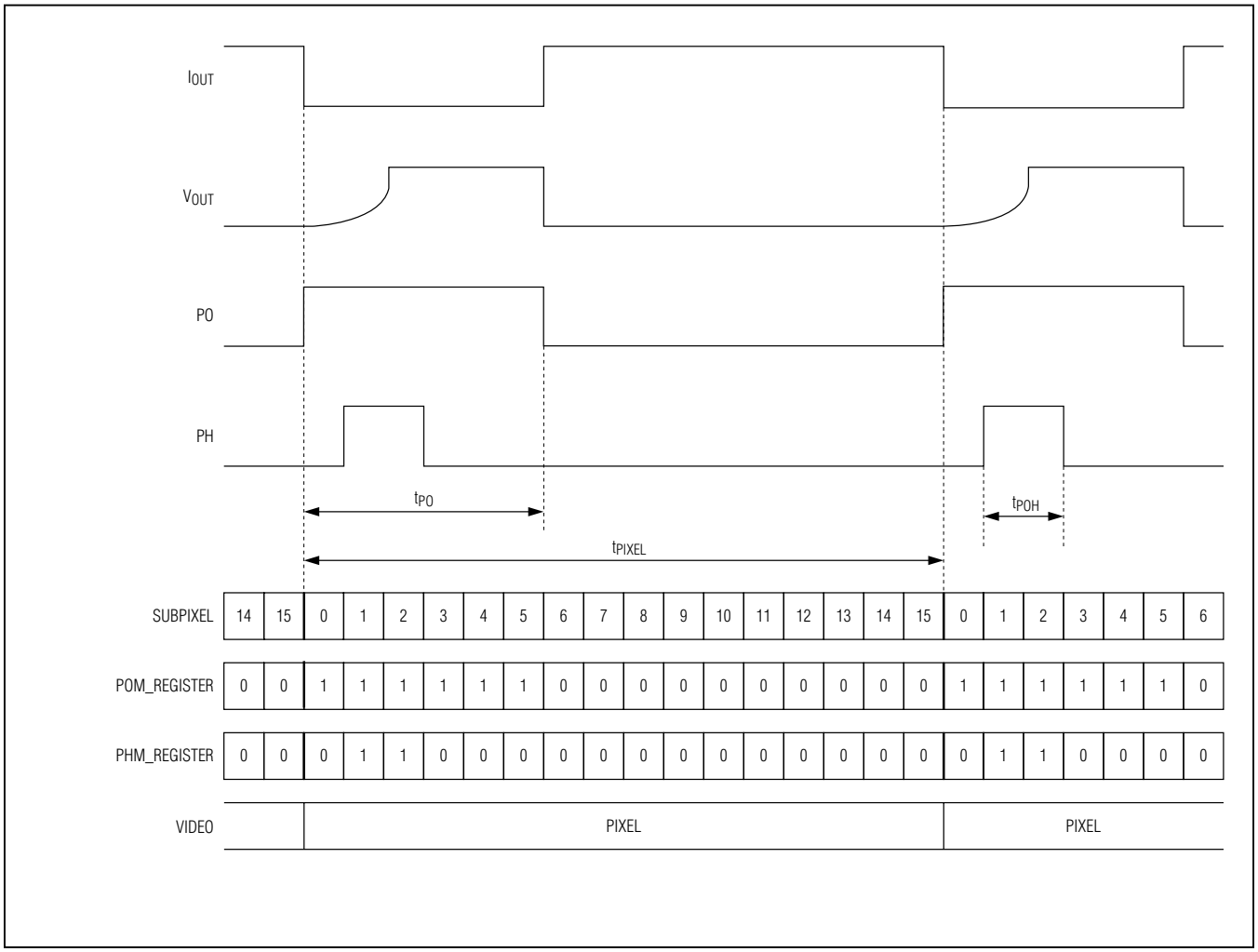


Figure 9. Pulse Timing Generator

Subpixel Programming

The subpixel programming bits (D[2:0] of register 0x0C) determine the number of subpixels and duration of the pulse time (Table 1). The pulse width is applied to every pixel when the programmed pulse-off length > 0. This can be dynamically implemented to adjust for various lighting conditions.

Pulse-Off

The pulse-timing generator can be configured to skip pulse events to save power. The Pulse-Off Configuration (POC) register selects options shown in Table 2. Random pulse-off events are triggered from a 31-bit pseudo-random bit-stream. By default, the PRBS is common to all outputs. Bit D4 of the POC_ registers determine which PRBS bits control each output (Table 3).

Pulse-off synchronization between outputs occurs when POC_ registers match and POC_[4] = 0. For example, if POC1 = POC2 = POC3 and POC_[4] = 0, the occurrence of randomized pulse-off events at all outputs will be synchronized.

Table 1. Subpixel Programming (SP Register)

SP	f_{PIXEL} (MHz)		ACTIVE SUBPIXELS	INACTIVE SUBPIXELS
	MIN	MAX		
000	150	200	0:7	8:15
001*	**75**	**150**	**0:15**	**—**
010	50	100	0:11	12;15
011	37.5	75	0:15	—
100	30	60	0:9	10:15
101	25	50	0:15	—
110	21.4	42.8	0:13	14:15
111	18.75	37.5	0:15	—

**Power-on default*

Table 2. Pulse-Off Duty Cycle (POC_ Register)

POC_[3:0]	PULSE-OFF DUTY CYCLE
0000*	**Every pixel, 100%**
0001	Random, 87.5%
0010	Random, 75.0%
0011	Random, 62.5%
0100	Random, 50.0%
0101	Random, 37.5%
0110	Random, 25.0%
0111	Random, 12.0%
1XXX	Every other pixel, 50%

**Power-on default*

Table 3. Random Pulse-Off Programming

POC_[4]	PRBS31 BITS USED		
	OUTPUT 1	OUTPUT 2	OUTPUT 3
0*	**PRBS31[4], [3], [0]**	**PRBS31[8], [7], [0]**	**PRBS31[16], [15], [0]**
1	PRBS31[2:0]	PRBS31[2:0]	PRBS31[2:0]

**Power-on default*

Driver Outputs

Each of the three laser driver outputs contains two video DACs, two gain DACs, a Compliance Voltage alarm, and Pulse-Off Assist. For power savings, the MAX3601 reduces supply current when outputs are not in use.

Video DACs

Each laser driver output contains two video DACs that produce current representing the video image (Figure 10). DACA has 4x the current output capability of DACB but is otherwise identical. Video Data is input from the high-speed data inputs. VSA_ and VSB_ determine the output behavior of the two video DACs (Table 4 and Table 5) The output video of either DAC can be any of the following:

- Video data
- Pulse-off with zero amplitude

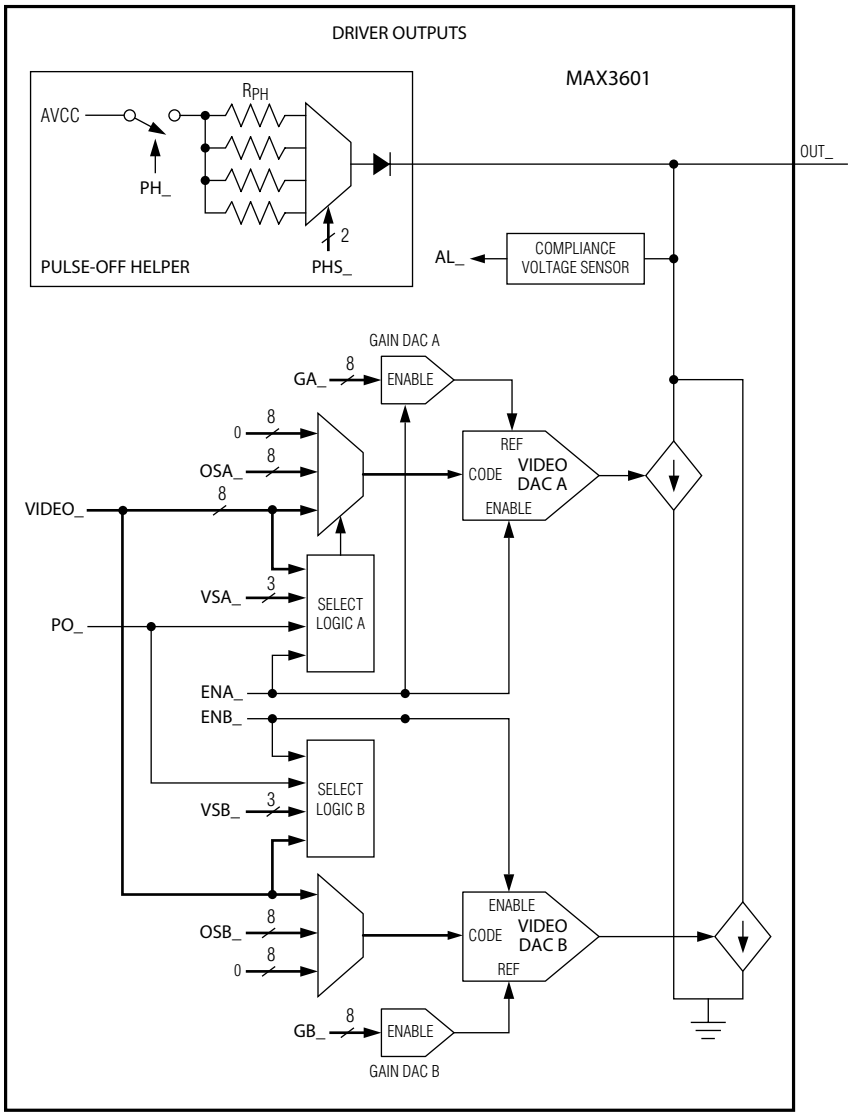


Figure 10. Driver Output

Table 4. Video Select Logic for DAC A

ENA_	VSA_	VIDEO	PO	CODE DAC A
0	X	X	X	0
1	000*	X	0	VIDEO
			1	0
	001	X	0	VIDEO
			1	OSA_
	010	X	0	OSA_
			1	0
	011	X	0	OSA_
			1	OSA_
	100	0	X	0
		> 0	0	OSA_
			1	0
	101	X	X	0
	110	X	X	0
	111	X	X	0

**Power-on default*

Table 5. Video Select Logic for DAC B

ENB_	VSB_	VIDEO	PO	CODE DAC B
0	X	X	X	0
1	000*	X	0	VIDEO
			1	0
	001	X	0	VIDEO
			1	OSB_
	010	X	0	OSB_
			1	0
	011	X	0	OSB_
			1	OSB_
	100	0	X	0
		> 0	0	OSB_
			1	0
	101	X	X	0
	110	X	X	0
	111	X	X	0

**Power-on default*

- Pulse-off with non-zero amplitude
- Constant value set from serial port
- Zero amplitude
- Constant for VIDEO > 0, zero when VIDEO = 0

The two gain DACs adjust the full-scale output current for laser slope efficiency and color balance. Video Gain is programmed from the serial port. Full-scale output for Video DACs A and B are adjustable up to a peak output of 320mA and 80mA, respectively (Figure 11). The laser driver output current is the combined output of DAC A and B:

$$I_{OUT}(mA) = \frac{CODEA}{FFh}\left[\frac{GA}{FFh}\right] \times 320 + \frac{CODEB}{FFh}\left[\frac{GB}{FFh}\right] \times 80 + OSERR$$

where OSERR is the offset error.

Carefully consider the absolute maximum ratings of output current. If I_{OUT} is 400mA peak with 50% duty cycle over the life of the product, the average DC current is 200mA.

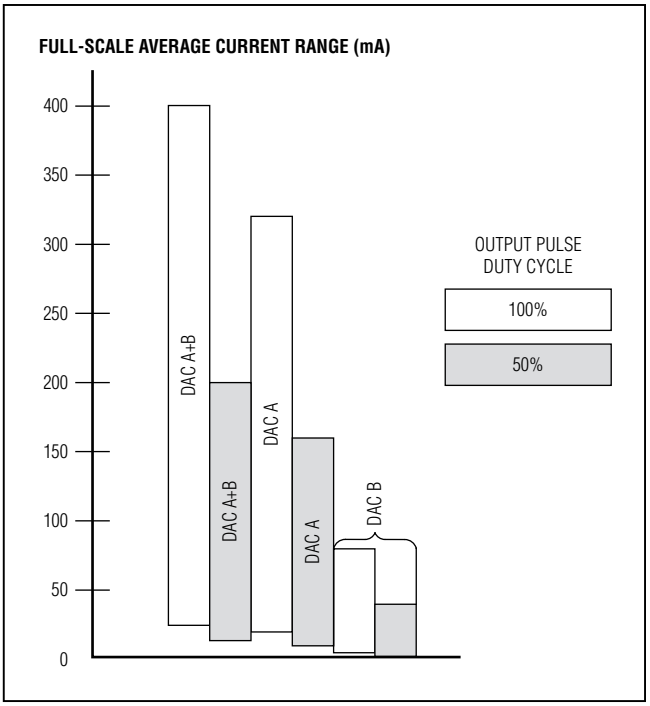


Figure 11. Driver Output Full-Scale Current Range

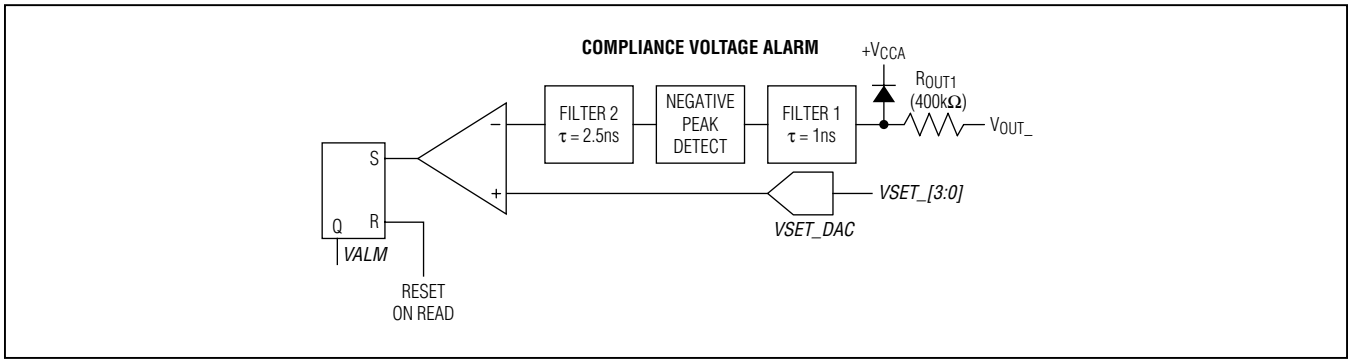


Figure 12. Output Compliance Sensor

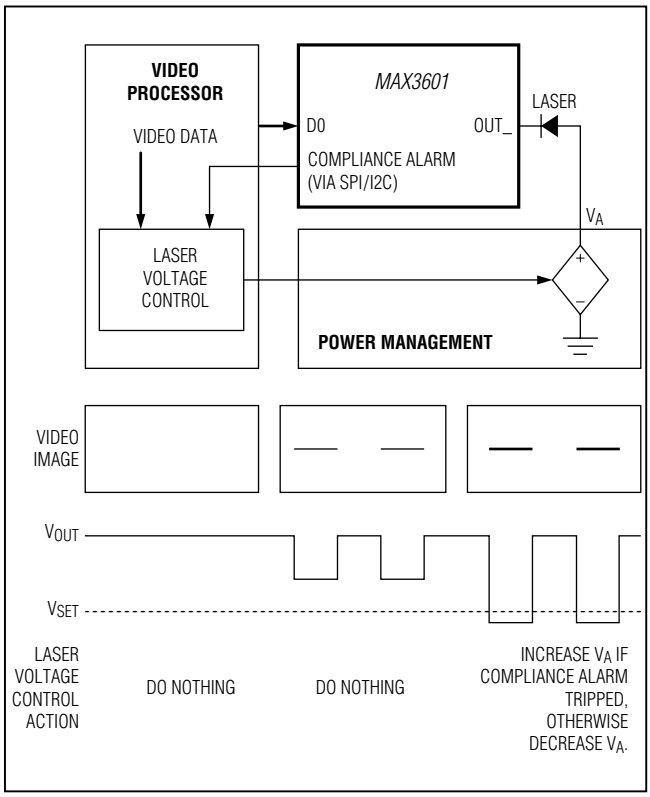


Figure 13. Example Use of Compliance Sensor

Pulse-Off and Pulse-off Assist

The Pulse feature rapidly pulses the laser off. The “off” level is set by the VSA_ and VSB_ registers (Table 4, Table 5).

Setting the PHM_ register > 0 and setting either ENA_ or ENB_ high enables the pulse-off Assist circuit. In addition, the circuit is only active when MARKER is high and either output is enabled. During a pulse-off event, laser voltage is momentarily connected to 3.3V to improve turn-off time of slow lasers. Note that the pulse-off assist is only effective when the OSA_ and OSB_ registers are set to zero during pulse-off.

Compliance Voltage Sensor

The output voltage affects overshoot, settling time and linearity. The compliance alarm detects output voltage lower than a programmed threshold (Table 6) and sets the Compliance Alarm (VALM_) bit (Figure 12). The alarm is cleared when read. The compliance alarm can be used to adjust laser power supplies after video data containing 50ns of bright pixels has been transmitted (Figure 13). The VALM bit will typically be set at power-on.

Table 6. Compliance Alarm Setpoint

VSET_[3:0]	TYPICAL COMPLIANCE VOLTAGE THRESHOLD (V)
0000*	**0.40**
0001	0.48
0010	0.56
	. . .
1110	1.52
1111	1.60

**Power-on default*

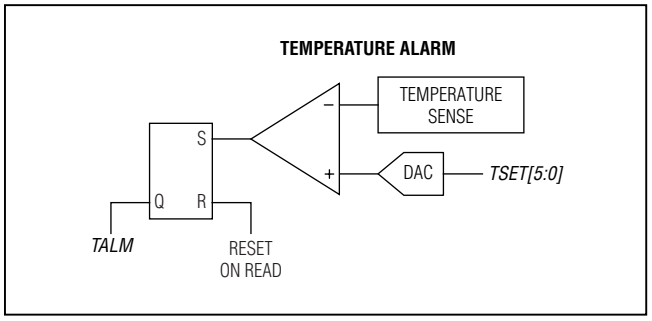


Figure 14. Temperature Alarm

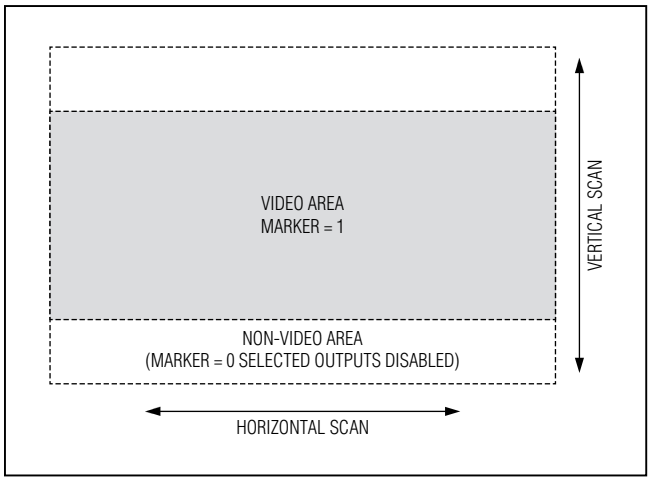


Figure 15. Video Marker

Table 7. Video Demultiplexer Selection Logic

MS[2:0]	PIXEL CLOCK SOURCE	VIDEO 1	VIDEO 2	VIDEO 3
000*	**DCLK**	**A1**	**A2**	**A3**
001	DCLK	B1	B1	B1
010	D8**	C1	C2	C3
011	D8**	C2	C2	C2
100	D8**	C2	C2	C3
101	D8**	C2	C3	C3
110	RESERVED			
111	RESERVED			

**Power-on default*

***D8 is gated by DCLK*

Temperature Alarm

The temperature alarm reports if the driver temperature has exceeded a programmable threshold as shown in Figure 14. The alarm is cleared when the TALM register is read. If the die temperature is still above the threshold, the temperature alarm immediately re-asserts itself. The temperature threshold is programmed with the T_SET register. The temperature alarm threshold includes offset of the temperature sensor. Accuracy of the threshold is increased by calibration of the alarm at a known temperature.

For example, if it is desired to set a temperature alarm at T_J = +125°C: With T_A = +25°C and outputs disabled, ramp TSET and read TALM. The code $TSET_{25}$, where the alarm is set, corresponds to $T_J \approx$ +25°C. $TSET_{125} \approx TSET_{25}$ + 100°C/2.5°C/LSB.

Control Logic

The Control Logic provides video selection, laser enable, and power savings.

Video Selection

The video demultiplexers A, B, and C creates signals A1–A3, B1, and C1–C3. The MS bits select the input source video for VIDEO1, VIDEO2, and VIDEO3.

Laser Control

When EN_MAIN is low, all drivers are off. This signal works asynchronously (no clock is required to disable outputs).

The Video Marker (MARKER) input can be used to disable selected outputs when a video signal is not present (Figure 15). The VE[1:3] bit settings determine which outputs respond to the MARKER signal.

Serial Port and Registers

The MAX3601 contains an I²C interface and a 3-wire SPI interface. The communication mode is determined by the state of CS at power-on. If CS is high (tied to DVDD), I²C mode is selected. If CS is open or low at power-on, SPI mode is selected.

I²C Interface

The serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). The master generates the clock signal (Figure 16).

I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Voltage clamps on the input protect the device high-voltage spikes not exceeding the absolute maximum voltage rating.

Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse (Figure 17). Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section for more information).

Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is 9 bits long; 8 bits of data followed by the acknowledge bit.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high (Figure 18).

A START condition from the master signals the beginning of a transmission. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see Figure 19 for more information). The STOP condition frees the bus. To issue a series of commands to the slave, the master may issue repeated START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a repeated START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the MAX3601 internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

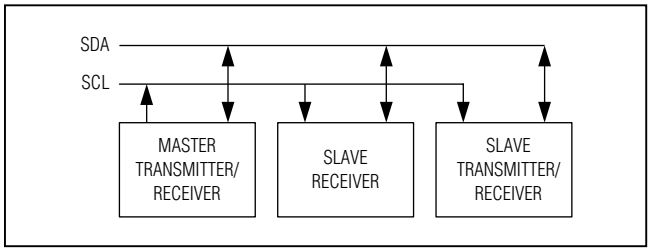


Figure 16. I²C Master/Slave Configuration

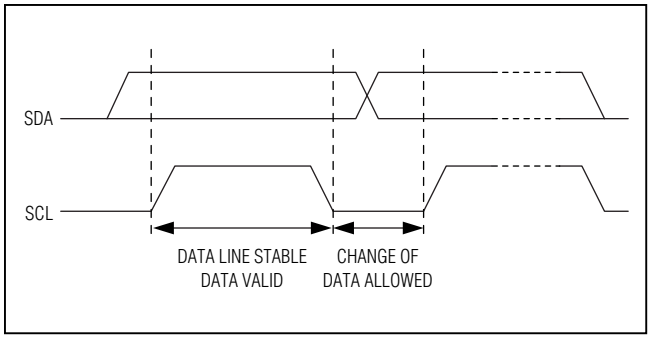


Figure 17. I²C Bit Transfer

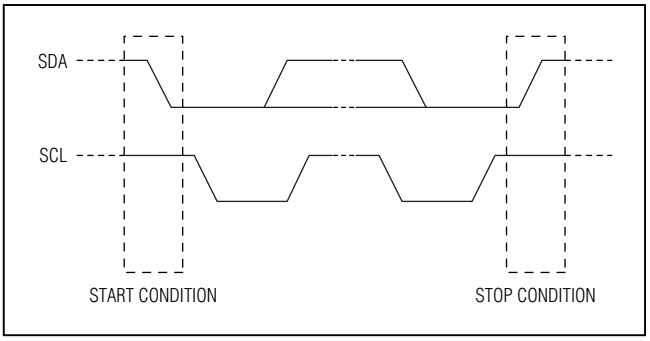


Figure 18. I²C START and STOP Conditions

Acknowledge

Both the master and the MAX3601 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each 9-bit data packet (Figure 19). To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a not acknowledge (NA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

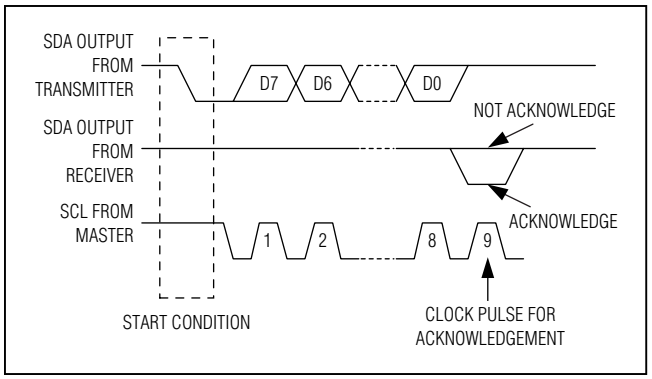


Figure 19. I²C Acknowledge

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by the slave address. The slave address byte consists of 7 address bits (1110 001) and a read/write bit (R/$\overline{W}$) which is a 0 for write and a 1 for read. After receiving the proper address, the MAX3601 issues an acknowledge by pulling SDA low during the ninth clock cycle. The MAX3601 write address is 0xE2. MAX3601 read address is 0xE3.

I²C Communication Protocols

The following I²C communications protocols are supported by the MAX3601

1) Writing to a Single Register
2) Writing to Sequential Registers
3) Reading from a Single Register
4) Reading from Sequential Registers

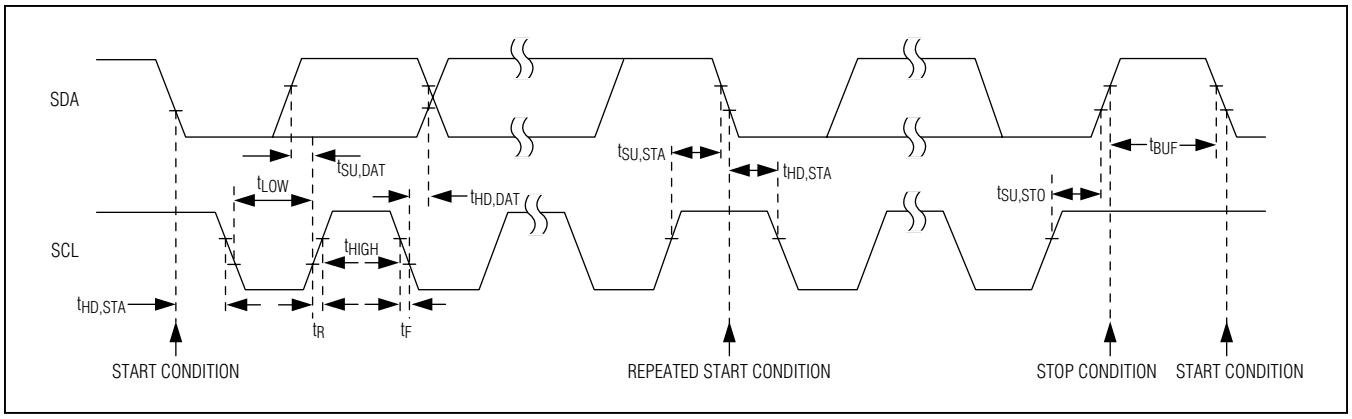


Figure 20. I²C Timing Diagram

Writing to a Single Register

Figure 21 shows the protocol for the I²C master device to write one byte of data to the MAX3601. The "write byte" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data
8) The slave acknowledges the data byte.
9) The master sends a STOP condition.

Writing to Sequential Registers

Figure 21 shows the protocol for the I²C master device to sequentially write data to the MAX3601. The sequential write protocol is as follows

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) Steps 6 to 8 are repeated as many times as the master requires.
10) The master sends a STOP condition.

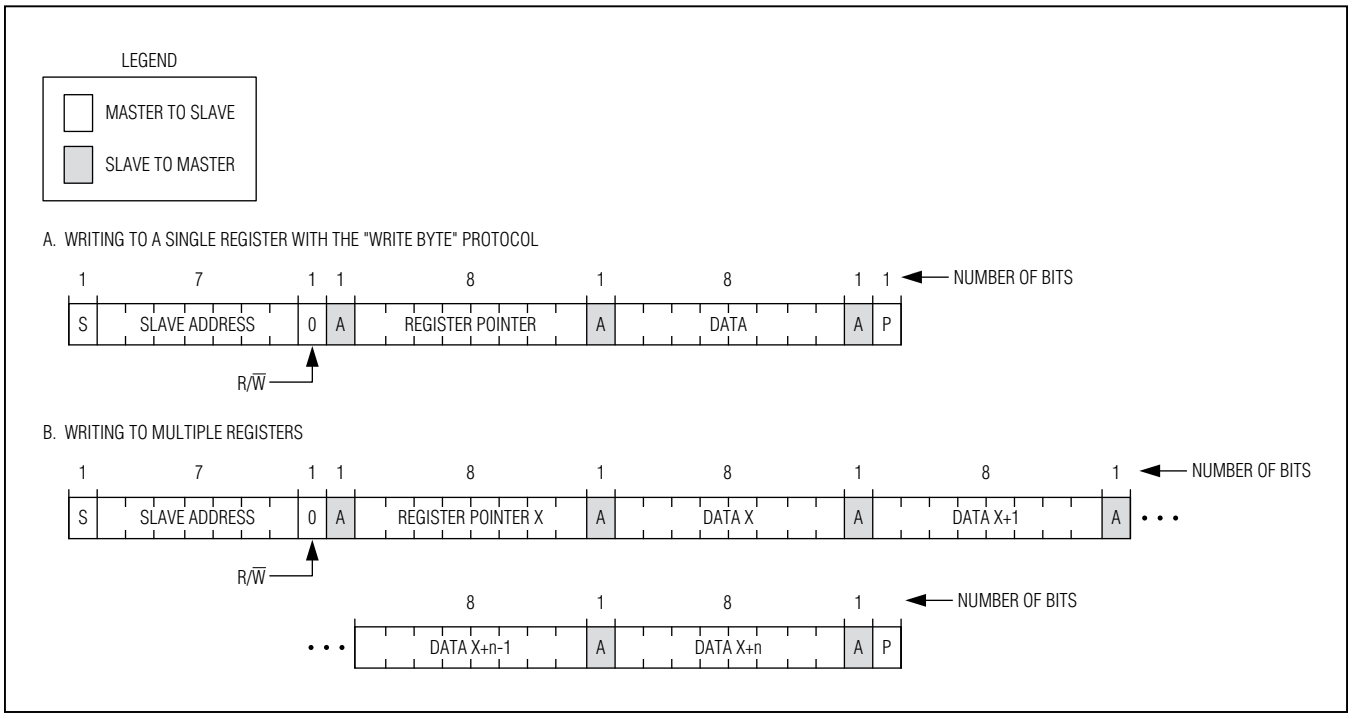


Figure 21. I²C Writing

Reading from a Single Register

Figure 22 shows the protocol for the I²C master device to read one byte of data to the MAX3601.

The "read byte" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit.
8) The addressed slave asserts acknowledge by pulling SDA low.
9) The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10) The master issues a not-acknowledge (NA).
11) The master issues a STOP condition (P).

The procedure (6) Sr cannot be replaced to STOP (P) and START (S).

Reading from Sequential Registers

Figure 22 shows the protocol for reading from sequential registers. This protocol is similar to the "read byte" protocol except the master issues an acknowledge to signal the slave that it wants more data. When the master has all the data it requires, it issues a not-acknowledge (NA) and a STOP (P) to end the transmission. The "continuous read from sequential registers" protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit.
8) The addressed slave asserts acknowledge by pulling SDA low.
9) The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.

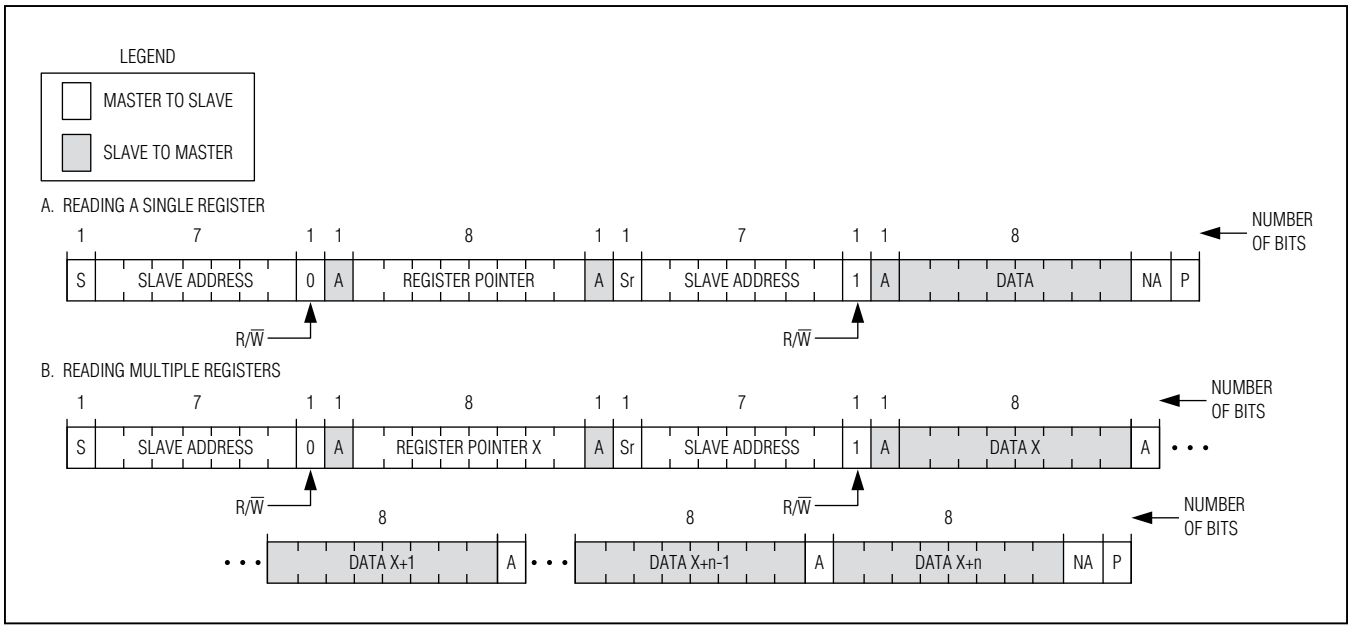


Figure 22. I²C Reading

10) The master issues acknowledge (A) signaling the slave that it wishes to receive more data.
11) Steps 9 and 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not-acknowledge (NA) to signal that it wishes to stop receiving data.
12) The master issues a STOP condition (P).

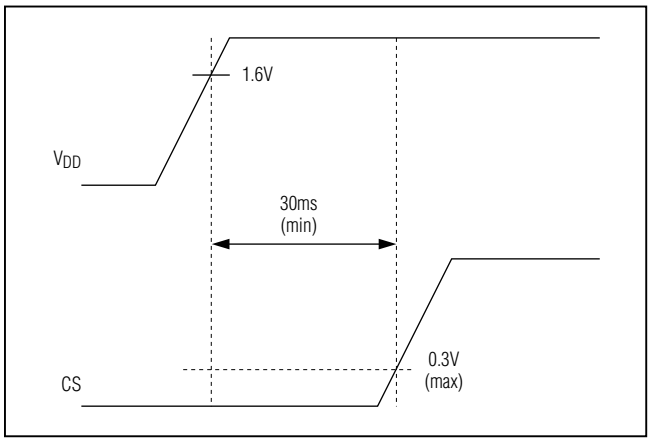


Figure 23. AVDD, DVDD, and CS Timing for SPI Mode

SPI Interface

Use the power-on and CS timing shown in Figure 23 when using the SPI interface.

Read/Write Data Using 3-Wire SPI

For both read/write, first set chip select (CS) high (Figure 24). Once the clock starts, specify the first bit (read/write data), then the register address and then the data. The SPI interface supports single byte and burst read/writes.

Read and write commands use MSB first. During a burst read/write, the register address auto-increments. Auto-incrementing is cyclic; address 0x00 follows address 0x7F.

When writing data, the data needs to be entered in 8-bit units. If the 8-bit data is not complete before CS goes to 0, the data will not be written correctly (Figure 25).

When reading data, DIO changes from input to output after receiving the address bits (Figure 26). To prevent collision, switch the microcontroller port driving DIO to an input or use open-drain logic.

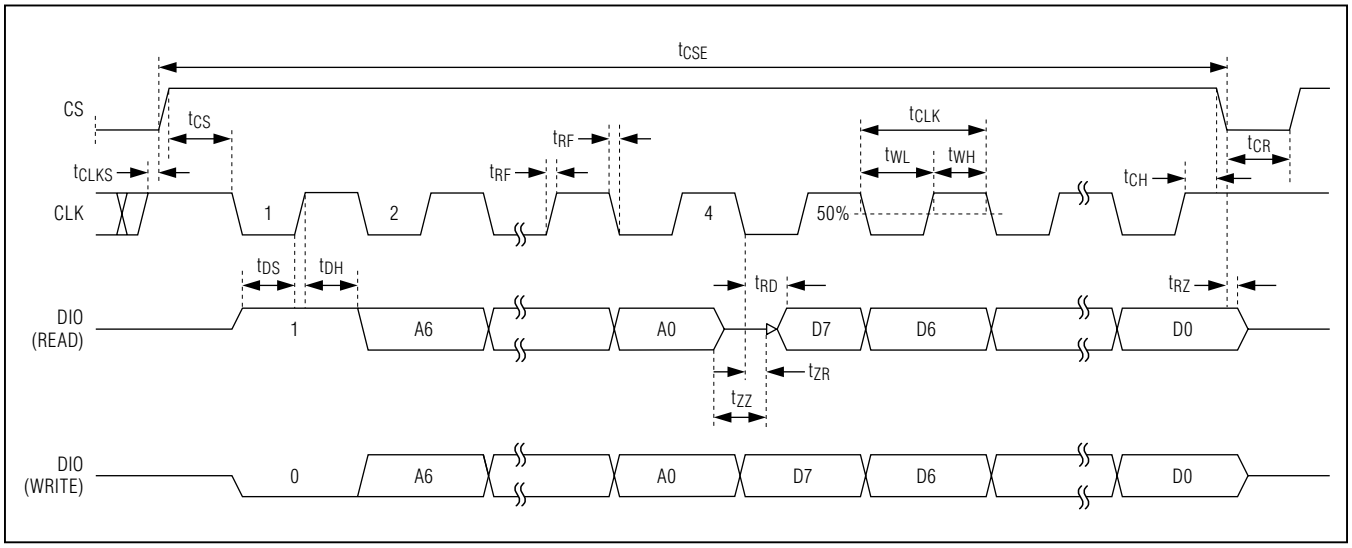


Figure 24. SPI Timing

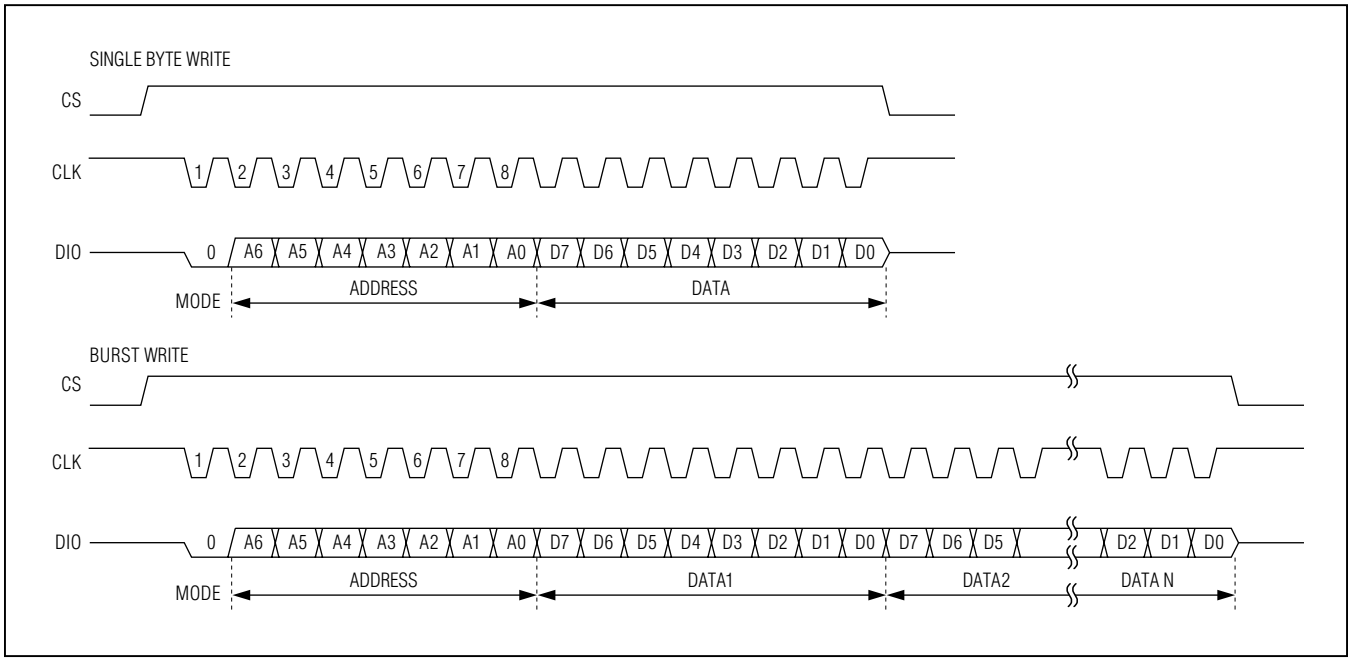


Figure 25. SPI Write Timing

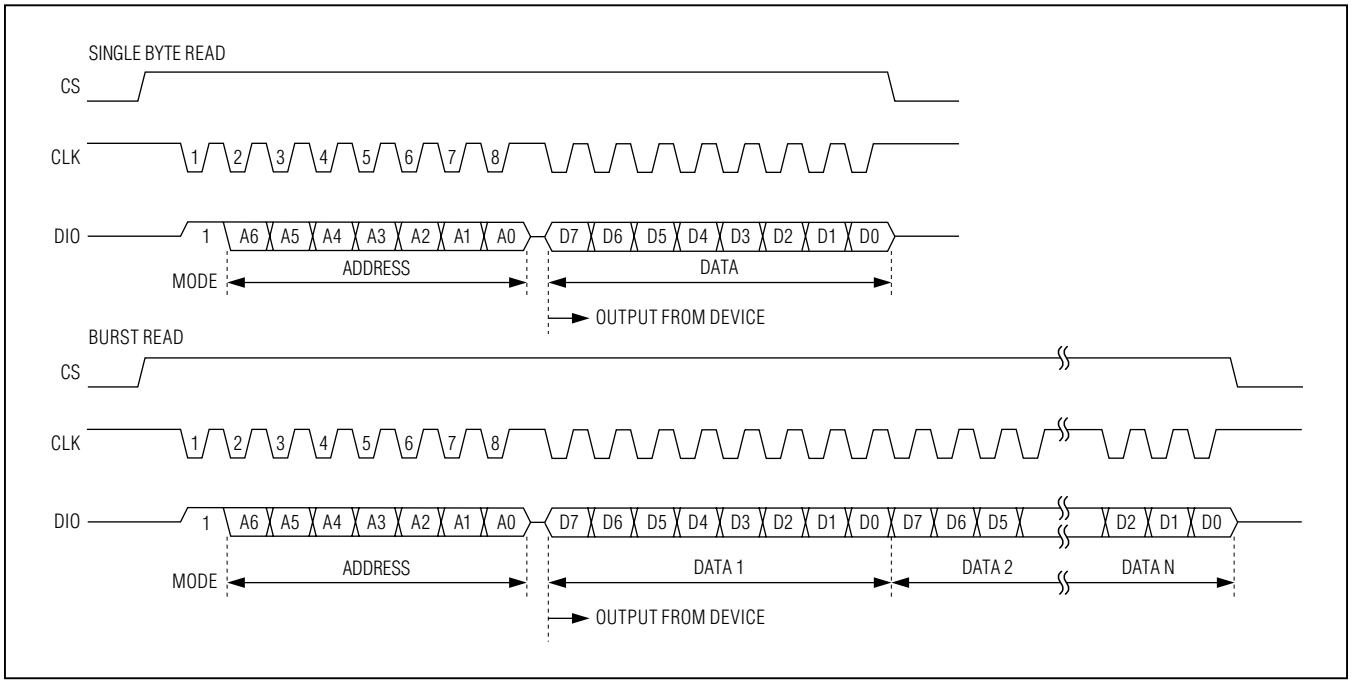


Figure 26. SPI Read Timing

Table 8. Register Table

ADDRESS [hex]	NAME	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT (hex)
0x00	DEVID	Device Identification	0 (MSB)	0	0	0	1	1	1	0	0x0E (READ ONLY)
0x01			0	0	0	1	0	0	0	1 (LSB)	0x11 (READ ONLY)
0x02	VER1	Version Identification 1	X	X	X	0	0	0	0	1	0x01
0x03	VER2	Version Identification 2	X	X	X	X	X	X	X	TG	0x0X (READ ONLY)
0x04	TSET	Temperature Setpoint	X	X	MSB					LSB	0x00
0x05	TALM	Temperature Alarm	X	X	X	X	X	X	X	AL	0x00 (READ ONLY)
0x06	VALM	Voltage Alarm	X	X	X	X	X	AL3	AL2	AL1	0x00 (READ ONLY)
0x07	OE	Output Enable	X	X	OEB3	OEA3	OEB2	OEA2	OEB1	OEA1	0x00
0x08	VE	Video Marker Enable	X	X	X	X	X	VE3	VE2	VE1	0x00
0x09	MS	Demux Mode Select	X	X	X	X	X	MSB		LSB	0x00
0x0A	—	RESERVED	X	X	X	X	X	X	X	X	0x00
0x0B	SP_EN	Subpixel Generator Enable	X	X	X	X	X	X	X	SP_EN	0x00
0x0C	SP	Subpixel Select	X	X	X	X	X	MSB		LSB	0x01
0x0D	SP_T	Subpixel Tuning	X	X	X	X	X	SP_T2	SP_T1	SP_T0	0x04
0x10	VSA1	OUT1 Video Select A	X	X	X	X	X	MSB		LSB	0x00
0x11	VSB1	OUT1 Video Select B	X	X	X	X	X	MSB		LSB	0x00
0x12	GA1	OUT1 DAC A Gain	MSB							LSB	0x00
0x13	GB1	OUT1 DAC B Gain	MSB							LSB	0x00
0x14	OSA1	OUT1 DAC A Offset	MSB							LSB	0x00

Table 8. Register Table (continued)

ADDRESS [hex]	NAME	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT (hex)
0x15	OSB1	OUT1 DAC B Offset	MSB							LSB	0x00
0x16	POM1	OUT1 Pulse-Off Assist Mask	MSB								0x00
0x17										LSB	0x00
0x18	PHM1	OUT1 Pulse-Assist Mask	MSB								0x00
0x19										LSB	0x00
0x1A	PHS1	OUT1 Pulse-Assist strength	X	X	X	X	X	X	MSB	LSB	0x00
0x1B	VSET1	OUT1 Compliance Alarm	X	X	X	X	MSB			LSB	0x00
0x20	VSA2	OUT2 Video Select A	X	X	X	X	X	MSB		LSB	0x00
0x21	VSB2	OUT2 Video Select B	X	X	X	X	X	MSB		LSB	0x00
0x22	GA2	OUT2 DAC A Gain	MSB							LSB	0x00
0x23	GB2	OUT2 DAC B Gain	MSB							LSB	0x00
0x24	OSA2	OUT2 DAC A Offset	MSB							LSB	0x00
0x25	OSB2	OUT2 DAC B Offset	MSB							LSB	0x00
0x26	POM2	OUT2 Pulse-Off Mask	MSB								0x00
0x27										LSB	0x00
0x28	PHM2	OUT2 Pulse-Assist Mask	MSB								0x00
0x29	PHM2									LSB	0x00
0x2A	PHS2	OUT2 Pulse-Assist Strength	X	X	X	X	X	X	MSB	LSB	0x00
0x2B	VSET2	OUT2 Compliance Alarm	X	X	X	X	MSB			LSB	0x00
0x30	VSA3	OUT2 Video Select A	X	X	X	X	X	MSB		LSB	0x00
0x31	VSB3	OUT2 Video Select B	X	X	X	X	X	MSB		LSB	0x00
0x32	GA3	OUT2 DAC A Gain	MSB							LSB	0x00
0x33	GB3	OUT2 DAC B Gain	MSB							LSB	0x00

Table 8. Register Table (continued)

ADDRESS [hex]	NAME	DESCRIPTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT (hex)
0x34	OSA3	OUT2 DAC A Offset	MSB							LSB	0x00
0x35	OSB3	OUT2 DAC B Offset	MSB							LSB	0x00
0x36	POM3	OUT2 Pulse-Off Mask	MSB								0x00
0x37										LSB	0x00
0x38	PHM3	OUT2 Pulse-Assist Mask	MSB								0x00
0x39										LSB	0x00
0x3A	PHS3	OUT2 Pulse-Assist Strength	X	X	X	X	X	X	MSB	LSB	0x00
0x3B	VSET3	OUT2 Compliance Alarm	X	X	X	X	MSB			LSB	0x00
0x40	DG1	Diagnostic 1	X	X	X	X	MSB				0x00 (READ ONLY)
0x41										LSB	0x00 (READ ONLY)
0x42	DG2	Diagnostic 2	X	X	X	X	PORB	DCLK	MARKER	EN-MAIN	0x00 (READ ONLY)
0x43	DG3	Diagnostic 3	PH3_EN	PH2_EN	PH1_EN	CMPS3_EN	CMPS2_EN	CMPS1_EN	TS_EN	BIAS_EN	0x00 (READ ONLY)
0x44	RST	Soft Reset	X	X	X	X	X	X	X	RST	0x00
0x45	—	RESERVED	X	X	X	X	X	X	X	X	0x00
0x46	—	RESERVED	X	X	X	X	X	X	X	X	0x00
0x47	POC1	Pulse-Off Config 1	X	X	X	MSB				LSB	0x00
0x48	POC2	Pulse-Off Config 2	X	X	X	MSB				LSB	0x00
0x49	POC3	Pulse-Off Config 3	X	X	X	MSB				LSB	0x00

Power-On-Reset

The power-on-reset monitors the supply voltages of the circuit. It is recommended that AVCC/DVCC and AVDD/DVDD be applied before V_{A1}-V_{A3} are applied. On power-down, it is recommended that V_{A1}-V_{A3} are powered down before AVCC/DVCC and AVDD/DVDD. Failure to follow the sequencing recommendation may result in device stress, but has not been observed to cause immediate damage.

- The pulse-off Assist function connects the driver output to AVCC (+3.3V). To prevent laser damage from reverse voltage, the pulse-off Assist function should only be enabled after V_A > AVCC. The pulse-off Assist defaults to disabled at power-on (The signal PH_EN_ is low).

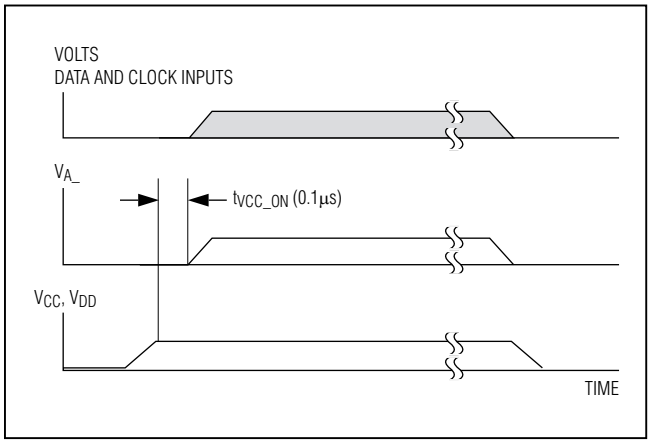


Figure 27. Power-Supply Sequencing

Design Procedure

Select Lasers

Figure 28 shows the model of the driver output and laser. Table 9 lists the component values for typical lasers of various colors.

Supply Filter

Element C_F (see the *Typical Operating Circuits*) is present to reduce supply noise and provide a ground return path for switched current. C_F can be composed of two or three capacitors in parallel. Use care to ensure V_A does not exceed 8.4V at any time, including power-on, as this can damage the ESD protection circuitry.

Table 9. Typical Laser Diode Parameters

PARAMETER	RED	GREEN	BLUE	UNITS
V_F	1.9	2.3	2.5	V
V_{D1} at 10mA	0.4	1.5	1	V
R_1	4	9	20	Ω
C_1	50	50	50	pF
L1	4	4	4	nH
Z0	20	20	20	Ω
Length	1.5	1.5	1.5	cm
R_{LK}	5	5	5	MΩ
I_{PEAK} (Continuous)	300	250	125	mA
V_F at I_{PEAK}	3.8	8.2	6	V

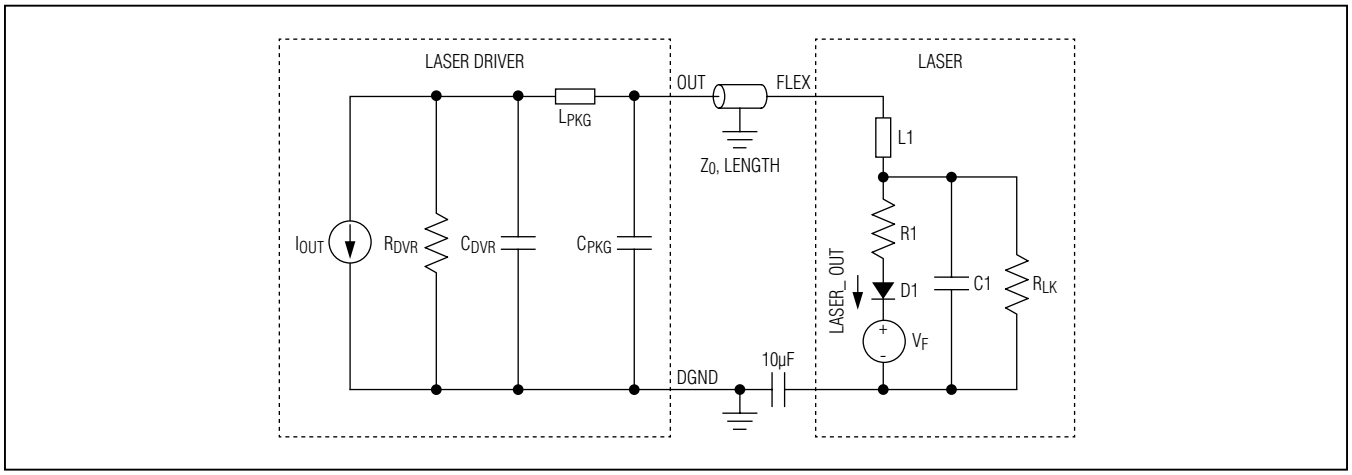


Figure 28. Laser and Package Model

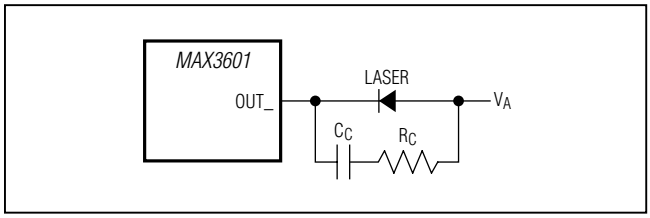


Figure 29. Optional Compensation Components

Compensation Network

Optional compensation elements R_C and C_C can be used to compensate the inductive load of the laser (Figure 29). The resulting filter reduces ringing and increases the switching time of the laser driver. The best values for R_C and C_C should be found by experimentation, as these values are different for each application. Note that C_C must be charged before light output appears from the laser. If a compensation network is used, minimize inductance in the ground return. Typical starting values:

$R_C \approx R_L$ to 2 x R_L (R_L = Laser Resistance)

$C_C \approx 1/(2\pi f_{VIDEO} \times R_L)$

PCB Layout

Place the lasers as close as possible to the laser driver. The laser connection should appear as a low-impedance transmission line. Use wide traces located close to the ground plane for maximum capacitance. The connection from OUT_ to the laser should be as short as possible, ideally < 15mm.

Consider the laser power supply $V_{A\_}$. Droop on these supplies reduces the compliance voltage. Use two or three capacitors to bypass $V_{A\_}$ to ground. Place a small capacitor as close as possible to the laser to keep the ground return loop small. A larger capacitor can be located farther from $V_{A\_}$. It is best to solder the laser to the PCB. If a connector is required, minimize inductance. Inductance > 1nH at OUT_ could cause large ringing.

Laser Driver Thermal Considerations

The circuit is designed to meet specifications with an operating junction temperature (T_J) up to +125°C. The controlling system must be designed to monitor the temperature register and adjust laser current to prevent overheating. The junction temperature is estimated by:

$$T_J \approx [(I\_VDD)(V\_VDD) + (I\_VCC)(V\_VCC) + \Sigma(I_{VA\_})(V_{A\_} - V_{D\_})]\ \theta_{JA} + T_A$$

where:

$I_{VA\_}$ is the laser diode current

$V_{A\_}$ is the laser supply voltage

$V_{D\_}$ is the voltage drop across the laser diode.

θ_{JA} is the junction to ambient thermal resistance

T_A is the ambient temperature

The recommended thermal path is through the package backside exposed pad (EP). A heatsink on the package top does not significantly reduce junction temperature. Recommendations for PCB design are found in Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Applications Information

Connecting Multiple Outputs

It is possible to connect the outputs together to achieve a higher output current.

Eye Safety

Specification IEC 825 defines the maximum safe output of optical devices. This laser driver provides features that aid compliance with IEC 825. Using this laser driver alone does not ensure that a product is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Maxim products are not designed for use as components in systems where the failure of a Maxim product could create a condition where human injury may occur.

Wafer-Level Packaging (WLP) Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results refer to Application Note 1891: *Wafer-Level Packaging (WLP) and its Applications*.

Table 10. Detailed Register Table (see Table 8)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:0]	DEVID1	XXXXXXXX	Device ID MSBs (0x0E)	00001110 (Read only)
0x01	D[7:0]	DEVID2	XXXXXXXX	Device ID LSBs (0x11)	00010001 (Read only)
0x02	D[7:5]	—	000	Reserved	000 (Read only)
	D[4:0]	VER1	00001	Version Identification 1 (0x01)	00001 (Read only)
0x03	D[7:1]	—	00000XX	Reserved	00000XX (Read only)
	D0	TG	0	Commercial temperature grade (0°C to 70°C)	X (Read only)
			1	Automotive temperature grade (-40°C to +105°C)	
0x04	D[7:6]	—	00	Reserved	00
	D[5:0]	TSET	XXXXXX	Temperature alarm setpoint	000000
0x05	D[7:1]	—	0000000	Reserved	0000000 (Read only)
	D0	TALM	0	No temperature alarm	0 (Read only)
			1	Temperature alarm exceeded (Bit clears when read)	
0x06	D[7:3]	—	00000	Reserved	00000 (Read only)
	D2	AL3	0	OUT3 compliance voltage normal	0 (Read only)
			1	OUT3 low compliance voltage alarm (Cleared when read)	
	D1	AL2	0	OUT2 compliance voltage normal	0 (Read only)
			1	OUT2 low compliance voltage alarm (Cleared when read)	
	D0	AL1	0	OUT1 compliance voltage normal	0 (Read only)
			1	OUT1 low compliance voltage alarm (Cleared when read)	

Table 10. Detailed Register Table (see Table 8) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x07	D[7:6]	—	00	Reserved	00
	D5	OEB3	0	Output 3 DAC B disabled	0
			1	Output 3 DAC B enabled	
	D4	OEA3	0	Output 3 DAC A disabled	0
			1	Output 3 DAC A enabled	
	D3	OEB2	0	Output 2 DAC B disabled	0
			1	Output 2 DAC B enabled	
	D2	OEA2	0	Output 2 DAC A disabled	0
			1	Output 2 DAC A enabled	
	D1	OEB1	0	Output 1 DAC B disabled	0
			1	Output 1 DAC B enabled	
	D0	OEA1	0	Output 1 DAC A disabled	0
			1	Output 1 DAC A enabled	
0x08	D[7:3]	—	00000	Reserved	00000
	D2	VE3	0	MARKER input does not affect OUT3	0
			1	OUT3 disabled when MARKER is high	
	D1	VE2	0	MARKER input does not affect OUT2	0
			1	OUT2 disabled when MARKER is high	
	D0	VE1	0	MARKER input does not affect OUT1	0
			1	OUT1 disabled when MARKER is high	
0x09	D[7:3]	—	00000	Reserved	00000
	D[3:0]	MS	**000**	Video demux mode select (see Table 7) Select Demux A **(Power-on default)**	**000**
			001	Select Demux B	
			010	Select Demux C (C1, C2, C3)	
			011	Select Demux C (C2, C2, C2)	
			100	Select Demux C (C2, C2, C3)	
			101	Select Demux C (C2, C3, C3)	
			11X	Do not use	
0x0A	D[7:0]	—	00000000	Reserved	00000000
0x0B	D[7:6]	—	0000000	Reserved	0000000
	D0	SP_EN	0	Disable subpixel generator	0
			1	Enable subpixel generator	
0x0C	D[7:3]	—	00000	Reserved	00000
	D[2:0]	SP	XXX	Subpixel Programming See Table 3	001

Table 10. Detailed Register Table (see Table 8) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0D	D[7:3]	—	00000	Reserved	00000
	D2	SP_T2	X	Subpixel tuning. Do not change from default	1
	D1	SP_T1	X	Do not change from default	0
	D0	SP_T0	X	Do not change from default	0
0x10	D[7:3]	—	00000	Reserved	00000
	D[2:0]	VSA1	**000**	OUT1 DACA video select (see Table 4) Video output with zero output pulse-off (**Power-on default)**	000
			001	Video output with offset output pulse-off	
			010	Offset output with zero output pulse-off	
			011	Offset output	
			100	Offset output (if video data is present) with zero output pulse-off	
			101	Zero output	
			11X	Zero output	
0x11	D[7:3]	—	00000	Reserved	00000
	D[2:0]	VSB1	**000**	OUT1 DACB video select (see Table 5) Video output with zero output pulse-off (**Power-on default)**	000
			001	Video output with offset output pulse-off	
			010	Offset output with zero output pulse-off	
			011	Offset output	
			100	Offset output (if video data is present) with zero output pulse-off	
			101	Zero output	
			11X	Zero output	
0x12	D[7:0]	GA1	XXXXXXXX	OUT1 DAC A gain setting	00000000
0x13	D[7:0]	GB1	XXXXXXXX	OUT1 DAC B gain setting	00000000
0x14	D[7:0]	OSA1	XXXXXXXX	OUT1 DAC A offset setting	00000000
0x15	D[7:0]	OSB1	XXXXXXXX	OUT1 DAC B offset setting	00000000
0x16	D[7:0]	POM1	XXXXXXXX	OUT1 Pulse-off mask MSBs (see Figure 9)	00000000
0x17	D[7:0]		XXXXXXXX	OUT1 Pulse-off mask LSBs	00000000
0x18	D[7:0]	PHM1	XXXXXXXX	OUT1 Pulse-Assist mask MSBs (see Figure 9)	00000000
0x19	D[7:0]		XXXXXXXX	OUT1 Pulse-off mask LSBs	00000000

Table 10. Detailed Register Table (see Table 8) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x1A	D[7:2]	—	000000	Reserved	000000
	D[1:0]	PHS1	**00**	OUT1 pulse-off Assist uses 64Ω resistance **(Power-on default)**	**00**
			01	32Ω pulse-off Assist resistance	
			10	16Ω pulse-off Assist resistance	
			11	8Ω pulse-off Assist resistance	
0x1B	D[7:4]	—	0000	Reserved	0000
	D[3:0]	VSET1	XXXX	OUT1 compliance alarm setpoint (see Table 6)	0000
0x20	D[7:3]	—	00000	Reserved	00000
	D[2:0]	VSA2	**000**	OUT2 DACA video select (see Table 4) Video output with zero output pulse-off (**Power-on default)**	000
			001	Video output with offset output pulse-off	
			010	Offset output with zero output pulse-off	
			011	Offset output	
			100	Offset output (if video data is present) with zero output pulse-off	
			101	Zero output	
			11X	Zero output	
0x21	D[7:3]	—	00000	Reserved	00000
	D[2:0]	VSB2	**000**	OUT2 DACB video select (see Table 5) Video output with zero output pulse-off (**Power-on default)**	000
			001	Video output with offset output pulse-off	
			010	Offset output with zero output pulse-off	
			011	Offset output	
			100	Offset output (if video data is present) with zero output pulse-off	
			101	Zero output	
			11X	Zero output	
0x22	D[7:0]	GA2	XXXXXXXX	OUT2 DAC A gain setting	00000000
0x23	D[7:0]	GB2	XXXXXXXX	OUT2 DAC B gain setting	00000000
0x24	D[7:0]	OSA2	XXXXXXXX	OUT2 DAC A offset setting	00000000
0x25	D[7:0]	OSB2	XXXXXXXX	OUT2 DAC B offset setting	00000000
0x26	D[7:0]	POM2	XXXXXXXX	OUT2 pulse-off mask MSBs (see Figure 9)	00000000
0x27	D[7:0]		XXXXXXXX	OUT2 pulse-off mask LSBs	00000000

Table 10. Detailed Register Table (see Table 8) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x28	D[7:0]	PHM2	XXXXXXXX	OUT2 pulse-Assist mask MSBs (see Figure 9)	00000000
0x29	D[7:0]		XXXXXXXX	OUT2 pulse-off mask LSBs	00000000
0x2A	D[7:2]	—	000000	Reserved	000000
	D[1:0]	PHS2	**00**	OUT2 pulse off Assist uses 64Ω resistance **(Power-on default)**	**00**
			01	32Ω pulse-off Assist resistance	
			10	16Ω pulse-off Assist resistance	
			11	8Ω pulse-off Assist resistance	
0x2B	D[7:4]	—	0000	Reserved	0000
	D[3:0]	VSET2	XXXX	OUT2 compliance alarm setpoint (see Table 6)	0000
0x30	D[7:3]	—	00000	Reserved	00000
	D[2:0]	VSA3	**000**	OUT3 DACA video select (see Table 4) Video output with zero output pulse-off (**Power-on default)**	000
			001	Video output with offset output pulse-off	
			010	Offset output with zero output pulse-off	
			011	Offset output	
			100	Offset output (if video data is present) with zero output pulse-off	
			101	Zero output	
			11X	Zero output	
0x31	D[7:3]	—	00000	Reserved	00000
	D[2:0]	VSB3	**000**	OUT3 DACB video select (see Table 5) Video output with zero output pulse-off (**Power-on default)**	000
			001	Video output with offset output pulse-off	
			010	Offset output with zero output pulse-off	
			011	Offset output	
			100	Offset output (if video data is present) with zero output pulse-off	
			101	Zero output	
			11X	Zero output	
0x32	D[7:0]	GA3	XXXXXXXX	OUT3 DAC A gain setting	00000000
0x33	D[7:0]	GB3	XXXXXXXX	OUT3 DAC B gain setting	00000000
0x34	D[7:0]	OSA3	XXXXXXXX	OUT3 DAC A offset setting	00000000
0x35	D[7:0]	OSB3	XXXXXXXX	OUT3 DAC B offset setting	00000000

Table 10. Detailed Register Table (see Table 8) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x36	D[7:0]	POM3	XXXXXXXX	OUT3 pulse-off mask MSBs (see Figure 9)	00000000
0x37	D[7:0]		XXXXXXXX	OUT3 pulse-off mask LSBs	00000000
0x38	D[7:0]	PHM3	XXXXXXXX	OUT3 pulse-Assist mask MSBs (see Figure 9)	00000000
0x39	D[7:0]		XXXXXXXX	OUT3 pulse-off mask LSBs	00000000
0x3A	D[7:2]	—	000000	Reserved	000000
	D[1:0]	PHS3	**00**	OUT3 pulse off Assist uses 64Ω resistance **(Power-on default)**	**00**
			01	32Ω pulse-off Assist resistance	
			10	16Ω pulse-off Assist resistance	
			11	8Ω pulse-off Assist resistance	
0x3B	D[7:4]	—	0000	Reserved	0000
	D[3:0]	VSET3	XXXX	OUT3 compliance alarm setpoint (see Table 6)	0000
0x40	D[7:4]	—	0000	Reserved	0000 (Read only)
	D[3:0]	DG1	XXXX	Diagnostic Register 1. Mirrors digital video input MSBs (D[11:8])	0000 (Read only)
0x41	D[7:0]	DG2	XXXXXXXX	Diagnostic Register 2. Mirrors digital video input LSBs (D[7:0])	00000000 (Read only)
0x42	D[7:4]	—	0000	Reserved	0000 (Read only)
	D3	PORB	0	Device in power-on-reset condition	0 (Read only)
			1	Normal Operation	
	D2	DCLK	X	Mirrors digital video input clock	0 (Read only)
	D1	MARKER	X	Mirrors MARKER input	0 (Read only)
	D0	EN_MAIN	X	Mirrors EN_MAIN input	0 (Read only)

Table 10. Detailed Register Table (see Table 8) (continued)

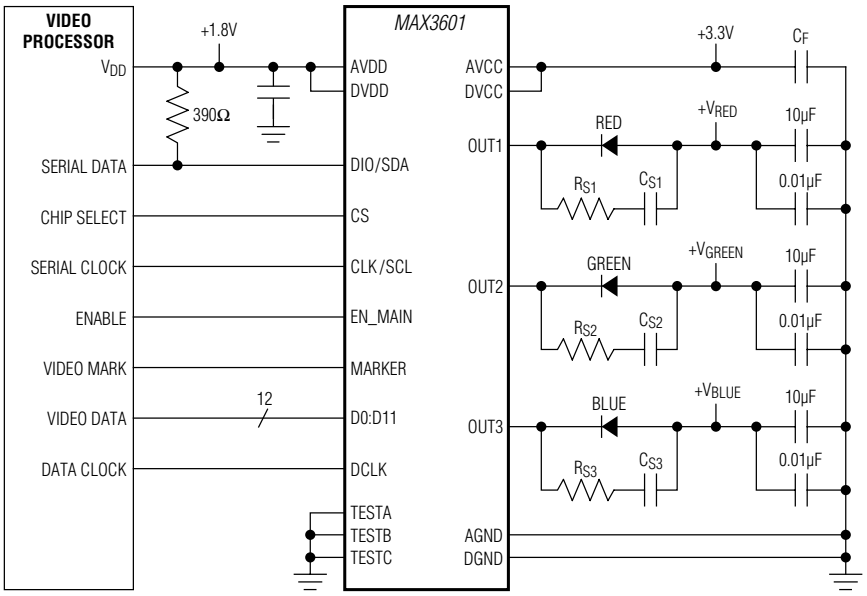
REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x43	D7	PH3_EN	0	OUT3 pulse-Assist disabled	0 (Read only)
			1	OUT3 pulse-Assist enabled	
	D6	PH2_EN	0	OUT2 pulse-Assist disabled	0 (Read only)
			1	OUT2 pulse-Assist enabled	
	D5	PH1_EN	0	OUT1 pulse-Assist disabled	0 (Read only)
			1	OUT1 pulse-Assist enabled	
	D4	CMPS3	0	OUT3 compliance sensor disabled	0 (Read only)
			1	OUT3 compliance sensor enabled	
	D3	CMPS2	0	OUT2 compliance sensor disabled	0 (Read only)
			1	OUT2 compliance sensor enabled	
	D2	CMPS1	0	OUT1 compliance sensor disabled	0 (Read only)
			1	OUT1 compliance sensor enabled	
	D1	TS_EN	0	Temperature sensor disabled	0 (Read only)
			1	Temperature sensor enabled	
	D0	BIAS_EN	0	Master bias voltage generator disabled	0 (Read only)
			1	Master bias voltage generator enabled	
0x44	D[7:1]	—	0000000	Reserved	0000000
	D0	RST	0	Normal operation	0
			1	Reset the device. bit always reads as a zero	
0x45	D[7:0]	—	00000000	Reserved	00000000
0x46	D[7:0]	—	00000000	Reserved	00000000
0x47	D[7:5]	—	000	Reserved	000
	D4	POC1[4]	0	OUT1 random pulse-off events synchronized to other outputs with POC_[4] = '0'	0
			1	OUT1 random pulse-off events are unsynchronized (Table 3)	
	D3	POC1[3]	0	OUT1 pulse-off events are random	0
			1	OUT1 pulse-off events occur every other pixel (Table 2)	
	D[2:0]	POC1[2:0]	XXX	OUT1 pulse-off duty cycle configuration (Table 2)	0

Table 10. Detailed Register Table (see Table 8) (continued)

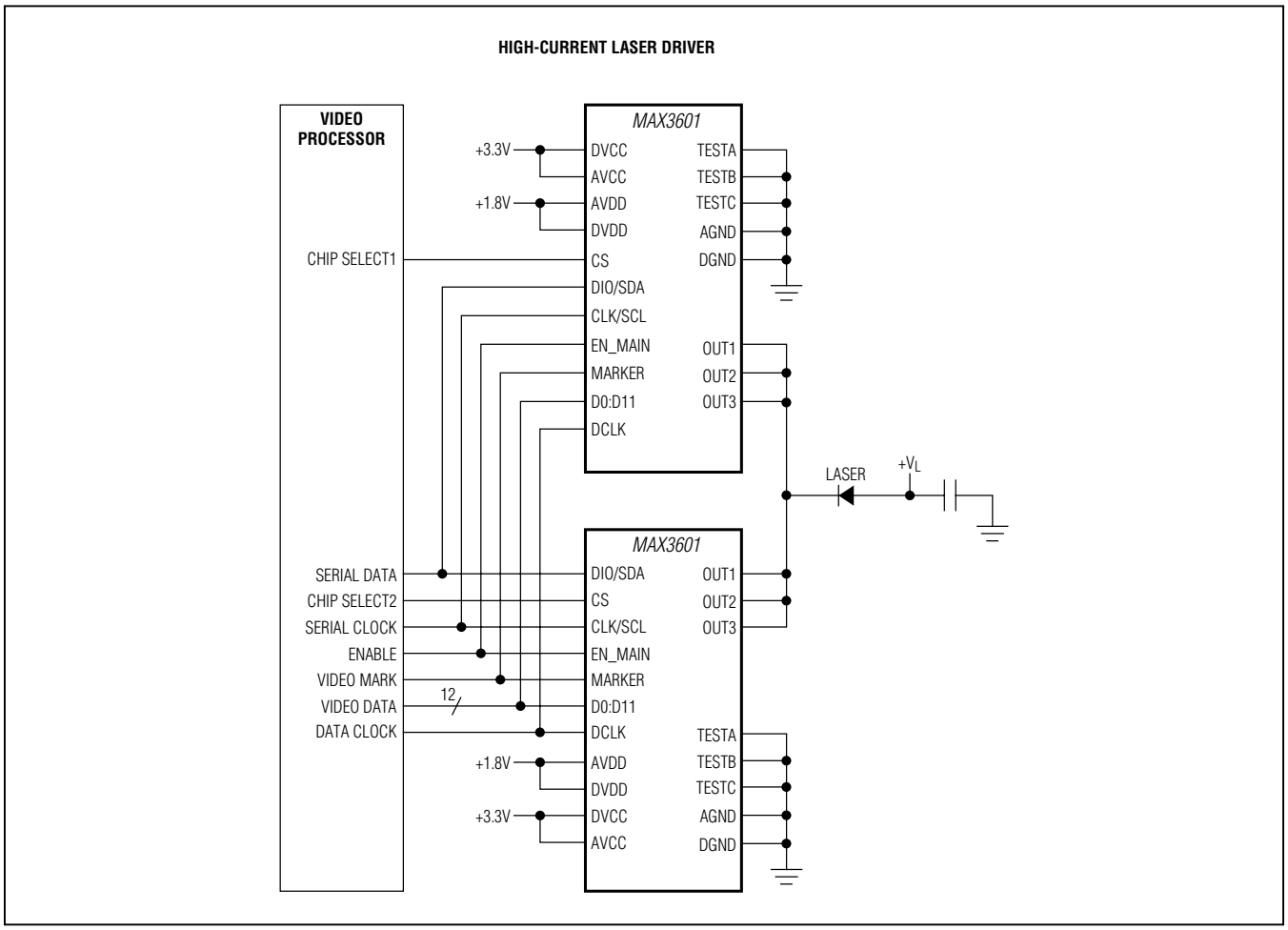
REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x48	D[7:5]	—	000	Reserved	000
	D4	POC1[4]	0	OUT2 random pulse-off events synchronized to other outputs with POC_[4] = '0'	0
			1	OUT2 random pulse-off events are unsynchronized (Table 3)	
	D3	POC1[3]	0	OUT2 pulse-off events are random	0
			1	OUT2 pulse-off events occur every other pixel (Table 2)	
	D[2:0]	POC1[2:0]	XXX	OUT2 pulse-off duty cycle configuration (Table 2)	0
0x49	D[7:5]	—	000	Reserved	000
	D4	POC1[4]	0	OUT3 random pulse-off events synchronized to other outputs with POC_[4] = '0'	0
			1	OUT3 random pulse-off events are unsynchronized (Table 3)	
	D3	POC1[3]	0	OUT3 pulse-off events are random	0
			1	OUT3 pulse-off events occur every other pixel (Table 2)	
	D[2:0]	POC1[2:0]	XXX	OUT3 pulse-off duty cycle configuration (Table 2)	0

Typical Operating Circuits

RGB LASER PROJECTOR



Typical Operating Circuits (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3601GTL+	-40°C to +105°C	40 TQFN-EP*
MAX3601CWO+	0°C to +70°C	42 WLP

+Denotes a lead (Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055N+1	21-0140	90-0103
42 WLP	W423E3+1	21-0440	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/12	Initial release	—
1	1/13	Updated the *Electrical Characteristics* table for I_{DVCC_G2B} and I_{AVCC}, Current at OUT parameter, t_H, and t_{RZ}; removed future status from the TQFN package in the *Ordering Information* table	7–10, 50
2	5/13	Updated SDA Hold Time in *Electrical Characteristics* table, Table 2, and Figure 10	10, 25, 26
3	3/15	Updated the *Absolute Maximum Ratings* and *Supply Filter* section to meet customer requirements.	6, 39