



AK1590

1GHz Delta-Sigma Fractional-N Frequency Synthesizer

1. Overview

AK1590 is a Delta-Sigma Fractional-N PLL (Phase Locked Loop) frequency synthesizer with a frequency switching function, covering a wide range of frequencies from 60 to 1000MHz. This product consists of an 18-bit Delta-Sigma modulator, a low-noise phase frequency comparator, a highly accurate charge pump, a reference divider and dual-module prescaler (P/P+1) and frequency offset adjustable circuits.

2. Features

- | | | |
|--------------------------|--|--|
| <input type="checkbox"/> | Operating frequency: | 60 to 1000MHz |
| <input type="checkbox"/> | Programmable charge pump current: | In a normal operating scheme, the charge pump current can be set in 8 steps, in the range from 20 to 168 μ A. In a Fast Lockup scheme, the charge pump current can be set in 8 steps, in the range from 0.8 to 2.3mA. |
| <input type="checkbox"/> | Supply Voltage: | 2.7 to 5.5 V (PVDD pin) |
| <input type="checkbox"/> | Separate power supply for the charge pump: | PVDD to 5.5V (CPVDD pin) |
| <input type="checkbox"/> | On-chip power-saving features | |
| <input type="checkbox"/> | Frequency offset adjustable function: | No glitch operation for AFC(Automatic Frequency Control) and DFM(Digital Frequency Modulation) |
| <input type="checkbox"/> | General-purpose output: | Two general-purpose output ports to control peripheral parts |
| <input type="checkbox"/> | Low phase noise: | -201dBc/Hz |
| <input type="checkbox"/> | Low consumption current: | 2.5mA typ |
| <input type="checkbox"/> | Package: | 24pin QFN (0.5mm pitch, 4mm \times 4mm \times 0.7mm) |
| <input type="checkbox"/> | Operating temperature: | -40 to +85°C |

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In this specification, the following notations are used for specific signal and register names:

[Name] : Pin name

<Name> : Register group name (Address name)

{Name} : Register bit name

3. Block Diagram

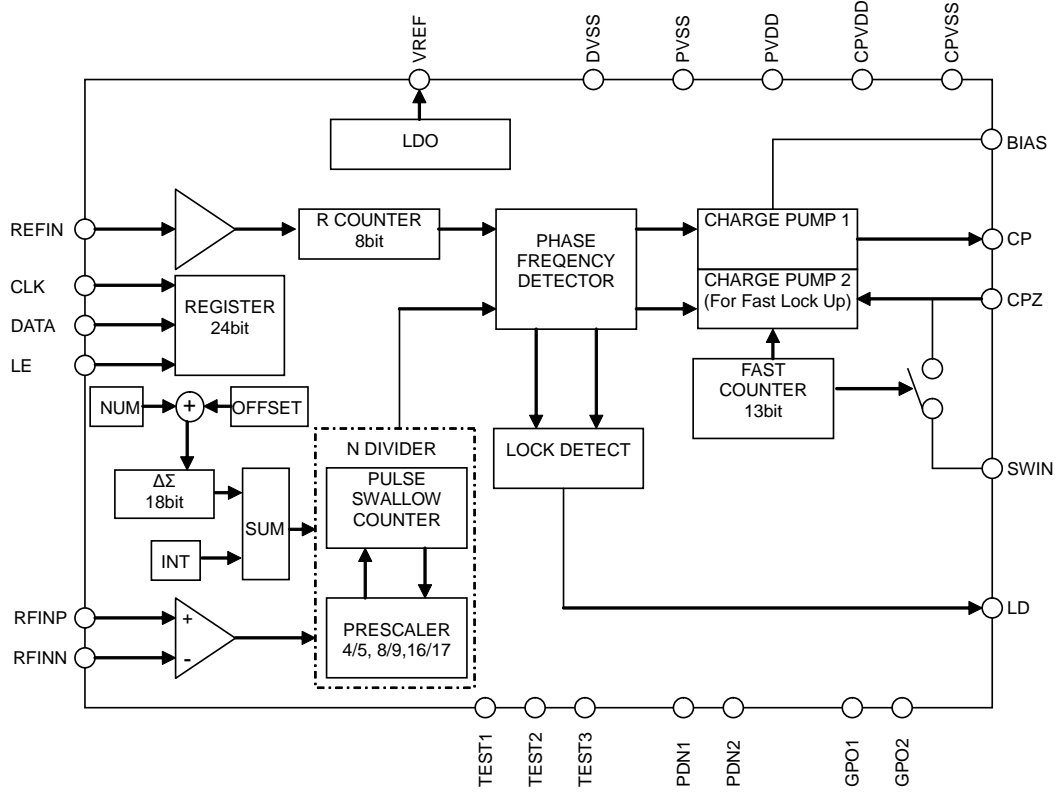


Fig. 1 Block Diagram

4. Pin Functional Description

Table 1 Pin Function

| No. | Name | I/O | Pin Functions | Power down | Remarks |
|-----|-------|-----|---|------------|---|
| 1 | CPVDD | P | Power supply for charge pump | | |
| 2 | TEST3 | DI | Test pin 3. This pin must be connected to ground. | | Internal pull-down, Schmidt trigger input |
| 3 | TEST1 | DI | Test pin 1. This pin must be connected to ground. | | Internal pull-down, Schmidt trigger input |
| 4 | LE | DI | Load enable | | Schmidt trigger input |
| 5 | DATA | DI | Serial data input | | Schmidt trigger input |
| 6 | CLK | DI | Serial clock | | Schmidt trigger input |
| 7 | LD | DO | Lock detect | Low | |
| 8 | PDN2 | DI | Power down pin for PLL | | Schmidt trigger input |
| 9 | PDN1 | DI | Power down signal for LDO | | Schmidt trigger input |
| 10 | REFIN | AI | Reference input | | |
| 11 | TEST2 | DI | Test pin 2. This pin must be connected to ground. | | Internal pull-down, Schmidt trigger input |
| 12 | GPO1 | DO | General-purpose output pin 1 | Low | |
| 13 | GPO2 | DO | General-purpose output pin 2 | Low | |
| 14 | DVSS | G | Digital ground pin | | |
| 15 | VREF | AIO | Connect to LDO reference voltage capacitor | Low | |
| 16 | RFINN | AI | Prescaler input | | |
| 17 | RFINP | AI | Prescaler input | | |
| 18 | PVDD | P | Power supply for peripherals | | |
| 19 | BIAS | AIO | Resistance pin for setting charge pump output current | | |
| 20 | PVSS | G | Ground pin for peripherals | | |
| 21 | CP | AO | Charge pump output | Hi-Z | |
| 22 | CPZ | AIO | Connect to the loop filter capacitor | | Note 1, Note 2 |
| 23 | SWIN | AI | Connect to resistance pin for Fast Lockup | | Note 1, Note 2 |
| 24 | CPVSS | G | Ground pin for charge pump | | |

Note 1) For detailed functional descriptions, see the section “Charge Pump and Loop Filter” in “8. Block Functional Description” below.

Note 2) The input voltage from [CPZ] pin is used in the internal circuit. [CPZ] pin must not be open even when the Fast Lockup feature is unused. For the output destination from [CPZ] pin, see “Fig.5 Loop Filter Schematic”.

[SWIN] pin could be open when the Fast Lockup feature is not used.

The state of loop filter switch is ON when “[PDN1]=Low, [PDN2]=Low” or “[PDN1]=High, [PDN2]=Low”.

Note 3) Power down means the state where [PDN1]=[PDN2]=Low after power on.

| | | | |
|------------------------|-----------------------|---------------------|-----------------------|
| AI: Analog input pin | AO: Analog output pin | AIO: Analog I/O pin | DI: Digital input pin |
| DO: Digital output pin | P: Power supply pin | G: Ground pin | |

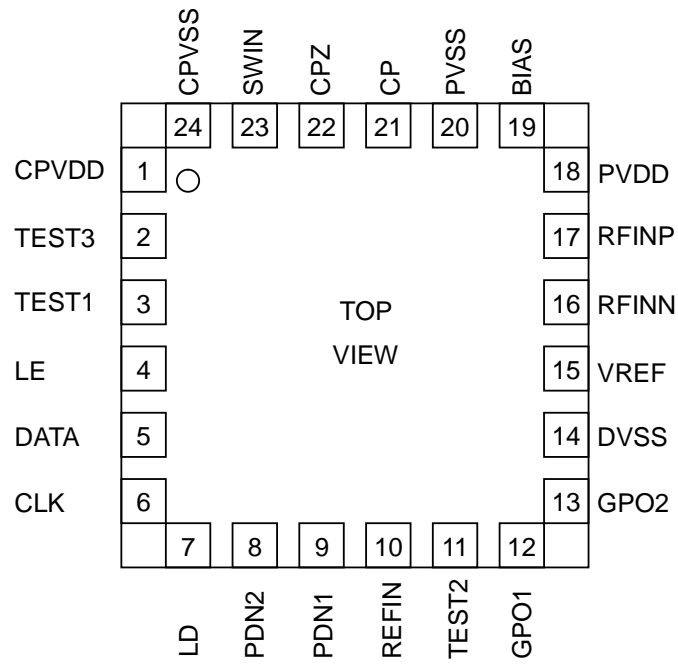


Fig. 2 Package Pin Layout

5. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit | Remarks |
|-----------------------|--------|----------|----------|------|------------------------------|
| Supply Voltage | VDD1 | -0.3 | 6.5 | V | Note 1, Note 2 |
| | VDD2 | -0.3 | 6.5 | V | Note 1, Note 3 |
| Ground Level | VSS1 | 0 | 0 | V | Voltage ground level, Note 4 |
| | VSS2 | 0 | 0 | V | Voltage ground level, Note 5 |
| | VSS3 | 0 | 0 | V | Voltage ground level, Note 6 |
| Analog Input Voltage | VAIN1 | VSS1-0.3 | VDD1+0.3 | V | Note 1, Note 7, Note 10 |
| | VAIN2 | VSS2-0.3 | VDD2+0.3 | V | Note 1, Note 8, Note 10 |
| Digital Input Voltage | VDIN | VSS3-0.3 | VDD1+0.3 | V | Note 1, Note 9, Note 10 |
| Input Current | IIN | -10 | 10 | mA | |
| Storage Temperature | Tstg | -55 | 125 | °C | |

Note 1) 0V reference for all voltages.

Note 2) Applied to [PVDD] pin.

Note 3) Applied to [CPVDD] pin

Note 4) Applied to [PVSS] pin.

Note 5) Applied to [CPVSS] pin.

Note 6) Applied to [DVSS] pin.

Note 7) Applied to [REFIN], [RFINN] and [RFINP] pins.

Note 8) Applied to [CPZ] and [SWIN] pins.

Note 9) Applied to [CLK], [DATA], [LE], [PDN1] and [PDN2] pins.

Note 10) Maximum must not be over 6.5V.

Exceeding these maximum ratings may result in damage to AK1590. Normal operation is not guaranteed at these extremes.

6. Recommended Operating Range

Table 3 Recommended Operating Range

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|-----------------------|--------|------|------|------|------|------------------------|
| Operating Temperature | Ta | -40 | | 85 | °C | |
| Supply Voltage | VDD1 | 2.7 | 3.3 | 5.5 | V | Applied to [PVDD] pin |
| | VDD2 | VDD1 | 5.0 | 5.5 | V | Applied to [CPVDD] pin |

VDD1 and VDD2 can be driven individually within the recommended operating range.

The specifications are applicable within the recommended operating range (supply voltage / operating temperature).

7. Electrical Characteristics

1. Digital DC Characteristics

Table 4 Digital DC Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit | Remarks |
|---------------------------|--------|-----------------------|----------|------|----------|------|---------|
| High level input voltage | Vih | | 0.8×VDD1 | | | V | Note 1 |
| Low level input voltage | Vil | | | | 0.2×VDD1 | V | Note 1 |
| High level input current | Iih | Vih = VDD1 = 5.5V | -1 | | 1 | μA | Note 1 |
| Low level input current | Iil | Vil = 0V, VDD1 = 5.5V | -1 | | 1 | μA | Note 1 |
| High level output voltage | Voh | Ioh = -500μA | VDD1-0.4 | | | V | Note 2 |
| Low level output voltage | Vol | Iol = 500μA | | | 0.4 | V | Note 2 |

Note 1) Applied to [CLK], [DATA], [LE], [PDN1] and [PDN2] pins.

Note 2) Applied to [LD], [GPO1] and [GPO2] pins.

2. Serial Interface Timing

<Write-In Timing>

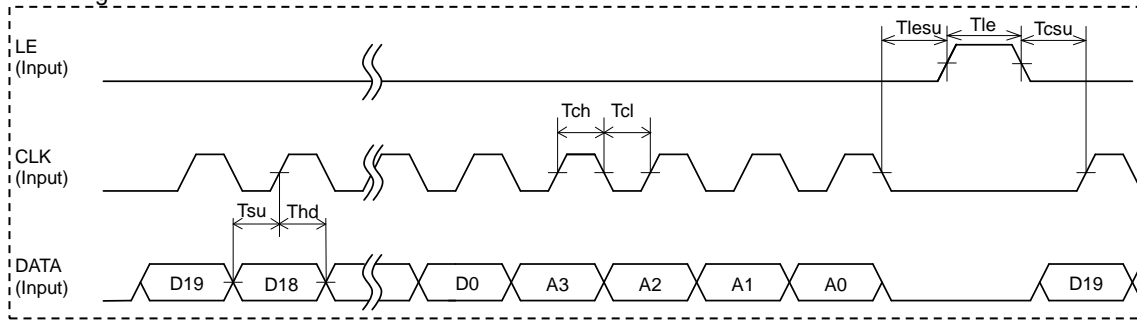


Fig. 3 Serial Interface Timing Chart

Table 5 Serial Interface Timing

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|-------------------------|--------|------|------|------|------|---------|
| Clock L level hold time | Tcl | 40 | | | ns | |
| Clock H level hold time | Tch | 40 | | | ns | |
| Clock setup time | Tcsu | 20 | | | ns | |
| Data setup time | Tsu | 20 | | | ns | |
| Data hold time | Thd | 20 | | | ns | |
| LE Setup Time | Tlesu | 20 | | | ns | |
| LE Pulse Width | Tle | 40 | | | ns | |

Note 1) While [LE] pin is setting at “Low”, 24 iteration clocks have to be set with [CLK] pin. If 25 or more clocks are set, the last 24 clocks synchronized data are valid.

Note 2) OFFSET register must be written at the lower speed than calculated frequency by “ $1/3.5 \times RF \text{ Frequency} / (INT+7)$ ”. If the writing speed is faster than this, the setting is invalid.

3. Analog Circuit Characteristics

The resistance of 27kΩ is connected to [BIAS] pin, VDD1 = 2.7V to 5.5V, VDD2 = VDD1 to 5.5V, $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$

| Parameter | Min. | Typ. | Max. | Unit | Remarks |
|--|------|-------|------|------|--|
| RF Characteristics | | | | | |
| Input Sensitivity | -10 | | +5 | dBm | |
| Input Frequency | 60 | | 500 | MHz | Prescaler 4/5 |
| | 60 | | 1000 | MHz | Prescaler 8/9,16/17 |
| REFIN Characteristics | | | | | |
| Input Sensitivity | 0.4 | | 2 | Vpp | |
| Input Frequency | 5 | | 40 | MHz | |
| Prescaler | | | | | |
| Maximum Allowable Prescaler Output Frequency | | | 125 | MHz | |
| Phase Detector | | | | | |
| Phase Detector Frequency | | | 5 | MHz | |
| Charge Pump | | | | | |
| Charge Pump 1 Maximum Current | | 168.9 | | μA | |
| Charge Pump 1 Minimum Current | | 21.1 | | μA | |
| Charge Pump 2 Maximum Current | | 2.32 | | mA | |
| Charge Pump 2 Minimum Current | | 0.84 | | mA | |
| Icp TRI-STATE Leak Current | | 1 | | nA | $0.6 \leq V_{cpo} \leq VDD2-0.7$ |
| Mismatch between Source and Sink Currents (Note 1) | | | 10 | % | $V_{cpo} = VDD2/2, T_a = 25^{\circ}\text{C}$ |
| Icp vs. Vcpo (Note 2) | | | 15 | % | $0.5 \leq V_{cpo} \leq VDD2-0.5, T_a = 25^{\circ}\text{C}$ |
| Regulator | | | | | |
| VREF Rise Time | | | 50 | μs | |
| Current Consumption | | | | | |
| IDD1 | | | 10 | μA | Power Down mode [PDN1]="Low", [PDN2]="Low" |
| IDD2 | | 2.4 | 3.6 | mA | [PDN1]="High", [PDN2]="High" IDD for [PVDD] |
| IDD3 | | 0.17 | | mA | [PDN1]="High", [PDN2]="High" IDD for [CPVDD] (Note 3) |
| IDD4 | | 0.5 | | mA | Power Save mode [PDN1]="High", [PDN2]="Low" |

Note 1) Mismatch between Source and Sink Currents: $\frac{(|I_{sink}| - |I_{source}|)}{(|I_{sink}| + |I_{source}|)/2} \times 100$ [%]

Note 2) See "Fig. 4 Charge Pump Characteristics - Voltage vs. Current": Icp vs. Vcpo:

$$\frac{\{1/2 \times (|I_1| - |I_2|)\}}{\{1/2 \times (|I_1| + |I_2|)\}} \times 100$$
 [%]

Note 3) I_{DD3} is the current that consumes constantly at [CPVDD]. This does not include the operation current in Fast Lockup mode.

Note 4) When both [PDN1] and [PDN2] are "High", the total current consumption is equivalent to " $I_{DD2}+I_{DD3}$ ".

Note 5) In the shipment test, the exposed pad on the center of the back of package is connected to ground.

Resistance Connected to BIAS Pin for Setting Charge Pump Output Current

| Parameter | Min. | Typ. | Max. | Unit | Remarks |
|-----------------|------|------|------|------------|---------|
| BIAS resistance | 22 | 27 | 33 | k Ω | |

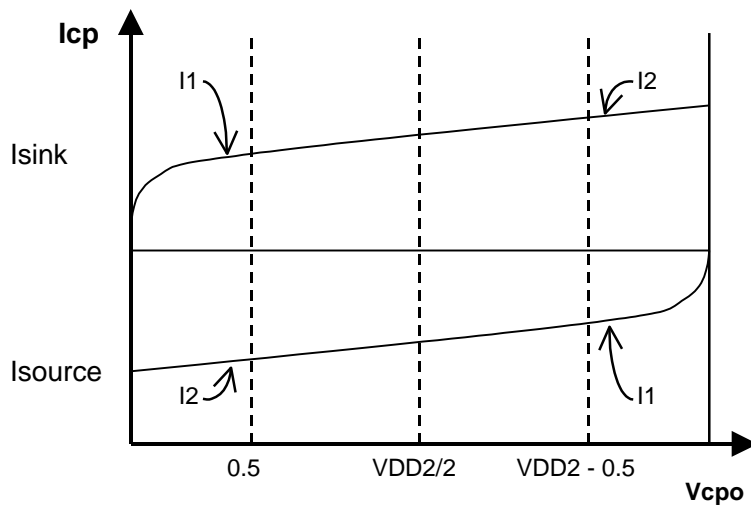


Fig. 4 Charge Pump Characteristics - Voltage vs. Current

8. Block Functional Descriptions

1. Frequency Setup

AK1590 is a Fractional-N type synthesizer that takes 2^{18} as the denominator, which calculates the integer and numerator to be set using the following formulas:

$$\begin{aligned} \text{Frequency setting} &= F_{\text{PFD}} \times (\text{Integer} + \text{Numerator} / 2^{18}) \\ \text{Integer} &= \text{ROUND} (\text{Target Frequency} / F_{\text{PFD}}) \\ \text{Numerator} &= \text{ROUND} \{(\text{Target Frequency} - \text{Integer} \times F_{\text{PFD}}) / (F_{\text{PFD}} / 2^{18})\} \end{aligned}$$

Note) ROUND: Rounded off to the nearest integer

F_{PFD} : Phase Frequency Detector comparative Frequency (= [REFIN] input frequency / R divider ratio)

- **Calculation examples**

Example 1) The numerator is positive; when the target frequency is 950.0375MHz and F_{PFD} is 1MHz.

$$\text{Integer} = 950.0375\text{MHz} / 1\text{MHz} = 950.0375$$

It is rounded off to 950 (decimal) = 3B6 (hexadecimal) = 0011 1011 0110 (binary)

$$\text{Numerator} = (950.0375\text{MHz} - 950 \times 1\text{MHz}) / (1\text{MHz} / 2^{18}) = 9830.4$$

It is rounded off to 9830 (decimal) = 2666 (hexadecimal) = 10 0110 0110 0110 (binary)

$$\text{Frequency setting} = 1\text{MHz} \times (950 + 9830 / 2^{18}) = 950.0374985\text{MHz}$$

(In this case the frequency error is 1.5Hz.)

Example 2) The numerator is negative; when the target frequency is 950.550MHz and F_{PFD} is 1MHz.

$$\text{Integer} = 950.550\text{MHz} / 1\text{MHz} = 950.550$$

It is rounded off to 951 (decimal) = 3B7 (hexadecimal) = 0011 1011 0111 (binary)

$$\text{Numerator} = (950.550\text{MHz} - 951 \times 1\text{MHz}) / (1\text{MHz} / 2^{18}) = -117964.8$$

It is rounded off to -117965 (decimal), which is reduced from 2^{18} to be converted into binary for 2's complementary expression.

$$2^{18} - 117965 \text{ (decimal)} = 144179 \text{ (decimal)} = 23333 \text{ (hexadecimal)} = 10 0011 0011 0011 0011 \text{ (binary)}$$

$$\text{Frequency setting} = 1\text{MHz} \times (951 + (-117965/2^{18})) = 950.5499992\text{MHz}$$

(In this case the frequency error is 0.8Hz.)

- **Calculation of 2's complement representation**

1) Positive number: Binary expression (Unmanipulated) exp. 100 (decimal)
64 (hexadecimal) = 110 0100 (binary)

2) Negative number: 2^{18} minus this number in binary expression exp. -100 (decimal)
 $2^{18} - 100 = 262044$ (decimal) = 3FF9C (hexadecimal) = 11 1111 1111 1001 1100 (binary)

2. Charge Pump and Loop Filter

AK1590 has two charge pumps; Charge Pump 1 for normal operation and Charge Pump 2 for Fast Lockup mode.

The internal timer is used to switch these two charge pumps to achieve a Fast Lock PLL.

The loop filter is external and connected to [CP], [SWIN] and [CPZ] pins. [CPZ] pin should be connected to R2 and C2, which are intermediate nodes, even if the Fast Lockup is not used. Therefore, R2 must be connected to [CP] pin, while C2 must be connected to the ground.

R2 and R2' are connected in parallel with internal switch in Fast Lockup. These R2 and R2' parallel resistance value is required for calculating loop bandwidth and phase margin in Fast Lockup operation.

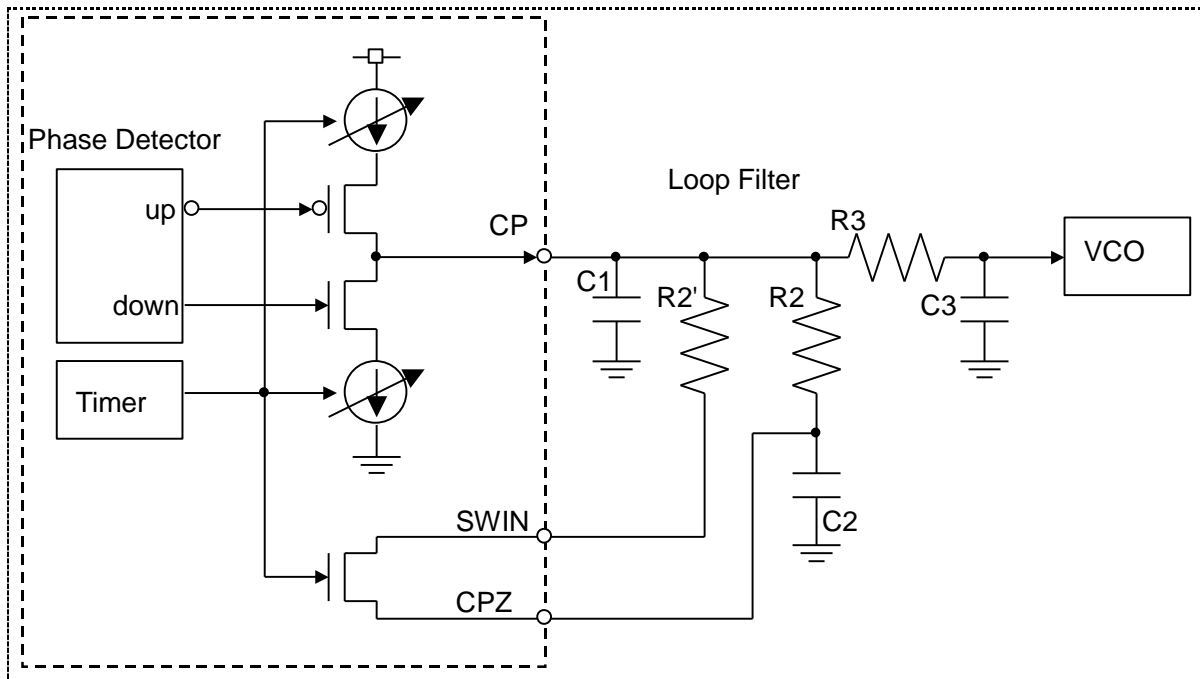


Fig. 5 Loop Filter Schematic

3. Fast Lockup Mode

Setting D[16] = {FASTEN} in <Address4> to "1" enables the Fast Lockup mode for AK1590.

Changing a frequency setting (The frequency changes at the rising edge of [LE], when <Address1> and <Address2> are accessed.) or [PDN2] pin is turned from "Low" to "High" with {FASTEN}=1 enables the Fast Lockup mode. The loop filter switch turns ON during the timer period specified by the counter value in D[12:0] = {FAST[12:0]} in <Address4>, and the charge pump for the Fast Lockup mode (Charge Pump 2) is enabled. After the timer period elapsed, the loop filter switch turns OFF. The charge pump for normal operation (Charge Pump 1) is enabled. D[12:0] = {FAST[12:0]} in <Address4> is used to set the timer period for this mode.

The following formula is used to calculate the time period:

$$\text{Phase detector frequency cycle} \times \text{counter value set in } \{ \text{FAST}[12:0] \}$$

The charge pump current can be adjusted with the register setting in 8 steps in normal operation (Charge Pump 1) and 8 steps in the Fast Lockup operation (Charge Pump 2).

The charge pump current for normal operation (Charge Pump 1) is determined by the setting in {CP1[2:0]}, which is a 3-bit address of D[17:15] in <Address2>, and a value of the resistance connected to [BIAS] pin. The following formulas show the relationship between the resistance value, the register setting and the current.

$$\text{Charge Pump 1 minimum current (CP1_min)} = 0.57 / \text{Resistance connected to [BIAS] pin}$$

$$\text{Charge Pump 1 current} = \text{CP1_min} \times (\{ \text{CP1}[2:0] \} + 1)$$

The charge pump current for the Fast Lockup mode operation (Charge Pump 2 current) is determined by the setting in {CP2[2:0]}, which is a 3-bit address of D[15:13] in <Address4>, and a value of the resistance connected to [BIAS] pin. The following formulas show the relationship between the resistance value, the register setting and the current.

$$\text{Charge Pump 2 minimum current (CP2_min)} = 5.7 / \text{Resistance connected to [BIAS] pin}$$

$$\text{Charge Pump 2 current} = \text{CP2_min} \times (\{ \text{CP2}[2:0] \} + 4)$$

The allowed range for the resistance (connected to [BIAS] pin) is from 22 to 33kΩ for both normal and Fast Lockup mode operations. For details of current settings, see "10. Register Functional Description".

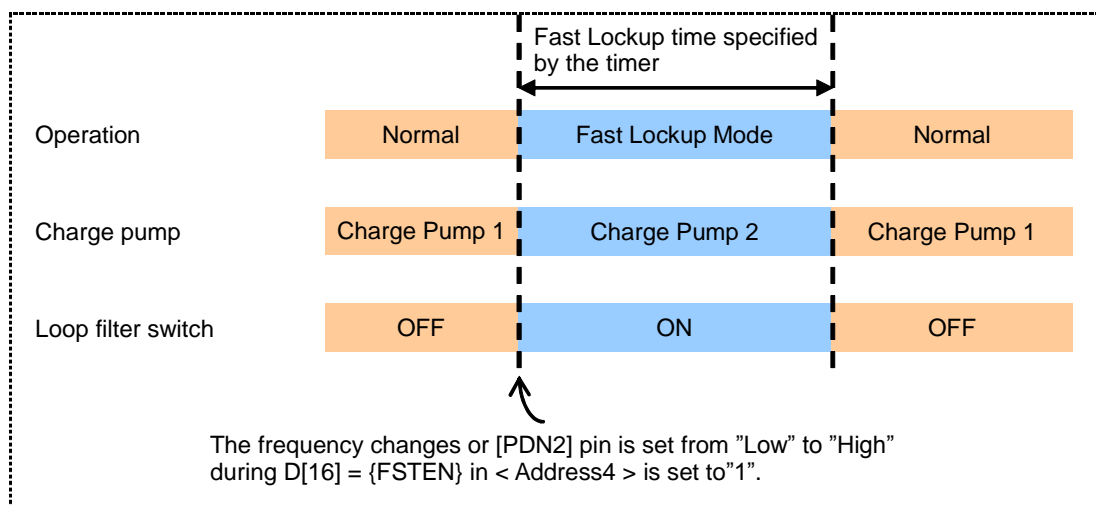


Fig. 6 Timing Chart for Fast Lockup Mode

4. Lock Detect (LD) Signal

In AK1590, "lock detect" output can be selected by $D[11] = \{LD\}$ in $\langle Address3 \rangle$. When $D[11]$ is set to "1", the phase detector output provides a phase detection status as an analog level (comparison result). This is called "Analog Lock Detect".

When $D[11]$ is set to "0", the lock detect signal outputs according to the on-chip logic. This is called "Digital Lock Detect".

4.1 Analog Lock Detect

In analog lock detect, the phase detector output comes from [LD] pin.

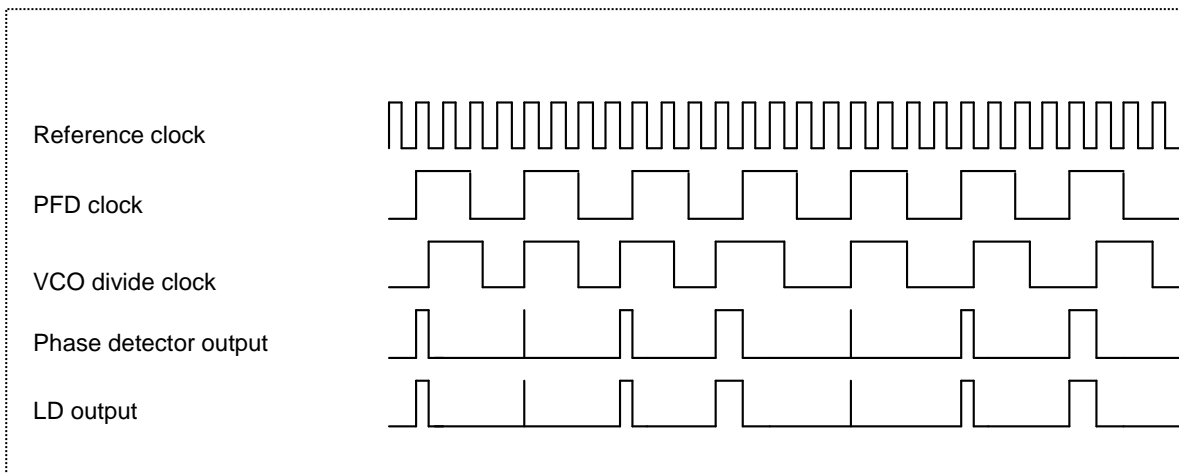


Fig. 7 Analog Lock Detect Operation

4.2 Digital Lock Detect

In digital lock detect, [LD] pin outputs "Low" when the frequency is set. The output of [LD] pin turns from "Low" to "High" (which means "locked state") when a phase error smaller than T is detected for 63 times consecutively. If the phase error that is larger than T is detected for 63 times consecutively during [LD] pin outputs "High", the output of [LD] pin turns to "Low" (which means "unlocked state").

The accuracy of the phase detect is set by {LDCKSEL[1:0]}.

{LDCKSEL[1:0]} is set to "00": T = REFIN cycle (This is not available for the reference dividing ratio ≤ 3 .)

{LDCKSEL[1:0]} is set to "01": T = REFIN cycle $\times 2$ (This is not available for the reference dividing ratio ≤ 5 .)

{LDCKSEL[1:0]} is set to "10": T = REFIN cycle $\times 3$ (This is not available for the reference dividing ratio ≤ 6 .)

Since AK1590 is a Delta-Sigma Fractional-N type, a phase error up to 7 times larger than the VCO period frequency may occur in the phase detector. Therefore {LDCKSEL[1:0]} setting should be large enough to cover the amplitude of the Delta-Sigma Fractional frequency. However, if the VCO frequency does not satisfy either of the following formula, the digital lock detect is not available. In such case, the analog lock detect should be used.

{DITH} = D[14] in <Address3> is set to "1" (DITH ON):

$$\text{VCO frequency} > [\text{REFIN}] \text{ pin input frequency} / \{ \{ \text{LDCKSEL}[1:0] \} + 1 \} \times 7$$

{DITH} = D[14] in <Address3> is set to "0" (DITH OFF):

$$\text{VCO frequency} > [\text{REFIN}] \text{ pin input frequency} / \{ \{ \text{LDCKSEL}[1:0] \} + 1 \} \times 4$$

Example 1)

When [REFIN] input frequency = 33.6MHz, {DITH} = 1, {LDCKSEL[1:0]} = "10";

$$33.6\text{MHz} / (2+1) \times 7 = 78.4\text{MHz}$$

As a result, the digital lock detect is not available if the VCO frequency is equivalent to or smaller than 78.4MHz.

Example 2)

When [REFIN] input frequency = 33.6MHz, {DITH} = 0, {LDCKSEL[1:0]} = "01";

$$33.6\text{MHz} / (1+1) \times 4 = 67.2\text{MHz}$$

As a result, the digital lock detect is not available if the VCO frequency is equivalent to or smaller than 67.2MHz.

□ Setup example

{DITH} = D[14] in <Address3> is set to "1" (DITH ON):

| | Digital Lock Detect Available | Digital Lock Detect Unavailable |
|-------------------------|--|--|
| VCO frequency | 180MHz | 70MHz |
| [REFIN] input frequency | 12.8MHz | 32MHz |
| {LDCKSEL[1:0]} | "00" | "10" |
| Calculation | $180\text{MHz} > 12.8 / (0+1) \times 7 = 89.6\text{MHz}$ | $70\text{MHz} < 32 / (2+1) \times 7 = 74.67\text{MHz}$ |

{DITH} = D[14] in <Address3> is set to "0" (DITH OFF):

| | Digital Lock Detect Available | Digital Lock Detect Unavailable |
|-------------------------|--|---|
| VCO frequency | 180MHz | 60MHz |
| [REFIN] input frequency | 12.8MHz | 32MHz |
| {LDCKSEL[1:0]} | "00" | "01" |
| Calculation | $180\text{MHz} > 12.8 / (0+1) \times 4 = 51.2\text{MHz}$ | $60\text{MHz} < 32 / (1+1) \times 4 = 64\text{MHz}$ |

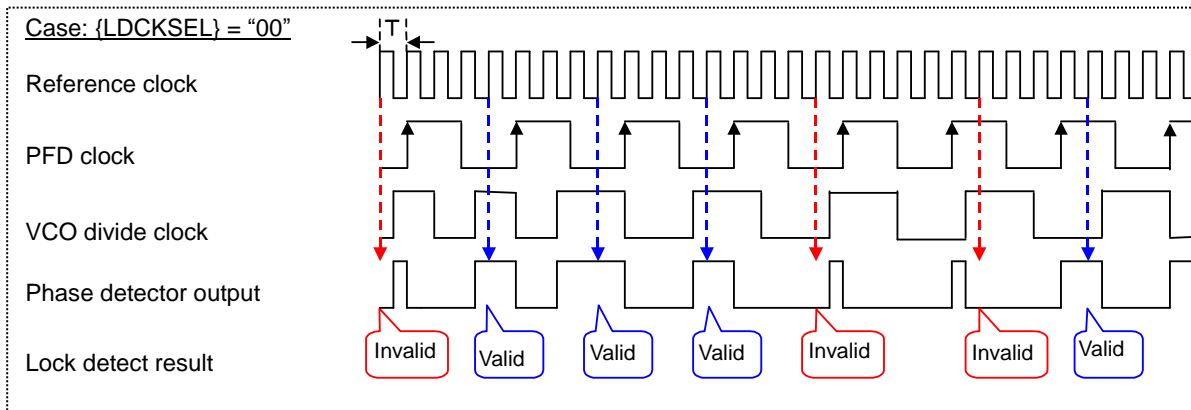


Fig. 8 Digital Lock Detect Operation

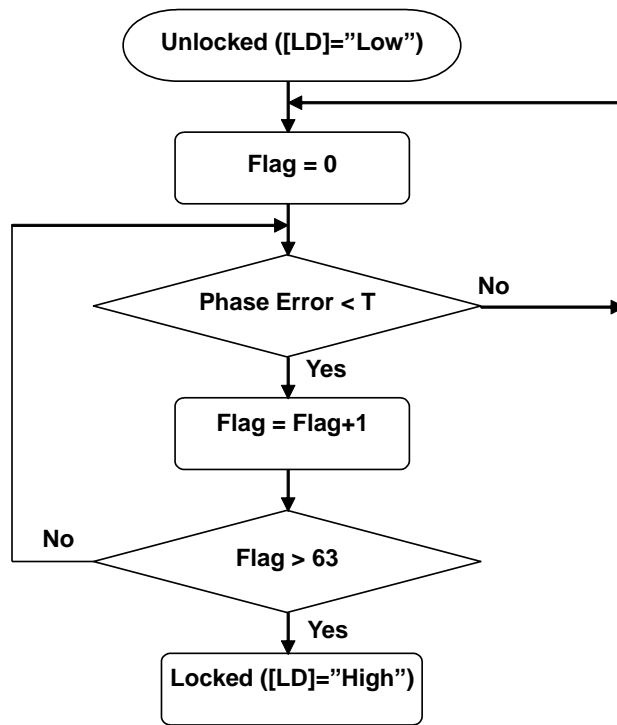


Fig. 9 Transition Flow Chart: Unlocked State to Locked State

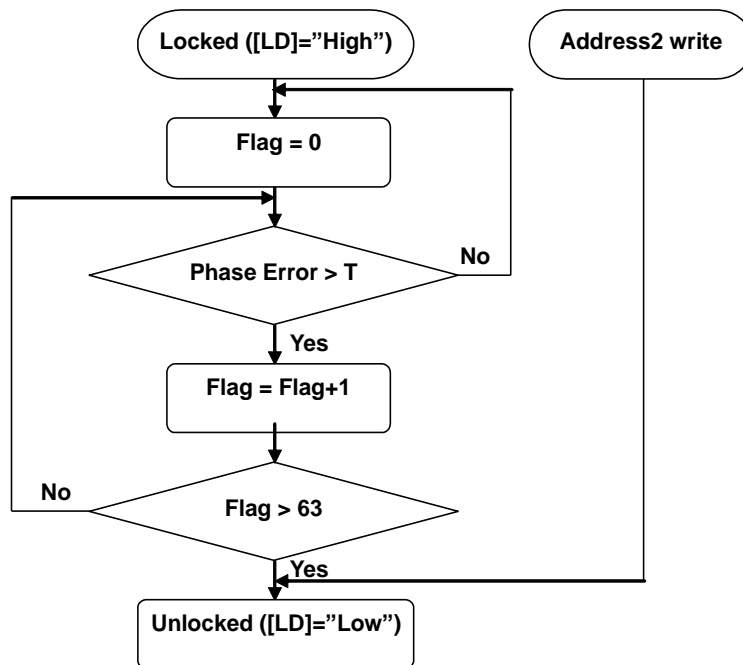


Fig. 10 Transition Flow Chart: Locked State to Unlocked State

5. Reference Input

The reference input can be set with a dividing number in the range of 4 to 255 using {R[7:0]}, which is a 8-bit address in <Address3>. A dividing number from 0 to 3 cannot be set.

6. Prescaler and Swallow Counter

The dual modulus prescaler (P/P+1) and the swallow counter are used to provide a large dividing ratio.

The prescaler is set by {PRE[1:0]}, which is a 2-bit address in <Address3>.

When {PRE[1:0]} = "00", P = 4 is selected and then an integer from 89 to 8191 can be set.

When {PRE[1:0]} = "01", P = 8 is selected and then an integer from 201 to 16383 can be set.

When {PRE[1:0]} = "10" or "11", P = 16 is selected and then an integer from 521 to 32767 can be set.

For details of how to calculate an integer, see the section "Frequency Setup" in "8. Block Functional Description".

7. Operation Mode

AK1590 can be operated in Power Down or Power Save mode as necessary by using the external control pins [PDN1] and [PDN2].

- Power On
See "13. Power-up Sequence".
- Normal Operation

| Pin name | | Mode |
|----------|--------|-------------------------------------|
| PDN1 | PDN2 | |
| "Low" | "Low" | Power Down mode |
| "Low" | "High" | Prohibited |
| "High" | "Low" | Power Save mode (Note 1 and Note 2) |
| "High" | "High" | Normal Operation mode |

Note 1) Registers setting can be acceptable after 50 μ s from [PDN1] is set to "High". The charge pump is in Hi-Z state during this period.

Note 2) Registers value are maintained when [PDN2] is set to "Low" during normal operation mode.

9. Register Map

| Name | Data | Address | | | |
|---------|-----------|---------|---|---|---|
| Num | D19 to D0 | 0 | 0 | 0 | 1 |
| Int | | 0 | 0 | 1 | 0 |
| Div | | 0 | 0 | 1 | 1 |
| Cp_fast | | 0 | 1 | 0 | 0 |
| GPO | | 0 | 1 | 0 | 1 |
| Offset | | 0 | 1 | 1 | 0 |

| Name | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Address |
|---------|-----|-----|-----------|-----------|-----------|-----------|-------------|-------------|-----------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|---------|
| Num | 0 | 0 | NUM [17] | NUM [16] | NUM [15] | NUM [14] | NUM [13] | NUM [12] | NUM [11] | NUM [10] | NUM [9] | NUM [8] | NUM [7] | NUM [6] | NUM [5] | NUM [4] | NUM [3] | NUM [2] | NUM [1] | NUM [0] | 0x01 |
| Int | 0 | 0 | CP1 [2] | CP1 [1] | CP1 [0] | INT [14] | INT [13] | INT [12] | INT [11] | INT [10] | INT [9] | INT [8] | INT [7] | INT [6] | INT [5] | INT [4] | INT [3] | INT [2] | INT [1] | INT [0] | 0x02 |
| Div | 0 | 0 | 0 | 0 | CP HiZ | DITH | LDCK SEL[1] | LDCK SEL[0] | LD | CP POLA | PRE [1] | PRE [0] | R [7] | R [6] | R [5] | R [4] | R [3] | R [2] | R [1] | R [0] | 0x03 |
| Cp_fast | 0 | 0 | 0 | FAST EN | CP2 [2] | CP2 [1] | CP2 [0] | FAST [12] | FAST [11] | FAST [10] | FAST [9] | FAST [8] | FAST [7] | FAST [6] | FAST [5] | FAST [4] | FAST [3] | FAST [2] | FAST [1] | FAST [0] | 0x04 |
| GPO | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | GPO 2 | GPO 1 | 0x05 |
| Offset | 0 | 0 | OFST [17] | OFST [16] | OFST [15] | OFST [14] | OFST [13] | OFST [12] | OFST [11] | OFST [10] | OFST [9] | OFST [8] | OFST [7] | OFST [6] | OFST [5] | OFST [4] | OFST [3] | OFST [2] | OFST [1] | OFST [0] | 0x06 |

Note 1) Writing into address 0x01 is enabled when writing into address 0x02 is performed. Be sure to write into address 0x01 first and then address 0x02.

Note 2) The initial register values are not defined just after [PDN1] releases ([PDN1] set to “High”). Therefore, even after [PDN1] is set to “High”, each bit value remains undefined. In order to set all register values, it is required to write the data in all addresses of the register.

| |
|--|
| 10. Register Functional Description |
|--|

< Address 1: Num >

| D19 | D18 | D[17:0] | Address |
|-----|-----|-----------|---------|
| 0 | 0 | NUM[17:0] | 0001 |

Note) Writing into address 0x01 is enabled when writing into address 0x02 is performed.

NUM[17:0] : Set the numerator in 2's complementary representation.

< Address 2: Int >

| D19 | D18 | D[17:15] | D[14:0] | Address |
|-----|-----|----------|-----------|---------|
| 0 | 0 | CP1[2:0] | INT[14:0] | 0010 |

CP1[2:0]: Set the current value for the charge pump in normal operation (Charge Pump 1).

Charge Pump 1 current is determined by the following formula:

$$CP1_min = 0.57 / \text{Resistance connected to [BIAS] pin}$$

$$\text{Charge Pump 1 current} = CP1_min \times ((CP1[2:0]) + 1)$$

| D[17:15] | Charge Pump 1 current [μ A] | | |
|----------|----------------------------------|--------------|--------------|
| | 22k Ω | 27k Ω | 33k Ω |
| 000 | 25.9 | 21.1 | 17.3 |
| 001 | 51.8 | 42.2 | 34.5 |
| 010 | 77.7 | 63.3 | 51.8 |
| 011 | 103.6 | 84.4 | 69.1 |
| 100 | 129.5 | 100.6 | 86.4 |
| 101 | 155.5 | 126.7 | 103.6 |
| 110 | 181.4 | 147.8 | 120.9 |
| 111 | 207.3 | 168.9 | 138.2 |

INT[14:0] : Set the integer.

When {PRE[1:0]} = "00", P = 4 is selected and then an integer from 89 to 8191 can be set.

When {PRE[1:0]} = "01", P = 8 is selected and then an integer from 201 to 16383 can be set.

When {PRE[1:0]} = "10" or "11", P = 16 is selected and then an integer from 521 to 32767 can be set.

< Address 3: Div >

| D19 | D18 | D17 | D16 | D15 | D14 | D[13:12] | D11 | D10 | D[9:8] | D[7:0] | Address |
|-----|-----|-----|-----|-------|------|--------------|-----|--------|----------|--------|---------|
| 0 | 0 | 0 | 0 | CPHIZ | DITH | LDCKSEL[1:0] | LD | CPPOLA | PRE[1:0] | R[7:0] | 0011 |

CPHIZ: Select normal or TRI-STATE for the CP1/CP2 output.

| D15 | Function | Remarks |
|-----|----------------------------|---------------------------------------|
| 0 | Charge pumps are activated | Use this setting for normal operation |
| 1 | TRI-STATE | Note 1) |

Note 1) The charge pump output is put in Hi-Z state.

DITH: Select dithering ON or OFF for a delta-sigma circuit.

| D14 | Function | Remarks |
|-----|----------|-------------------|
| 0 | DITH OFF | Low Noise mode |
| 1 | DITH ON | Low Spurious mode |

It is used to control the turning On or Off for dithering to cancel cyclical noise.

When OFFSET register is used, set DITH=0(OFF).

LDCKSEL[1:0] : Set phase error values for lock detect.

| D13 | D12 | Function | Remarks |
|-----|-----|-----------------------------|---------|
| 0 | 0 | 1 cycle of the REFIN clock | |
| 0 | 1 | 2 cycles of the REFIN clock | |
| 1 | 0 | 3 cycles of the REFIN clock | |
| 1 | 1 | Prohibited | |

For detailed functional descriptions, see the section "Lock Detect (LD) Signal" in "8. Block Functional Description".

LD: Select analog or digital for the lock detect.

| D11 | Function | Remarks |
|-----|---------------------|---------|
| 0 | Digital Lock Detect | |
| 1 | Analog Lock Detect | |

For detailed functional descriptions, see the section "Lock Detect (LD) Signal" in "8. Block Functional Description".

CPPOLA: Select positive or negative output polarity for Charge Pump 1 and Charge Pump 2.

| D10 | Function | Remarks |
|-----|----------|---------|
| 0 | Positive | |
| 1 | Negative | |

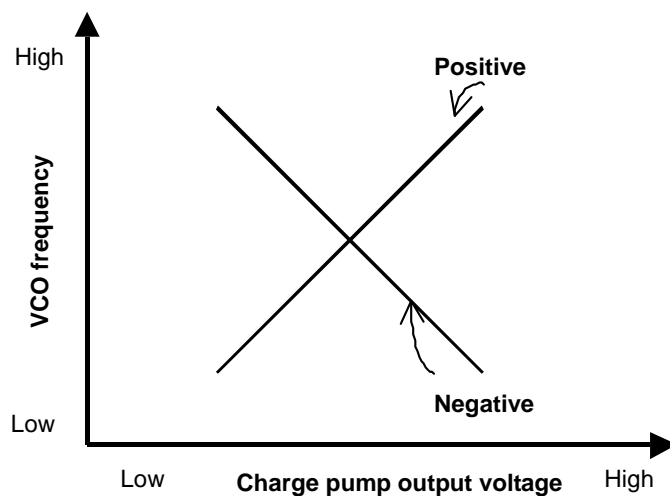


Fig. 11 Charge Pump slope Polarity

PRE[1:0] : Select a dividing ratio for the prescaler.

| D9 | D8 | Function | Remarks |
|----|----|----------|---------|
| 0 | 0 | P=4 | |
| 0 | 1 | P=8 | |
| 1 | 0 | P=16 | |
| 1 | 1 | P=16 | |

R[7:0]: Set a dividing ratio for the reference clock.

This can be set in the range from 4 (4 divisions) to 255 (255 divisions). 0 to 3 cannot be set.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Remarks |
|------|----|----|----|----|----|----|----|----------|------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Prohibited |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Prohibited |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | Prohibited |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 | Prohibited |
| DATA | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 253 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255 | |

< Address 4: Cp_fast >

| D19 | D18 | D17 | D16 | D[15:13] | D[12:0] | Address |
|-----|-----|-----|--------|----------|------------|---------|
| 0 | 0 | 0 | FASTEN | CP2[2:0] | FAST[12:0] | 0100 |

FASTEN: Enable or disables the Fast Lockup mode.

| D16 | Function | Remarks |
|-----|--|---------|
| 0 | The switchover settings specified in CP2[2:0] and FAST[12:0] are disabled. | |
| 1 | The switchover settings specified in CP2[2:0] and FAST[12:0] are enabled. | |

CP2[2:0]: Set the current value for the charge pump for the Fast Lockup mode (Charge Pump 2).

Charge Pump 2 current is determined by the following formula:

$$CP2_min = 5.7 / \text{Resistance connected to [BIAS] pin}$$

$$\text{Charge Pump 2 current} = CP2_min \times ((CP2[2:0]) + 4) \text{ [mA]}$$

| D[15:13] | Charge Pump 2 current [mA] | | |
|----------|----------------------------|------|------|
| | 22kΩ | 27kΩ | 33kΩ |
| 000 | 1.04 | 0.84 | 0.69 |
| 001 | 1.30 | 1.06 | 0.86 |
| 010 | 1.55 | 1.27 | 1.04 |
| 011 | 1.81 | 1.48 | 1.21 |
| 100 | 2.07 | 1.69 | 1.38 |
| 101 | 2.33 | 1.90 | 1.55 |
| 110 | 2.59 | 2.11 | 1.73 |
| 111 | 2.85 | 2.32 | 1.90 |

FAST[12:0] : Set the FAST counter value.

A decimal number from 1 to 8191 can be set. This counter value is used to set the time period during which the charge pump for the Fast Lockup mode is ON.

The charge pump for the Fast Lockup mode is turned OFF after the time period calculated by “this count value × the reference clock cycle”. 0 cannot be set.

| D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Function | Remarks |
|------|-----|-----|----|----|----|----|----|----|----|----|----|----|----------|------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Prohibited |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | |
| DATA | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 8189 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8190 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8191 | |

< Address 5: GPO >

| D[19:2] | D1 | D0 | Address |
|---------|------|------|---------|
| 0 | GPO2 | GPO1 | 0101 |

GPO2: Set the state of [GPO2] pin

This value controls the General-Purpose Output pin GPO2.

The voltage applied to PVDD pin determines the “High” output level.

| D1 | Function | Remarks |
|----|---------------------------------|---------|
| 0 | “Low” output from the GPO2 pin | |
| 1 | “High” output from the GPO2 pin | |

GPO1: Set the state of [GPO1] pin

This value controls the General-Purpose Output pin GPO1.

The voltage applied to the PVDD pin determines the “High” output level.

| D0 | Function | Remarks |
|----|---------------------------------|---------|
| 0 | “Low” output from the GPO1 pin | |
| 1 | “High” output from the GPO1 pin | |

< Address 6: Offset >

| D19 | D18 | D[17:0] | Address |
|-----|-----|------------|---------|
| 0 | 0 | OFST[17:0] | 0110 |

OFST[17:0] : Set the adjustable frequency offset in 2’s complementary representation.

This register designates offset from carrier frequency.

After this register is accessed, {NUM[17:0]} is recalculated and {NUM[17:0]}+{OFST[17:0]} are used in delta-sigma and N-divider as the numerator. When this register is not used, this register must be written 00000 (hexadecimal).

When this register is used continuously as below,

$$\{OFST\}(0) \rightarrow \{OFST\}(1) \rightarrow \dots \rightarrow \{OFST\}(k-1) \rightarrow \{OFST\}(k) \rightarrow \{OFST\}(k+1) \rightarrow \dots$$

{NUM} and {OFST} can be set in the below range.

$$-131072 \leq \{NUM\} + \{OFST\} \leq 131071 \text{ (decimal)}$$

$$|\{OFST\}(k) - \{OFST\}(k-1)| \leq 2000 \text{ (decimal)}$$

When this register is used in out of this range, the circuit of delta-sigma modulator may cause unexpected glitches in VCO control voltage.

When OFFSET register is used, set DITH=0(OFF).

OFFSET register must be written at the lower speed than calculated frequency by "1/3.5×RF Frequency/(INT+7)". If the writing speed is faster than this, the setting is invalid.

- **Setting examples**

Example 1) The frequency offset is positive; when the frequency offset is 100Hz and F_{PFD} is 1MHz.

$$\text{Frequency offset} = 100\text{Hz} / (1\text{MHz}/2^{18}) = 26.2$$

It is round off to 26 (decimal) = 1A (hexadecimal) = 11010 (binary)

Example 2) The frequency offset is negative; when the frequency offset is -100Hz and F_{PFD} is 1MHz.

$$\text{Frequency offset} = -100\text{Hz} / (1\text{MHz}/2^{18}) = -26.2$$

It is round off to -26 (decimal), which is reduced from 2^{18} to be converted into binary for 2's complementary expression.

$$2^{18} - 26 = 262118 \text{ (decimal)} = 3FFE6 \text{ (hexadecimal)} = 11\ 1111\ 1111\ 1110\ 0110 \text{ (binary)}$$

Example 3) Calculation example : $\{ \text{NUM} \} + \{ \text{OFST} \}$

When the frequency offset is 1500Hz, F_{PFD} is 4.8MHz, and VCO frequency is 467.52MHz.

$$\text{Integer} = 467.52\text{MHz} / 4.8\text{MHz} = 97.4$$

It is rounded off to 97 (decimal) = 61 (hexadecimal) = 110 0001 (binary)

$$\text{Numerator} = (467.52\text{MHz} - 97 \times 4.8\text{MHz}) / (4.8\text{MHz} / 2^{18}) = 104857.6$$

It is rounded off to 104858 (decimal) = 1999A (hexadecimal) = 1 1001 1001 1010 (binary)

$$\text{Frequency offset} = 1500\text{Hz} / (4.8\text{MHz}/2^{18}) = 81.92$$

It is round off to 82 (decimal) = 52 (hexadecimal) = 101 0010 (binary)

In this case, $\{ \text{NUM} \} + \{ \text{OFST} \} = 104858 + 82 = 104940$ (decimal)

Example 4) Calculation example : $\{ \text{OFST} \}(k) - \{ \text{OFST} \}(k-1)$

When F_{PFD} is 1MHz. The frequency offset is set to 2000Hz at the 1st time. Then the frequency offset is set to -2000Hz at the 2nd time.

$$\text{Frequency offset(1st time)} = 2000\text{Hz} / (1\text{MHz}/2^{18}) = 524.288$$

It is round off to 524 (decimal) = 20C (hexadecimal) = 10 0000 1100 (binary)

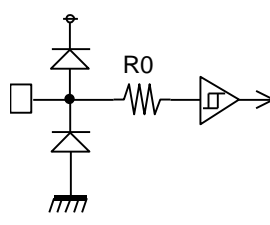
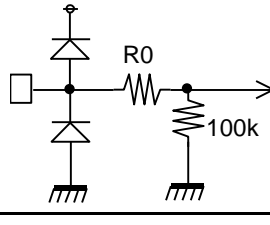
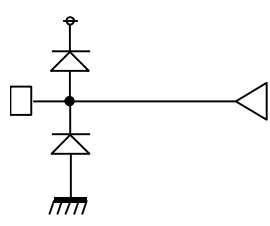
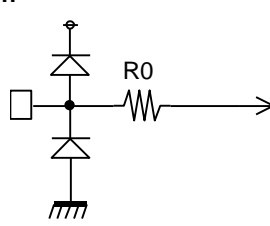
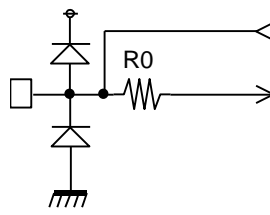
$$\text{Frequency offset(2nd time)} = -2000\text{Hz} / (1\text{MHz}/2^{18}) = -524.288$$

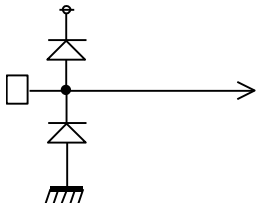
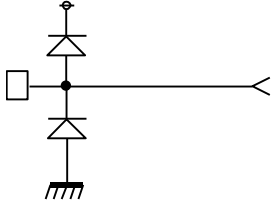
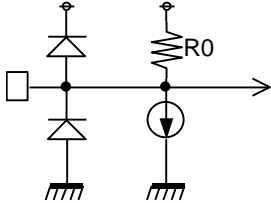
It is round off to -524 (decimal), which is reduced from 2^{18} to be converted into binary for 2's complementary expression.

$$2^{18} - 524 = 261620 \text{ (decimal)} = 3FDF4 \text{ (hexadecimal)} = 11\ 1111\ 1101\ 1111\ 0100 \text{ (binary)}$$

In this case, $\{ \text{OFST} \}(k) - \{ \text{OFST} \}(k-1) = -524 - 524 = -1048$ (decimal)

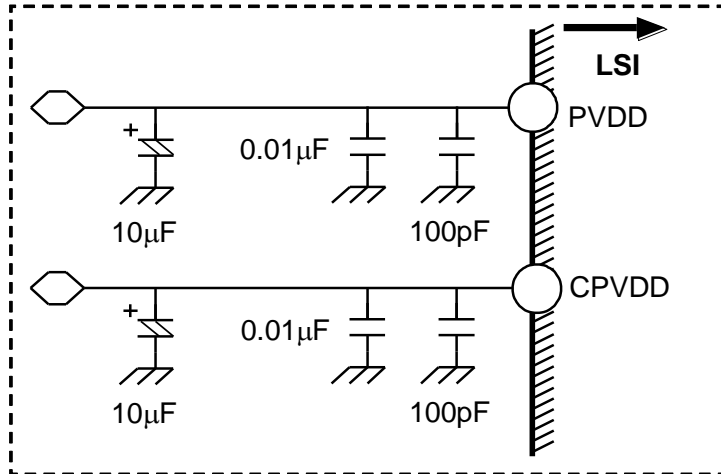
11. IC Interface Schematic

| No. | Name | I/O | R0(Ω) | Cur(μ A) | Function |
|-----|-------|-----|----------------|---------------|---|
| 4 | LE | I | 300 | | Digital input pins  |
| 5 | DATA | I | 300 | | |
| 6 | CLK | I | 300 | | |
| 8 | PDN2 | I | 300 | | |
| 9 | PDN1 | I | 300 | | |
| 2 | TEST3 | I | 300 | | Digital input pins Pull-Down  |
| 3 | TEST1 | I | 300 | | |
| 11 | TEST2 | I | 300 | | |
| 7 | LD | O | | | Digital output pin  |
| 12 | GPO1 | O | | | |
| 13 | GPO2 | O | | | |
| 10 | REFIN | I | 300 | | Analog input pin  |
| 15 | VREF | IO | 300 | | Analog I/O pin  |
| 19 | BIAS | IO | 300 | | |
| 22 | CPZ | IO | 300 | | |

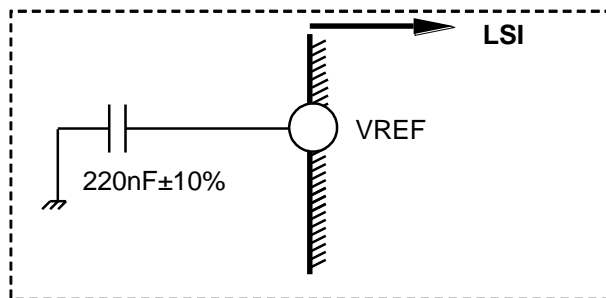
| No. | Name | I/O | R0(Ω) | Cur(μ A) | Function |
|-----|-------|-----|----------------|---------------|--|
| 23 | SWIN | I | | | Analog input pin  |
| 21 | CP | O | | | Analog output pin  |
| 16 | RFINN | I | 40k | 20 | Analog input pin (RF signal input)  |
| 17 | RFINP | I | 40k | 20 | |

12. Recommended Connection Schematic for Off-Chip Components

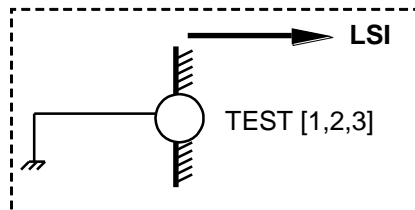
1. PVDD, CPVDD



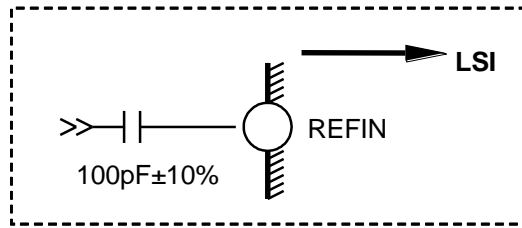
2. VREF



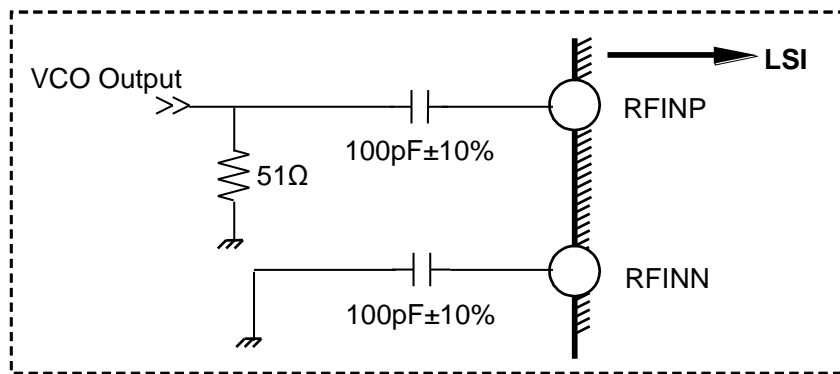
3. TEST [1,2,3]



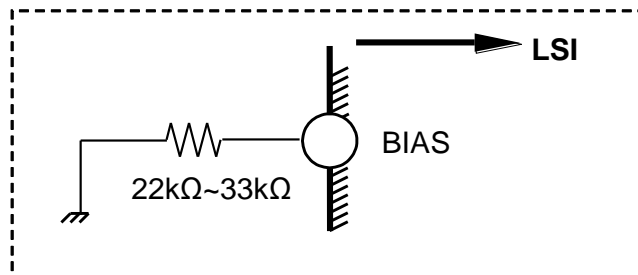
4. REFIN



5. RFINP, RFINN



6. BIAS



13. Power-up Sequence

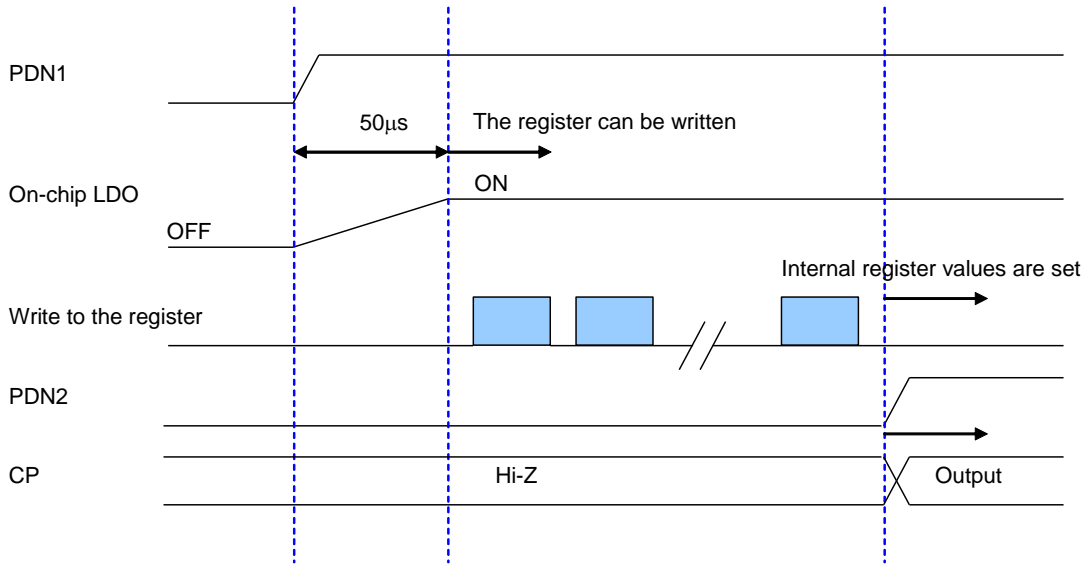


Fig. 12 Recommended Power-up Sequence

- Note 1) The initial register values are not defined. Therefore, even after [PDN1] is set to "High", each bit value remains undefined. In order to set all register values, it is required to write the data in all addresses of the register.
- Note 2) It is prohibited to do power up and [PDN2] release at the same time. It is mandatory to power up first, then set [PDN2] to "High". If they are set simultaneously, initial operation might be unstable.

14. Typical Evaluation Board Schematic

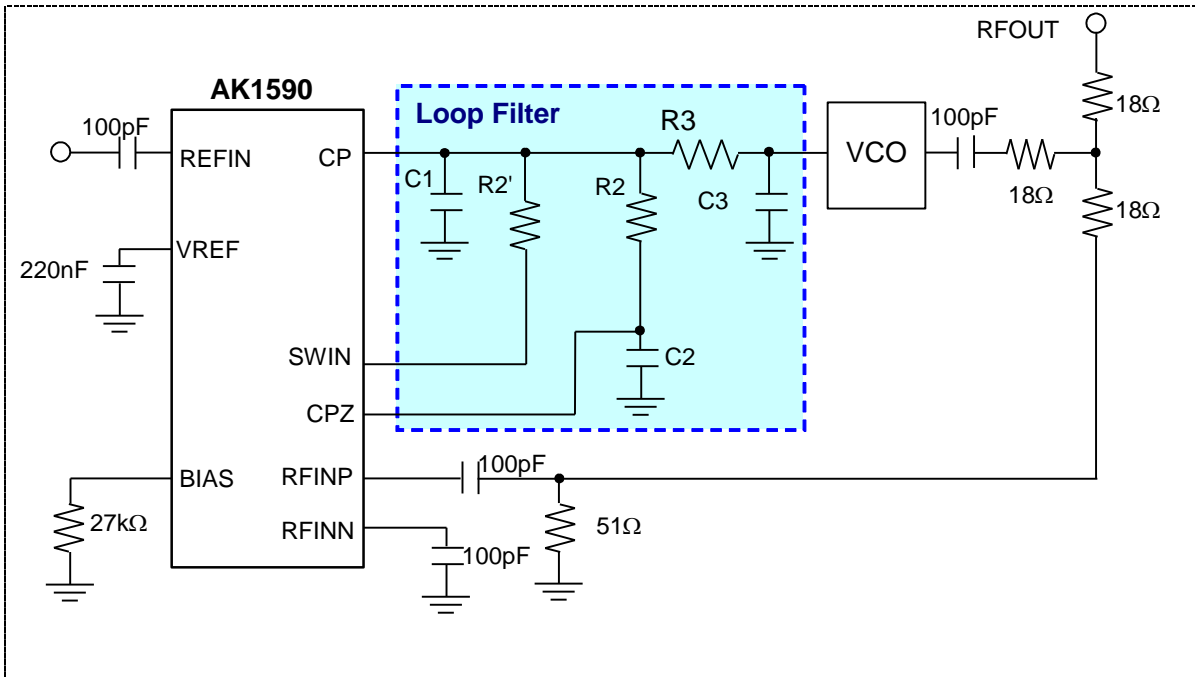


Fig. 13 Typical Evaluation Board Schematic

The input voltage from [CPZ] pin is used in the internal circuit. [CPZ] pin must not be open even when the Fast Lockup feature is unused. For the output destination from [CPZ] pin, see “Fig.5 Loop Filter Schematic”. [SWIN] pin could be open when the Fast Lockup feature is not used.

R2 and R2' are connected in parallel with internal switch in Fast Lockup. These R2 and R2' parallel resistance value is required for calculating loop bandwidth and phase margin in Fast Lockup. The on-resistance value of the internal switch is 150Ω for reference.

It is recommended to connect the exposed pad (the center of the back of the package) to ground, although it will not make any impact on the electrical characteristics even if the pad is open. Moreover, all test pins should be connected to ground.

15. Block Diagram by Power Supply

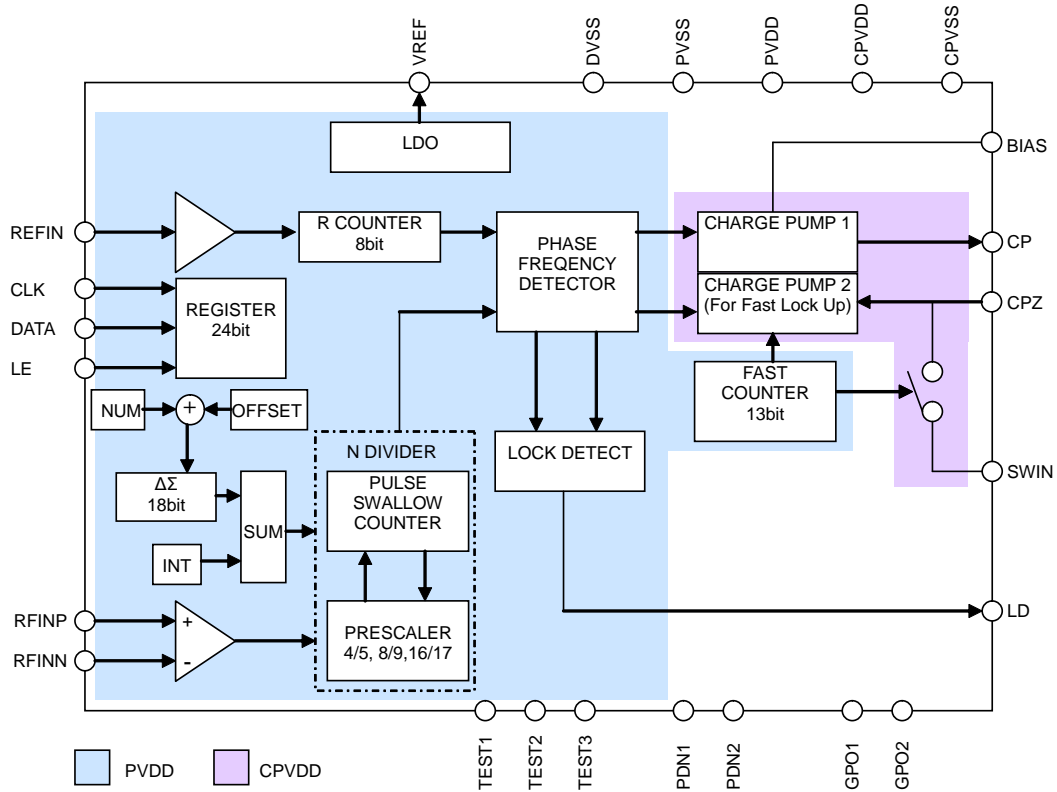
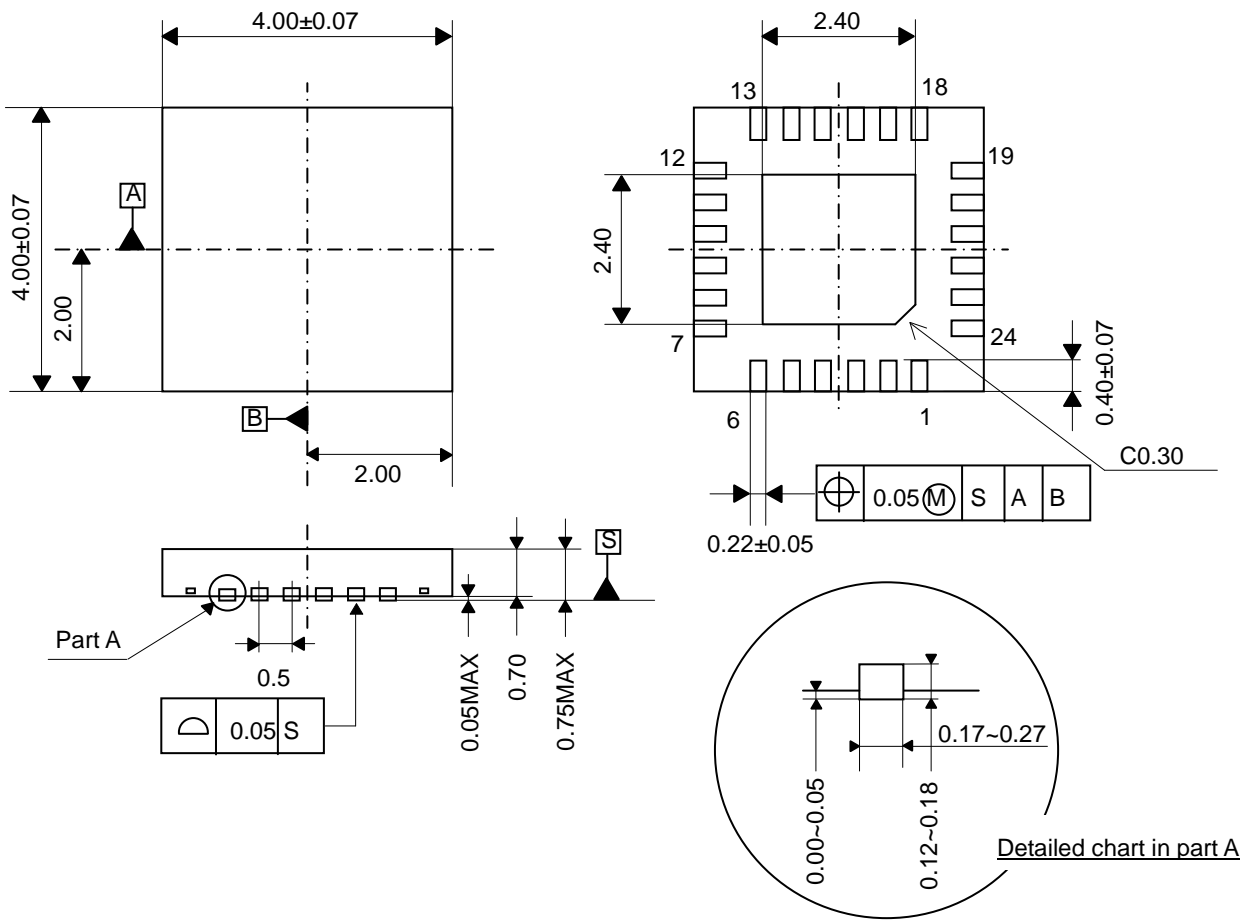


Fig. 14 Block Diagram by Power Supply

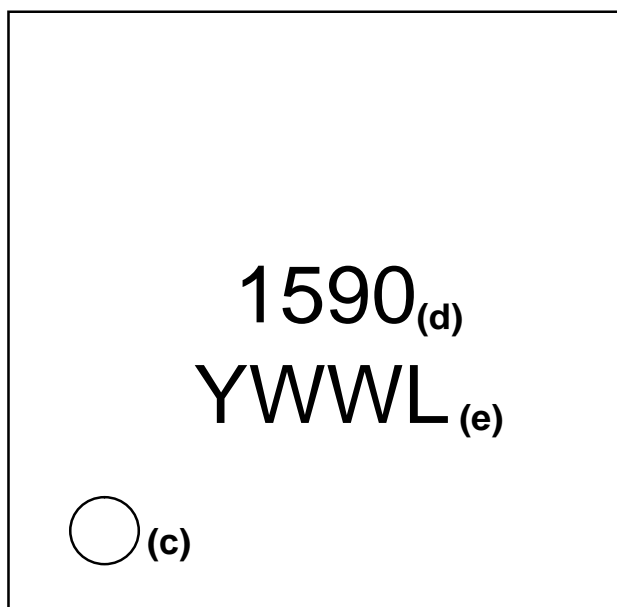
16. Outer Dimensions



Note) It is recommended to connect the exposed pad (the center of the back of the package) to ground, although it will not make any impact on the electrical characteristics even if the pad is open.

17. Marking

- (a) Style : QFN
(b) Number of pins : 24
(c) 1 pin marking: : ○
(d) Product number : 1590
(e) Date code : YWWL (4 digits)
Y: Lower 1 digit of calendar year (Year 2012 → 2, 2013 → 3 ...)
WW: Week
L: Lot identification, given to each product lot which is made in a week
→ LOT ID is given in alphabetical order (A, B, C...).

**Fig. 16 Marking**

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●**Related Parts**

| Part# | Discription | Comments |
|---|---|---------------------------------------|
| Mixer | | |
| AK1220 | 100MHz~900MHz High Linearity Down Conversion Mixer | IIP3:+22dBm |
| AK1222 | 100MHz~900MHz Low Power Down Conversion Mixer | IDD:2.9mA |
| AK1224 | 100MHz~900MHz Low Noise, High Liniarity Down Conversion Mixer | NF:8.5dB, IIP3:+18dBm |
| AK1228 | 10MHz~2GHz Up/Down Conversion Mixer | 3V Supply, NF:8.5dB |
| AK1221 | 0.7GHz~3.5GHz High Linearity Down Conversion Mixer | IIP3:+25dBm |
| AK1223 | 3GHz~8.5GHz High Linearity Down Conversion Mixer | IIP3:+13dB, NF:15dB |
| PLL Synthesizer | | |
| AK1541 | 20MHz~600MHz Low Power Fractional-N Synthesizer | IDD:4.6mA |
| AK1542A | 20MHz~600MHz Low Power Integer-N Synthesizer | IDD:2.2mA |
| AK1543 | 400MHz~1.3GHz Low Power Fractional-N Synthesizer | IDD:5.1mA |
| AK1544 | 400MHz~1.3GHz Low Power Integer-N Synthesizer | IDD:2.8mA |
| AK1590 | 60MHz~1GHz Fractional-N Synthesizer | IDD:2.5mA |
| AK1545 | 0.5GHz~3.5GHz Integer-N Synthesizer | 16-TSSOP |
| AK1546 | 0.5GHz~3GHz Low Phase Noise Integer-N Synthesizer | Normalized C/N:-226dBc/Hz |
| AK1547 | 0.5GHz~4GHz Integer-N Synthesizer | 5V Supply |
| AK1548 | 1GHz~8GHz Low Phase Noise Integer-N Synthesizer | Normalized C/N:-226dBc/Hz |
| IFVGA | | |
| AK1291 | 100~300MHz Analog Signal Control IF VGA w/ RSSI | Dynamic Range:30dB |
| integrated VCO | | |
| AK1572 | 690MHz~4GHz Down Conversion Mixer with Frac.-N PLL and VCO | IIP3:24dBm, -111dBc/Hz@100kHz |
| AK1575 | 690MHz~4GHz Up Conversion Mixer with Frac.-N PLL and VCO | IIP3:24dBm, -111dBc/Hz@100kHz |
| IF Reciever (2nd Mixer + IF BPF + FM Detector) | | |
| AK2364 | Built-in programmable AGC+BPF, FM detector IC | IFBPF:±10kHz ~ ±4.5kHz |
| AK2365A | Built-in programmable AGC+BPF, IFIC | IFBPF:±7.5kHz ~ ±2kHz |
| Analog BB for PMR/LMR | | |
| AK2345C | CTCSS Filter, Encoder, Decoder | 24-VSOP |
| AK2360/ AK2360A | Inverted frequency(3.376kHz/3.020kHz) scrambler | 8-SON |
| AK2363 | MSK Modem/DTMF Receiver | 24-QFN |
| AK2346B | 0.3-2.55/3.0kHz Analog audio filter, | 24-VSOP |
| AK2346A | Emphasis, Compandor, scrambler, MSK Modem | 24-QFN |
| AK2347B | 0.3-2.55/3.0kHz Analog audio filter Emphasis, Compandor, scrambler, CTCSS filter | 24-VSOP |
| Function IC | | |
| AK2330 | 8-bit 8ch Electronic Volume | VREF can be selected for each channel |
| AK2331 | 8-bit 4ch Electronic Volume | VREF can be selected for each channel |

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