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FUJITSU MICROELECTRONICS
DATA SHEET

DS07-16912-1E

32-bit Microcontrollers

CMOS

FR60 MB91490 Series

MB91F492 / FV470

■ DESCRIPTION

The MB91490 series is Fujitsu's general-purpose 32-bit RISC microcontroller, which is designed for embedded control applications that require high-speed processing performance.
This series uses the FR60 CPU, which is compatible with the FR* family of CPUs.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of Fujitsu Microelectronics Limited.

■ FEATURES

- FR60 CPU
  - 32-bit RISC, load/store architecture, five-stage pipeline
  - Operating frequency of 80 MHz (PLL clock multiplied)
  - 16-bit fixed-length instructions (basic instructions)
  - Instruction execution speed : one instruction per cycle
  - Memory-to-memory transfer, bit processing, barrel shift instructions, etc. : instructions suitable for embedded applications
  - Function entry and exit instructions, multi load/store instructions of register contents : instructions compatible with C language.
  - Register interlock function to facilitate assembly-language coding
  - Built-in multiplier/instruction-level support
    - Signed 32-bit multiplication : 5 cycles
    - Signed 16-bit multiplication : 3 cycles
  - Interrupts (save PC and PS) : 6 cycles, 16 priority levels
  - Harvard architecture allowing program access and data access to be executed simultaneously
  - Instructions compatible with the FR family

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For the information for microcontroller supports, see the following web site.

http://edevice.fujitsu.com/micom/en-support/

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(Continued)

- Built-in Peripheral functions
  - I/O ports
  - NMI (Non Maskable Interrupt)
  - External interrupts
  - Bit search module (for REALOS)
    Function to search for the position of the first bit that has changed from 1 to 0 in a word starting from the MSB
  - 16-bit reload timers
  - Timing generator
  - 8/16-bit PPG timers
  - Multi-function timer
    - 16-bit free-run timer
    - Input capture (Linked to free-run timer)
    - Output compare (Linked to free-run timer)
    - A/D start up compare (Linked to free-run timer)
    - Wave form generator
      Various wave forms are generated by using output compare output, 16-bit PPG timer and 16-bit dead timer.
  - Base timer
    Only one timer function can be selected from the 16-bit PWM timer, 16-bit PPG timer, 16/32-bit reload timer, and 16/32-bit PWC timer.
  - 8/16-bit up/down counter
  - Multi-function serial interface
    - Full-duplex double buffer
    - Asynchronous (start-stop synchronization) communication, clock synchronous communication, I^2C standard mode (Max 100 kbps), I^2C high-speed mode (selectable various modes at maximum of 400 kbps)
    - Selectable parity On/Off
    - Each channel has built-in baud rate generator
    - Error detection function for parity, frame and overrun errors
    - External clock can be used as transfer clock
    - With I^2C function
  - 8/10-bit A/D Converter (Successive comparison type)
    - Resolution : 8-bit or 10-bit resolution selectable
    - Conversion time : 1.2 µs (minimum conversion time for 33 MHz peripheral clock (CLKP))
      1.2 µs (minimum conversion time for 40 MHz peripheral clock (CLKP))
  - DMAC (DMA Controller)
    - Transfers can be started by software or by interrupts from the built-in peripherals
  - Wild register
    - Instructions or data located at a target address can be replaced (in the built-in Flash area only)
  - Low voltage detection interrupt / reset
    - Detects low voltage (3.7 V ± 0.3 V) and generate external interrupt
    - Detects low voltage (3.0 V ± 0.24 V) and generate system initialization reset
  - Flash memory security function
    - Protects the content of Flash memory

- Other Features
  - Watchdog timer
  - Low-power consumption modes
    - Sleep/stop function
  - CMOS technologies : 0.18 µm
  - Power supply : Single power supply (V_{CC} = 2.7 V to 5.5 V)

■ PRODUCT LINEUP

Characteristics	Common EVA of the series	MB91490 series
	MB91FV470	MB91F492
Built-in Flash capacity	512 Kbytes (Flash)	256 Kbytes (Flash)
Flash security	—	○
Built-in RAM capacity	40 Kbytes	12 Kbytes
I/O ports	160	49
External interrupts	NMI 16 channels	NMI 7 channels
Reload timer	2 channels	2 channels
Timing generator	2 units	1 unit
PPG	8-bit × 16 channels 16-bit × 8 channels	8-bit × 8 channels 16-bit × 4 channels (PPG output: 3 channels)
Multi-function timer	2 units	1 unit
Free-run timer	6 channels	3 channels
OCU	12 channels	6 channels
ICU	8 channels	4 channels
A/D activating compare	6 channels	2 channels
Wave form generator	12 channels	6 channels
Base timer	6 channels	2 channels
Up/down counter	2 channels	1 channel
Multi-function serial interface	6 units (w FIFO)	3 units (w/o FIFO)
8/10-bit A/D converter	4 channels × 2 units 16 channels × 1 unit	4 channels × 1 unit 8 channels × 1 unit
Low voltage detection interrupt	—	1 channel
Low voltage detection reset	—	1 channel
DMAC	5 channels	5 channels
Wild register	16 channels	16 channels
Debug function	DSU4	—

○ : Supported

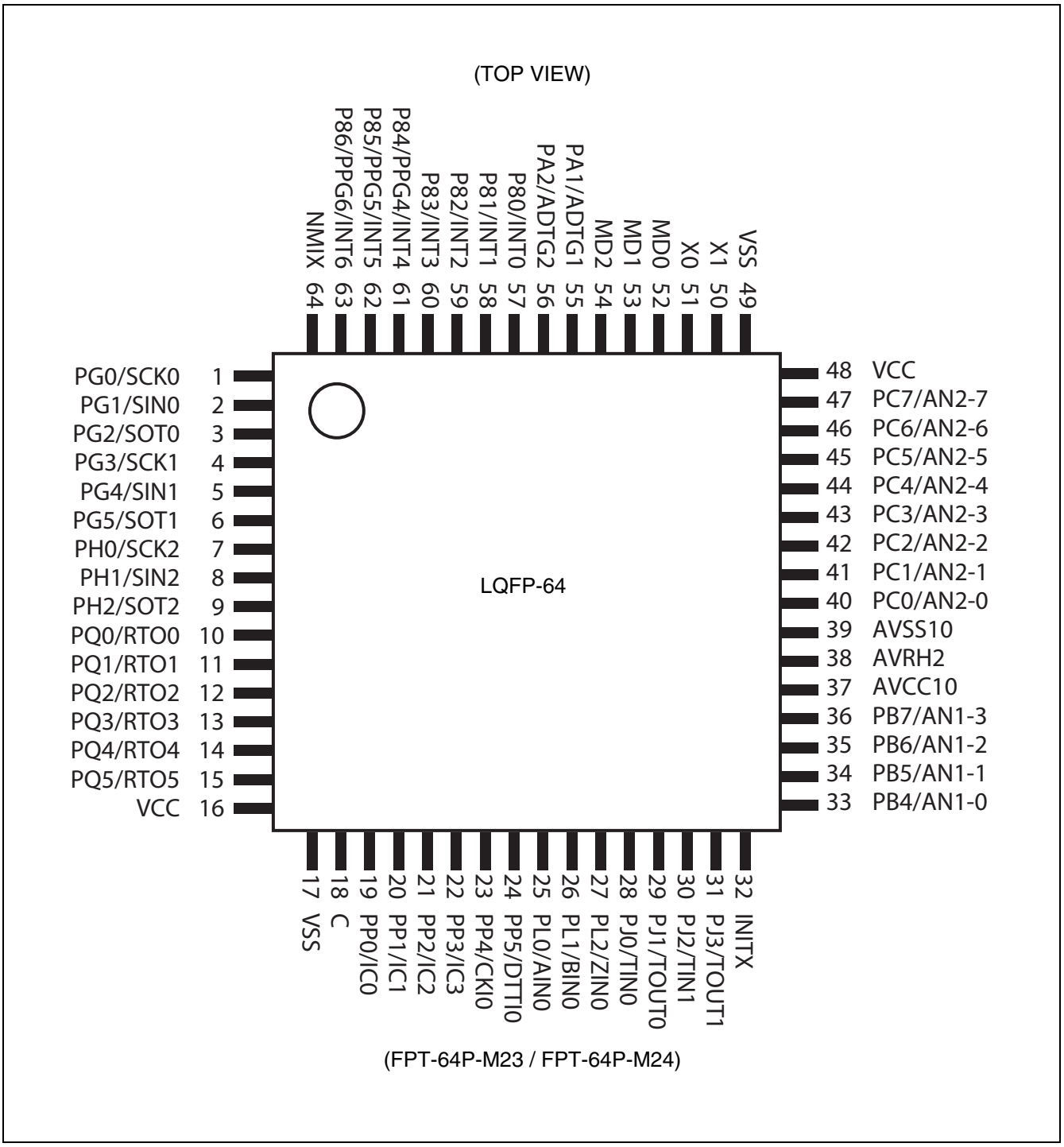
■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB91F492
FPT-64P-M23 (LQFP-0.65 mm)	○
FPT-64P-M24 (LQFP-0.50 mm)	○

○ : Supported

Note : For details of each package, refer to “■ PACKAGE DIMENSIONS”.

■ PIN ASSIGNMENT



(FPT-64P-M23 / FPT-64P-M24)

■ PIN DESCRIPTION

Pin no.	Pin name	I/O circuit type*	Function
54	MD2	K	Mode pin 2 This pin sets the basic operating mode. During normal communication, input must be at the “L” level. During serial programming to flash memory, input must be at the “H” level.
53	MD1	K	Mode pin 1 This pin sets the basic operating mode. Input must always be at the “L” level.
52	MD0	K	Mode pin 0 This pin sets the basic operating mode. Input must always be at the “L” level.
51	X0	A	Clock (oscillation) input
50	X1	A	Clock (oscillation) output
32	INITX	I	External reset input
64	NMIX	H	NMI (Non Maskable Interrupt) input
57	INT0	D	External interrupt 0 input
	P80		General-purpose I/O port
58	INT1	D	External interrupt 1 input
	P81		General-purpose I/O port
59	INT2	D	External interrupt 2 input
	P82		General-purpose I/O port
60	INT3	D	External interrupt 3 input
	P83		General-purpose I/O port
61	INT4	D	External interrupt 4 input
	PPG4		Output of PPG timer 4
	P84		General-purpose I/O port
62	INT5	D	External interrupt 5 input
	PPG5		Output of PPG timer 5
	P85		General-purpose I/O port
63	INT6	D	External interrupt 6 input
	PPG6		Output of PPG timer 6
	P86		General-purpose I/O port
55	ADTG1	D	External trigger input of 8/10-bit A/D converter 1
	PA1		General-purpose I/O port
56	ADTG2	D	External trigger input of 8/10-bit A/D converter 2
	PA2		General-purpose I/O port

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
33	AN1-0	G	Analog 0 input of 8/10-bit A/D converter 1
	PB4		General-purpose I/O port
34	AN1-1	G	Analog 1 input of 8/10-bit A/D converter 1
	PB5		General-purpose I/O port
35	AN1-2	G	Analog 2 input of 8/10-bit A/D converter 1
	PB6		General-purpose I/O port
36	AN1-3	G	Analog 3 input of 8/10-bit A/D converter 1
	PB7		General-purpose I/O port
40	AN2-0	G	Analog 0 input of 8/10-bit A/D converter 2
	PC0		General-purpose I/O port
41	AN2-1	G	Analog 1 input of 8/10-bit A/D converter 2
	PC1		General-purpose I/O port
42	AN2-2	G	Analog 2 input of 8/10-bit A/D converter 2
	PC2		General-purpose I/O port
43	AN2-3	G	Analog 3 input of 8/10-bit A/D converter 2
	PC3		General-purpose I/O port
44	AN2-4	G	Analog 4 input of 8/10-bit A/D converter 2
	PC4		General-purpose I/O port
45	AN2-5	G	Analog 5 input of 8/10-bit A/D converter 2
	PC5		General-purpose I/O port
46	AN2-6	G	Analog 6 input of 8/10-bit A/D converter 2
	PC6		General-purpose I/O port
47	AN2-7	G	Analog 7 input of 8/10-bit A/D converter 2
	PC7		General-purpose I/O port
1	SCK0 (SCL0)	D	Clock I/O of multi-function serial interface 0 (used in I^2C mode, SCL0)
	PG0		General-purpose I/O port
2	SIN0	D	Data input of multi-function serial interface 0 (not used in I^2C mode)
	PG1		General-purpose I/O port
3	SOT0 (SDA0)	D	Data output of multi-function serial interface 0 (used in I^2C mode, SDA0)
	PG2		General-purpose I/O port

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
4	SCK1 (SCL1)	D	Clock I/O of multi-function serial interface 1 (used in I²C mode, SCL1)
	PG3		General-purpose I/O port
5	SIN1	D	Data input of multi-function serial interface 1 (not used in I²C mode)
	PG4		General-purpose I/O port
6	SOT1 (SDA1)	D	Data output of multi-function serial interface 1 (used in I²C mode, SDA1)
	PG5		General-purpose I/O port
7	SCK2 (SCL2)	D	Clock I/O of multi-function serial interface 2 (used in I²C mode, SCL2)
	PH0		General-purpose I/O port
8	SIN2	D	Data input of multi-function serial interface 2 (not used in I²C mode)
	PH1		General-purpose I/O port
9	SOT2 (SDA2)	D	Data output of multi-function serial interface 2 (used in I²C mode, SDA2)
	PH2		General-purpose I/O port
28	TIN0	D	Base timer 0 input
	PJ0		General-purpose I/O port
29	TOUT0	D	Base timer 0 output
	PJ1		General-purpose I/O port
30	TIN1	D	Base timer 1 input
	PJ2		General-purpose I/O port
31	TOUT1	D	Base timer 1 output
	PJ3		General-purpose I/O port
25	AIN0	D	8/16-bit up count input pin for up/down counter 0
	PL0		General-purpose I/O port
26	BIN0	D	8/16-bit down count input pin for up/down counter 0
	PL1		General-purpose I/O port
27	ZIN0	D	8/16-bit reset input pin for up/down counter 0
	PL2		General-purpose I/O port
19	IC0	D	Trigger input of input capture 0
	PP0		General-purpose I/O port
20	IC1	D	Trigger input of input capture 1
	PP1		General-purpose I/O port

(Continued)

(Continued)

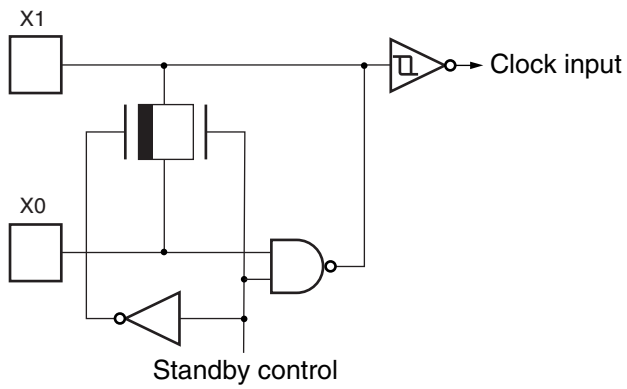
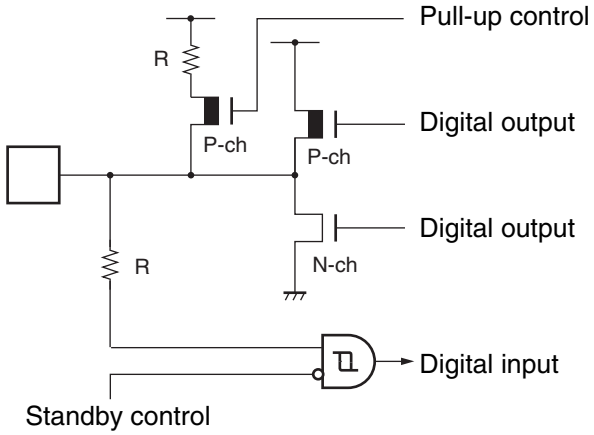
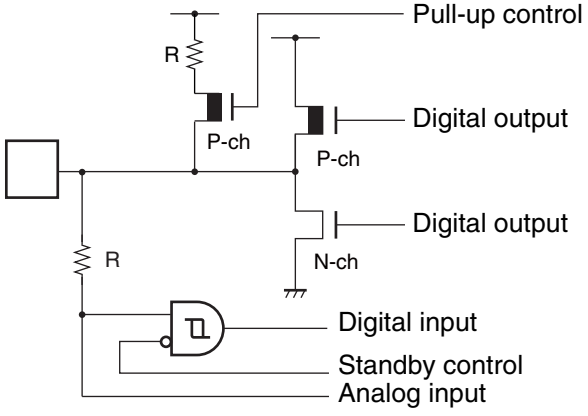
Pin no.	Pin name	I/O circuit type*	Function
21	IC2	D	Trigger input of input capture 2
	PP2		General-purpose I/O port
22	IC3	D	Trigger input of input capture 3
	PP3		General-purpose I/O port
23	CKI0	D	External clock input pin of free-run timer ch.0 to ch.2
	PP4		General-purpose I/O port
24	DTTI0	D	Input signal controlling wave form generator outputs RTO0 to RTO5 of multi-function timer 0
	PP5		General-purpose I/O port
10	RTO0	J	Wave form generator output of multi-function timer 0
	PQ0		General-purpose I/O port
11	RTO1	J	Wave form generator output of multi-function timer 0
	PQ1		General-purpose I/O port
12	RTO2	J	Wave form generator output of multi-function timer 0
	PQ2		General-purpose I/O port
13	RTO3	J	Wave form generator output of multi-function timer 0
	PQ3		General-purpose I/O port
14	RTO4	J	Wave form generator output of multi-function timer 0
	PQ4		General-purpose I/O port
15	RTO5	J	Wave form generator output of multi-function timer 0
	PQ5		General-purpose I/O port

* : Refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types.

Power supply pins and GND pins

Pin no.	Pin name	Function
16 48	VCC	Power supply pins Connect all pins to the same potential.
17 49	VSS	GND pins Connect all pins to the same potential.
18	C	Capacitor coupling pin for internal regulator
37	AVCC10	Analog power supply pin for 8/10-bit A/D converter 1/2
39	AVSS10	Analog GND pin for 8/10-bit A/D converter 1/2
38	AVRH2	Analog reference power supply pin for 8/10-bit A/D converter 1/2

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation feedback resistance for high speed (main clock oscillation) approx. 1 MΩ
D		• CMOS level output • CMOS level hysteresis input • With standby control • With pull-up control
G		• Analog/CMOS level hysteresis I/O pin • CMOS level output • CMOS level hysteresis input (with standby control) • Analog input (Operates as an analog input when the corresponding AICR register bit is “1”.) • With pull-up control

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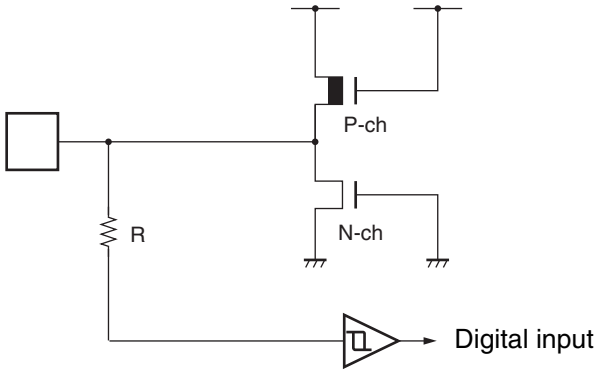
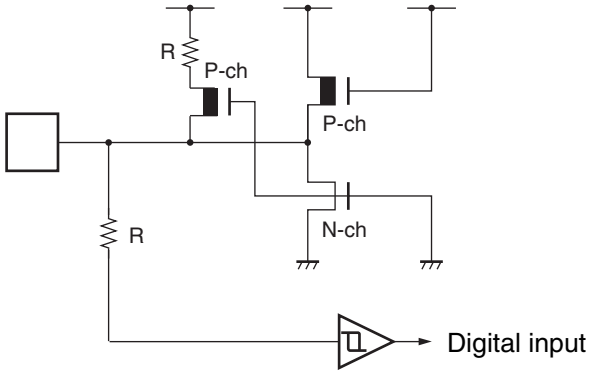
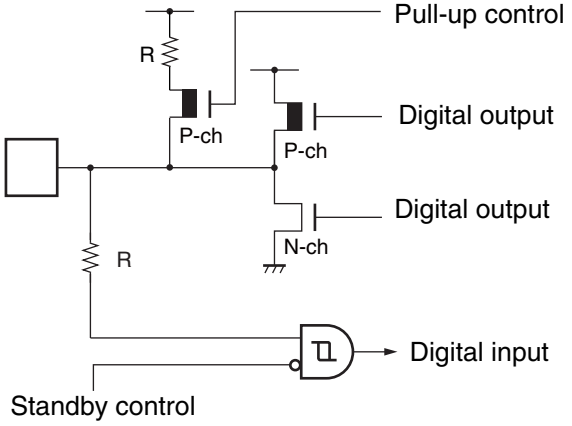
Type	Circuit	Remarks
H		• CMOS level hysteresis input • Without standby control
I		• CMOS level hysteresis input • Without standby control • With pull-up resistance
J		• CMOS level output • CMOS level hysteresis input • With standby control • With pull-up control

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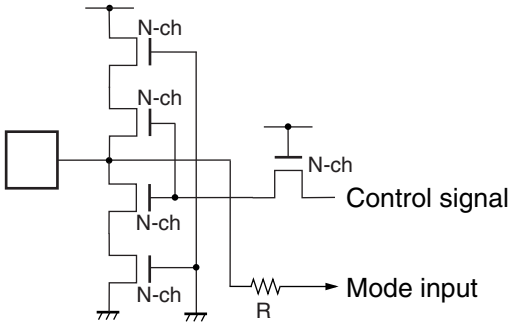
Type	Circuit	Remarks
K		CMOS level input

■ HANDLING DEVICES

• Preventing latch-up

Latch-up phenomenon may occur with CMOS IC, when a voltage higher than V_{CC} or lower than V_{SS} is applied to either the input or output terminals, or when a voltage is applied between VCC pin and VSS pin that exceeds the rated voltage. When latch-up occurs, a significant power-supply current surge results, which may damage some elements due to the excess heat, so great care must be taken to ensure that the maximum rating is never exceeded during use.

• Treatment of unused input pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

• Power pins

In products with multiple VCC and VSS pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to the same potential power supply and a ground line externally to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.
Moreover, connect the current supply source with the VCC and VSS pins of this device at the low impedance.
It is also advisable to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between VCC and VSS pins near this device.

• Crystal oscillator circuit

Noise near the X0 and X1 pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.
It is strongly recommended to design the PC board artwork with the X0 and X1 pins surrounded by ground plane because stable operation can be expected with such a layout. Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• About mode pins (MD0 to MD2)

These pins should be connected directly to V_{CC} pin or V_{SS} pin.
Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and power supply or GND pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

• Operation at start-up

Be sure to execute setting initialized reset (INIT) with INITX pin immediately after start-up.
Immediately after that, also, hold the "L"-level input to the INITX pin for the stabilization wait time required for the oscillator circuit to take the oscillation stabilization wait time for the oscillator circuit and the stabilization wait time for the regulator (For INIT via the INITX pin, the oscillation stabilization wait time setting is initialized to the minimum value).

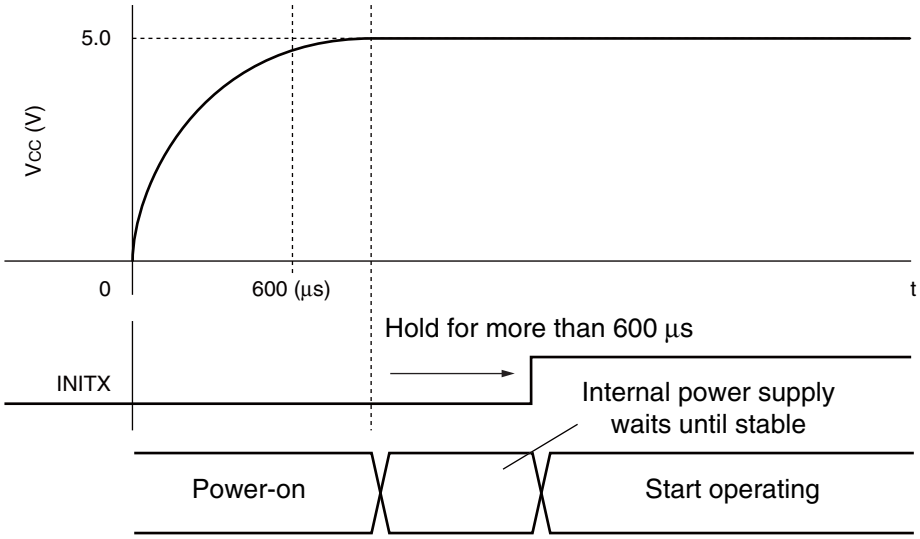
• Notes upon power-on sequence

It requires more than 600 µs (between 0.0 V to 5.0 V) to rise voltage upon power on in order to prevent the device malfunction caused by the overshooting in the built-in voltage step-down circuit.

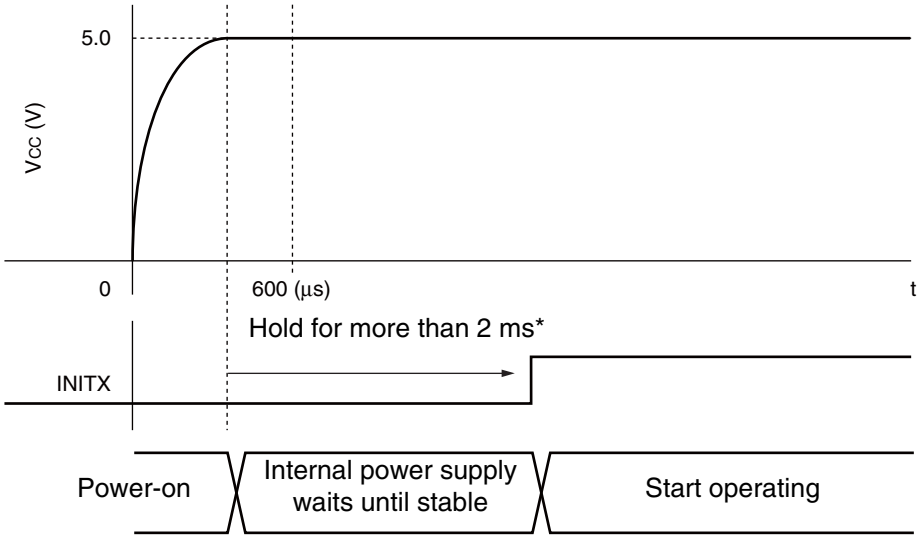
After the supply voltage is stable (voltage is risen) , it takes 600 µs until internal supply is stable. Hold the input to the INITX pin during that period.

If it takes less than 600 µs (between 0.0 V to 5.0 V) for power up, it requires 2 ms* until internal supply is stable after voltage supply is stable (voltage is risen) . Hold the input to the INITX pin during that period.

CASE : voltage rising time is more than 600 µs (0.0 V to 5.0 V)



CASE : voltage rising time is less than 600 µs (0.0 V to 5.0 V)



* : In case of which it takes less than 600 µs (between 0.0 V to 5.0 V) to rise voltage, the time to make internal power supply stable is proportional to the capacitance value of the bypass capacitor for the pin C.
It takes 2 ms if the pin C = 4.7 µF; 4 ms if the pin C = 9.4 µF.

• Order of power turning ON/OFF

Use the following procedure for turning the power on or off. If not using the A/D converter, connect $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$. Turn on the power supply in the sequence $V_{CC} \rightarrow AV_{CC} \rightarrow$ AVRH2, and turn off the power in the reverse sequence.

• Source oscillation input when turning on the power

When turning the power on, maintain the clock input until the device is released from the oscillation stabilization wait state.

• Cautions for operation during PLL clock mode

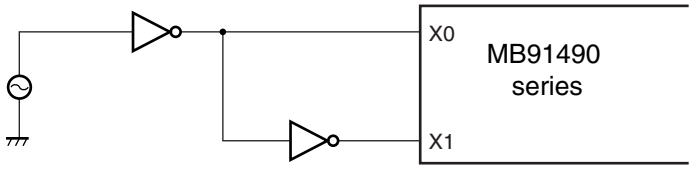
Even if the oscillator comes off or the clock input stops with the PLL clock selected for MB91490 series, MB91490 series may continue to operate at the free-run frequency of the PLL's internal self-oscillating oscillator circuit.
Performance of this operation, however, cannot be guaranteed.

• Using an external clock

When using an external clock, you must always input clock signals with opposite phase from X0 pin to X1 pin simultaneously. However, as the X1 pin halts with an output at the "H" level during stop mode, insert a resistor of approximately 1 kΩ externally to prevent a conflict between the two outputs if using stop mode (oscillation stop mode).

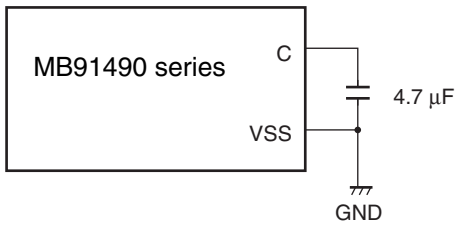
The figure below shows an example of how to use an external clock.

• Example of Using an External Clock



• C pin

As MB91490 series includes an internal regulator, always connect a bypass capacitor of approximately 4.7 µF to the C pin for use by the regulator.

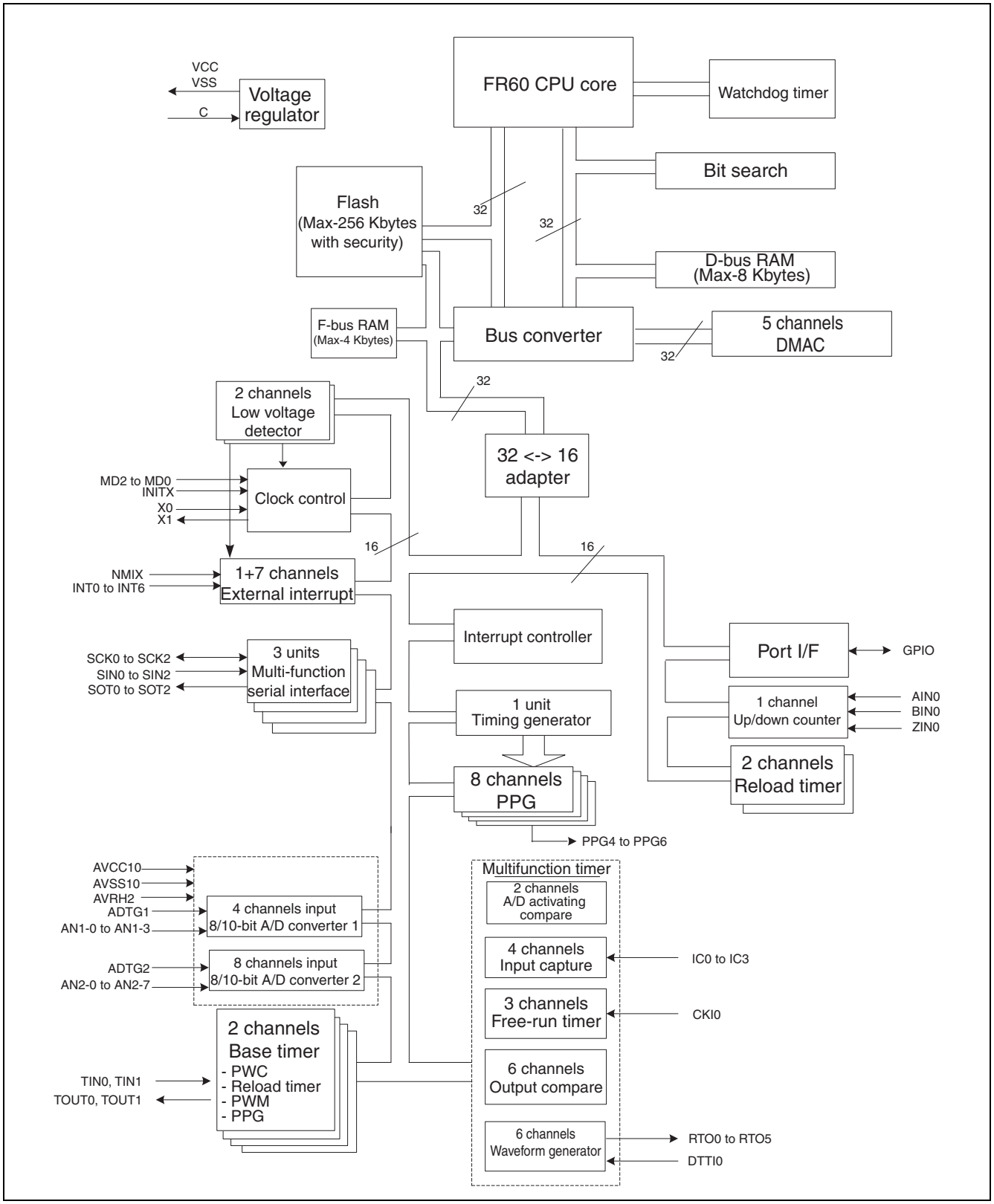


• Software reset on the synchronous mode

Be sure to meet the following two conditions before setting 0 to the SRST bit of STCR (standby control register) when the software reset is used on the synchronous mode.

- Set the interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0).
- Not used NMI

■ BLOCK DIAGRAM



■ MEMORY SPACE

1. Memory Space

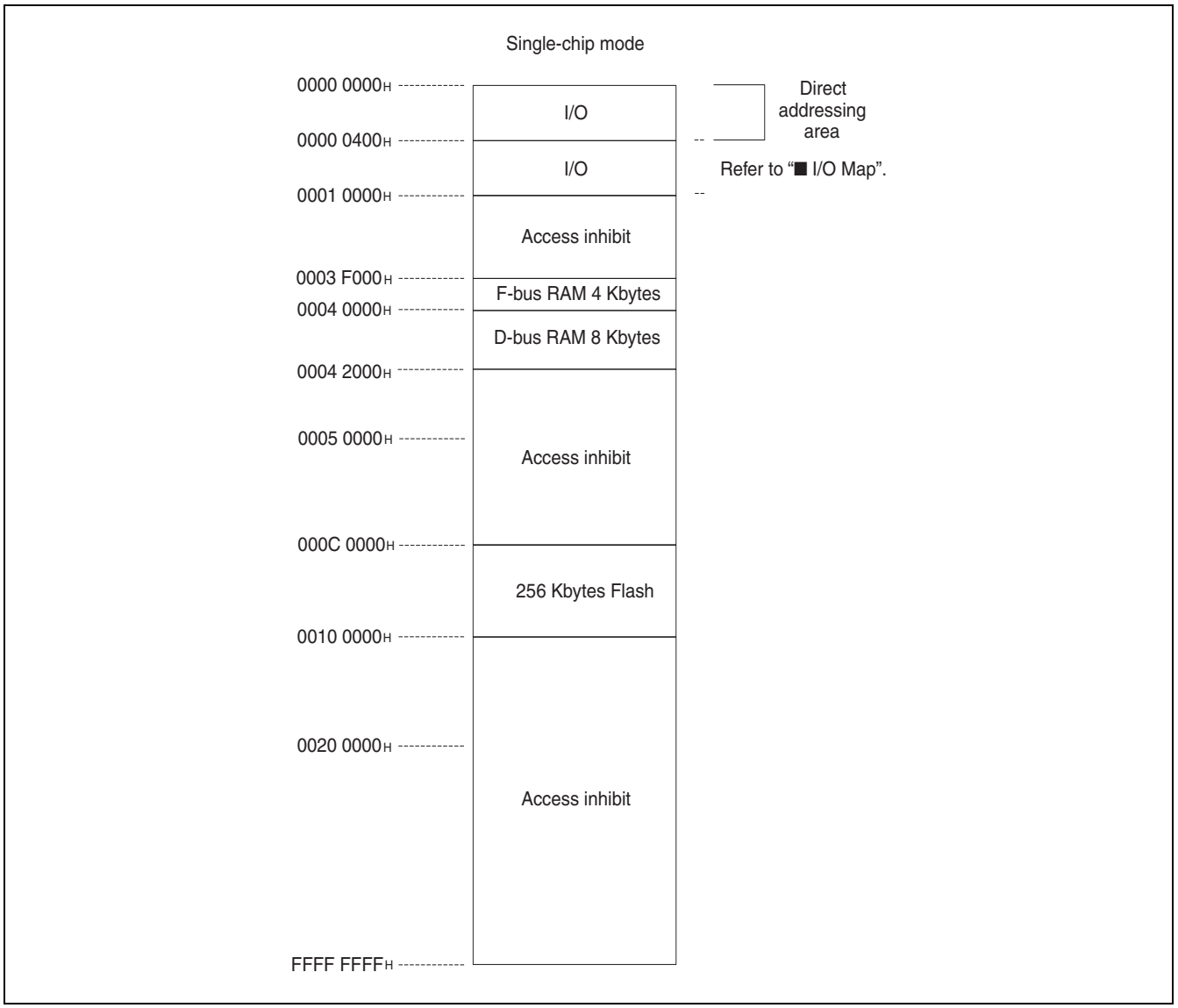
The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

• Direct Addressing Areas

The following address space areas are used as I/O areas.
These areas are called direct addressing areas, in which the address of an operand can be specified directly by the instruction. The size of directly addressable areas depends on the length of the data being accessed as shown below.

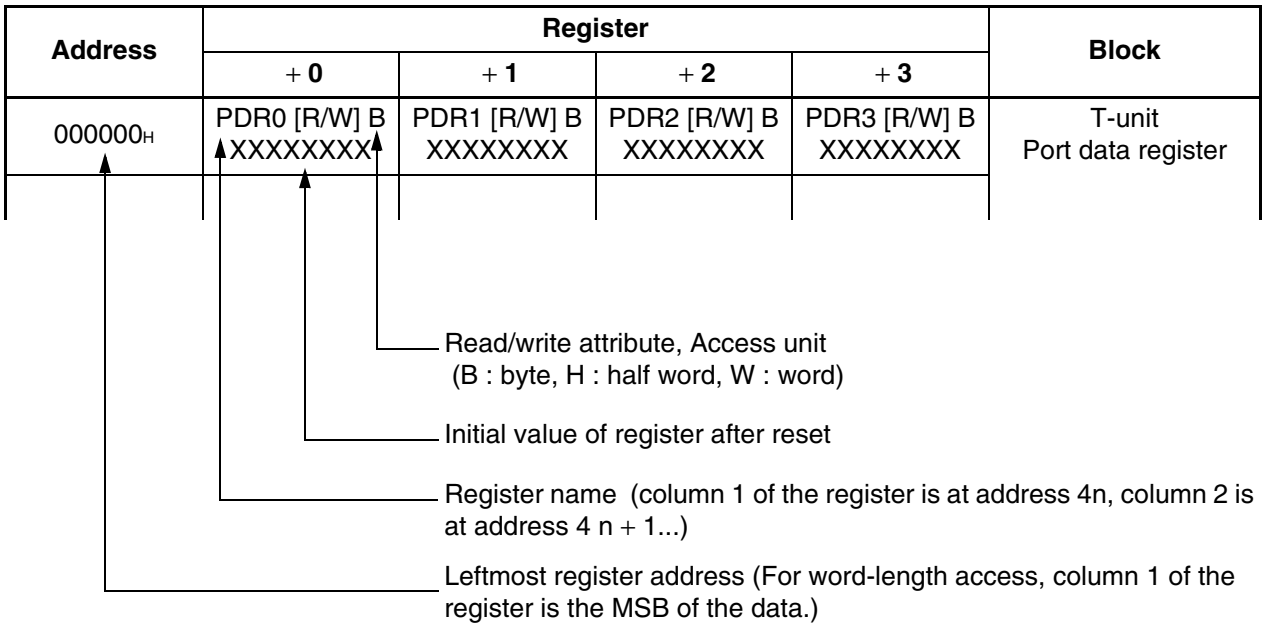
→ byte data access : 000_H to $0FF_H$
→ half word data access : 000_H to $1FF_H$
→ word data access : 000_H to $3FF_H$

2. Memory Map



■ I/O MAP

[How to read the table]



Note : Initial values of register bits are represented as follows :

" 1 " : Initial Value " 1 "

" 0 " : Initial Value " 0 "

" X " : Initial Value " undefined "

" - " : No physical register at this location

Access to addresses where the data access properties have not been documented is prohibited.

Address	Register				Block
	+0	+1	+2	+3	
000000H	—				(Reserved)
000004H	—		PDR8 [R/W] B -XXXXXXX	—	Port data register
000008H	PDRA [R/W] B, H -----XX-	PDRB [R/W] B, H XXXX----	PDRC [R/W] B XXXXXXXX	—	
00000CH	—		PDRG [R/W] B, H --XXXXXX	PDRH [R/W] B, H -----XXX	
000010H	PDRJ [R/W] B ----XXXX	—	PDRL [R/W] B -----XXX	—	
000014H	PDRP [R/W] B, H --XXXXXX	PDRQ [R/W] B, H --XXXXXX	—		
000018H to 00003CH	—				(Reserved)
000040H	EIRR0 [R/W] B, H, W 00000000	ENIR0 [R/W] B, H, W 00000000	ELVR0 [R/W] B, H, W 00000000 00000000		External interrupt (INT0 to INT6, Low voltage detection interrupt)
000044H	DICR [R/W] B, H -------0	HRCL [R/W, R] B, H 0--11111	—		Delay interrupt/ hold request
000048H	TMRLR0 [W] H, W XXXXXXXX XXXXXXXX		TMR0 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 0
00004CH	—		TMCSR0 [R/W, R] B, H ----00-- ---00000		
000050H	TMRLR1 [W] H, W XXXXXXXX XXXXXXXX		TMR1 [R] H, W XXXXXXXX XXXXXXXX		Reload timer 1
000054H	—		TMCSR1 [R/W, R] B, H ----00-- ---00000		
000058H, 00005CH	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000060H	SSR0 [R/W, R] B, H, W 00000011	ESCR0 [R/W]/ IBSR0 [R/W, R] B, H, W 00000000	SCR0 [R/W] / IBCR0 [R/W, R] B, H, W 00000000	SMR0 [R/W] B, H, W 000-0000	Multi-function serial interface 0
000064H	BGR01[R/W] B, H, W 00000000	BGR00 [R/W] B, H, W 00000000	RDR0 [R]/ TDR0 [W] H, W -------0 00000000		
000068H	—		ISMK0 [R/W] B, H 01111111	ISBA0 [R/W] B, H 00000000	
00006CH	—				(Reserved)
000070H	SSR1 [R/W, R] B, H, W 00000011	ESCR1 [R/W]/ IBSR1 [R/W, R] B, H, W 00000000	SCR1 [R/W] / IBCR1 [R/W, R] B, H, W 00000000	SMR1 [R/W] B, H, W 000-0000	Multi-function serial interface 1
000074H	BGR11 [R/W] B, H, W 00000000	BGR10 [R/W] B, H, W 00000000	RDR1 [R]/ TDR1 [W] H, W -------0 00000000		
000078H	—		ISMK1 [R/W] B, H 01111111	ISBA1 [R/W] B, H 00000000	
00007CH	—				(Reserved)
000080H	SSR2 [R/W, R] B, H, W 00000011	ESCR2 [R/W]/ IBSR2 [R/W, R] B, H, W 00000000	SCR2 [R/W] / IBCR2 [R/W, R] B, H, W 00000000	SMR2 [R/W] B, H, W 000-0000	Multi-function serial interface 2
000084H	BGR21 [R/W] B, H, W 00000000	BGR20 [R/W] B, H, W 00000000	RDR2 [R]/ TDR2 [W] H, W -------0 00000000		
000088H	—		ISMK2 [R/W] B, H 01111111	ISBA2 [R/W] B, H 00000000	
00008CH	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000090H to 00009CH	—				(Reserved)
0000A0H	OCCPBH0, OCCPBL0 [W]/ OCCPH0, OCCPL0 [R] H, W 00000000 00000000		OCCPBH1, OCCPBL1 [W]/ OCCPH1, OCCPL1 [R] H, W 00000000 00000000		OCU0
0000A4H	OCCPBH2, OCCPBL2 [W]/ OCCPH2, OCCPL2 [R] H, W 00000000 00000000		OCCPBH3, OCCPBL3 [W]/ OCCPH3, OCCPL3 [R] H, W 00000000 00000000		
0000A8H	OCCPBH4, OCCPBL4 [W]/ OCCPH4, OCCPL4 [R] H, W 00000000 00000000		OCCPBH5, OCCPBL5 [W]/ OCCPH5, OCCPL5 [R] H, W 00000000 00000000		
0000ACH	OCSH1 [R/W] B, H, W -110--00	OCSL0 [R/W] B, H, W 00001100	OCSH3 [R/W] B, H, W -110--00	OCSL2 [R/W] B, H, W 00001100	
0000B0H	OCSH5 [R/W] B, H -110--00	OCSL4 [R/W] B, H 00001100	OCMOD0 [R/W] B --000000	—	
0000B4H	CPCLRBH0, CPCLRBL0 [W]/ CPCLRH0, CPCLRL0 [R] H, W 11111111 11111111		TCDTH0, TCDTL0 [R/W] H, W 00000000 00000000		Free-run timer 0
0000B8H	TCCSH0 [R/W] B, H, W 00000000	TCCSL0 [R/W] B, H, W 01000000	TCCSM0 [R/W] B, H, W ----0000	ADTRGC0 [R/W] B, H, W -0-0-0-0	
0000BCH	CPCLRBH1, CPCLRBL1 [W] / CPCLRH1, CPCLRL1 [R] H, W 11111111 11111111		TCDTH1, TCDTL1 [R/W] H, W 00000000 00000000		Free-run timer 1
0000C0H	TCCSH1 [R/W] B, H, W 00000000	TCCSL1 [R/W] B, H, W 01000000	TCCSM1 [R/W] B, H, W ----0000	ADTRGC1 [R/W] B, H, W -0-0-0-0	
0000C4H	CPCLRBH2, CPCLRBL2 [W] / CPCLRH2, CPCLRL2 [R] H, W 11111111 11111111		TCDTH2, TCDTL2 [R/W] H, W 00000000 00000000		Free-run timer 2
0000C8H	TCCSH2 [R/W] B, H, W 00000000	TCCSL2 [R/W] B, H, W 01000000	TCCSM2 [R/W] B, H, W ----0000	ADTRGC2 [R/W] B, H, W -0-0-0-0	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000CCH	—	FRS2 [R/W] B --00--00	FRS1 [R/W] B, H --00--00	FRS0 [R/W] B, H --00--00	Free-run timer selector 0
0000D0H	—		FRS4 [R/W] B, H --00--00	FRS3 [R/W] B, H --00--00	
0000D4H	IPCPH0, IPCPL0 [R] H, W XXXXXXXX XXXXXXXX		IPCPH1, IPCPL1 [R] H, W XXXXXXXX XXXXXXXX		ICU0
0000D8H	IPCPH2, IPCPL2 [R] H, W XXXXXXXX XXXXXXXX		IPCPH3, IPCPL3 [R] H, W XXXXXXXX XXXXXXXX		
0000DCH	PICSH01 [W, R] B, H, W 00000000	PICSL01 [R/W] B, H, W 00000000	ICSH23 [R] B, H, W ------00	ICSL23[R/W] B, H, W 00000000	
0000E0H	TMRRH0, TMRRL0 [R/W] H, W XXXXXXXX XXXXXXXX		TMRRH1, TMRRL1 [R/W] H, W XXXXXXXX XXXXXXXX		Wave form generator 0
0000E4H	TMRRH2, TMRRL2 [R/W] H XXXXXXXX XXXXXXXX		—		
0000E8H	DTCR0 [R/W] B, H 00000000	DTCR1 [R/W] B, H 00000000	DTCR2 [R/W] B 00000000	—	
0000ECH	—	SIGCR10 [R/W] B 00000000	—	SIGCR20 [R/W] B 000000-1	
0000F0H	ADCOMP0 [W]/ ADCOMPB0 [R] H, W 00000000 00000000		ADCOMPD0 [W]/ ADCOMPDB0 [R] H, W 00000000 00000000		A/D activating compare 0
0000F4H	—				
0000F8H	ADCOMP2 [W]/ ADCOMPB2 [R] H, W 00000000 00000000		ADCOMPD2 [W]/ ADCOMPDB2 [R] H, W 00000000 00000000		
0000FCH	—	ADTGBUF0 [R/W] B -0-0-1-1	ADTGSEL0 [R/W] B, H --00--00	ADTGCE0 [R/W] B, H --00--00	
000100H	PRLH0 [R/W] B, H, W XXXXXXXX	PRLL0 [R/W] B, H, W XXXXXXXX	PRLH1 [R/W] B, H, W XXXXXXXX	PRLL1 [R/W] B, H, W XXXXXXXX	PPG
000104H	PRLH2 [R/W] B, H, W XXXXXXXX	PRLL2 [R/W] B, H, W XXXXXXXX	PRLH3 [R/W] B, H, W XXXXXXXX	PRLL3 [R/W] B, H, W XXXXXXXX	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000108H	PPGC0 [R/W] B, H, W 00000000	PPGC1 [R/W] B, H, W 00000000	PPGC2 [R/W] B, H, W 00000000	PPGC3 [R/W] B, H, W 00000000	PPG
00010CH	PRLH4 [R/W] B, H, W XXXXXXXX	PRLL4 [R/W] B, H, W XXXXXXXX	PRLH5 [R/W] B, H, W XXXXXXXX	PRLL5 [R/W] B, H, W XXXXXXXX	
000110H	PRLH6 [R/W] B, H, W XXXXXXXX	PRLL6 [R/W] B, H, W XXXXXXXX	PRLH7 [R/W] B, H, W XXXXXXXX	PRLL7 [R/W] B, H, W XXXXXXXX	
000114H	PPGC4 [R/W] B, H, W 00000000	PPGC5 [R/W] B, H, W 00000000	PPGC6 [R/W] B, H, W 00000000	PPGC7 [R/W] B, H, W 00000000	
000118H to 00012CH	—				(Reserved)
000130H	—	TRG [R/W] B 00000000	—	GATEC0 [R/W] B --00--00	PPG
000134H	—	REVC [R/W] B 00000000	—	GATEC4 [R/W] B ------00	
000138H to 000140H	—				(Reserved)
000144H	TTCR0 [R/W, W, R] B 11110000	—			Timing generator 0
000148H	COMP0 [R/W] B, H, W 00000000	COMP2 [R/W] B, H, W 00000000	COMP4 [R/W] B, H, W 00000000	COMP6 [R/W] B, H, W 00000000	
00014CH to 00015CH	—				(Reserved)
000160H	BT0TMR [R] B, H, W 00000000 00000000		BT0TMCR [R/W] B, H, W -0000000 00000000		Base timer 0
000164H	—	BT0STC [R/W] B 00000000	—		
000168H	BT0PCSR/BT0PRLL [R/W] H, W XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H, W XXXXXXXX XXXXXXXX		
00016CH	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000170H	AICR2 [R/W] B, H -------- 11111111		—		8/10-bit A/D converter 2 (8 channels)
000174H	ADCS2 [R/W, W] B 0000000-	—	ADCH2 [R/W] B, H 00000000	ADMD2 [R/W] B, H 00001111	
000178H	ADCD002 [R] B, H, W 10----XX XXXXXXXX		ADCD012 [R] B, H, W 10----XX XXXXXXXX		
00017CH	ADCD022 [R] B, H, W 10----XX XXXXXXXX		ADCD032 [R] B, H, W 10----XX XXXXXXXX		
000180H	ADCD042 [R] B, H, W 10----XX XXXXXXXX		ADCD052 [R] B, H, W 10----XX XXXXXXXX		
000184H	ADCD062 [R] B, H, W 10----XX XXXXXXXX		ADCD072 [R] B, H, W 10----XX XXXXXXXX		
000188H to 0001FCH	—				(Reserved)
000200H	DMACA0 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] B, H, W * 00000000 ----XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000228H to 00023CH	—				(Reserved)
000240H	DMACR [R/W] B, H, W 0--00000 -------- -------- --------				DMAC
000244H to 0003ECH	—				(Reserved)
0003F0H	BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit search module
0003F4H	BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	—				(Reserved)
000404H	—		DDR8 [R/W] B -0000000	—	Port direction register
000408H	DDRA [R/W] B, H -----00-	DDRB [R/W] B, H 0000----	DDRC [R/W] B 00000000	—	
00040CH	—		DDRG [R/W] B, H --000000	DDRH [R/W] B, H -----000	
000410H	DDRJ [R/W] B ----0000	—	DDRL [R/W] B -----000	—	
000414H	DDRP [R/W] B, H --000000	DDRQ [R/W] B, H --000000	—		
000418H to 000420H	—				(Reserved)
000424H	—		PFR8 [R/W] B -000----	—	Port function register
000428H	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00042C$_H$	—		PFRG [R/W] B, H --0-00-0	PFRH [R/W] B, H -----0-0	Port function register
000430$_H$	PFRJ [R/W] B ----0-0-	—			
000434$_H$	—	PFRQ [R/W] B --000000	—		
000438$_H$, 00043C$_H$	—				(Reserved)
000440$_H$	ICR00 [R/W, R] B, H, W ---11111	ICR01 [R/W, R] B, H, W ---11111	ICR02 [R/W, R] B, H, W ---11111	ICR03 [R/W, R] B, H, W ---11111	Interrupt controller
000444$_H$	ICR04 [R/W, R] B, H, W ---11111	ICR05 [R/W, R] B, H, W ---11111	ICR06 [R/W, R] B, H, W ---11111	ICR07 [R/W, R] B, H, W ---11111	
000448$_H$	ICR08 [R/W, R] B, H, W ---11111	ICR09 [R/W, R] B, H, W ---11111	ICR10 [R/W, R] B, H, W ---11111	ICR11 [R/W, R] B, H, W ---11111	
00044C$_H$	ICR12 [R/W, R] B, H, W ---11111	ICR13 [R/W, R] B, H, W ---11111	ICR14 [R/W, R] B, H, W ---11111	ICR15 [R/W, R] B, H, W ---11111	
000450$_H$	ICR16 [R/W, R] B, H, W ---11111	ICR17 [R/W, R] B, H, W ---11111	ICR18 [R/W, R] B, H, W ---11111	ICR19 [R/W, R] B, H, W ---11111	
000454$_H$	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000458H	ICR24 [R/W, R] B, H, W ---11111	ICR25 [R/W, R] B, H, W ---11111	ICR26 [R/W, R] B, H, W ---11111	ICR27 [R/W, R] B, H, W ---11111	Interrupt controller
00045CH	ICR28 [R/W, R] B, H, W ---11111	ICR29 [R/W, R] B, H, W ---11111	ICR30 [R/W, R] B, H, W ---11111	ICR31 [R/W, R] B, H, W ---11111	
000460H	—	ICR33 [R/W, R] B ---11111	ICR34 [R/W, R] B, H ---11111	ICR35 [R/W, R] B, H ---11111	
000464H	ICR36 [R/W, R] B, H, W ---11111	ICR37 [R/W, R] B, H, W ---11111	ICR38 [R/W, R] B, H, W ---11111	ICR39 [R/W, R] B, H, W ---11111	
000468H	—	ICR41 [R/W, R] B ---11111	ICR42 [R/W, R] B, H ---11111	ICR43 [R/W, R] B, H ---11111	
00046CH	ICR44 [R/W, R] B, H, W ---11111	ICR45 [R/W, R] B, H, W ---11111	ICR46 [R/W, R] B, H, W ---11111	ICR47 [R/W, R] B, H, W ---11111	
000470H to 00047CH	—				(Reserved)
000480H	RSRR [R/W] B, H, W 1-0-0-00	STCR [R/W] B, H, W 001100-1	TBCR [R/W] B, H, W 00XXX-00	CTBR [W] B, H, W XXXXXXXX	Clock control block
000484H	CLKR [R/W] B -000-000	—	DIVR0 [R/W] B 00000011	—	
000488H to 00050CH	—				(Reserved)
000510H	—	AICR1 [R/W] B ----1111	—		8/10-bit A/D converter 1 (4 channels)
000514H	ADCS1 [R/W, W] B 0000000-	—	ADCH1 [R/W] B, H --00--00	ADMD1 [R/W] B, H 00001111	
000518H	ADCD001 [R] B, H, W 10----XX XXXXXXXX		ADCD011 [R] B, H, W 10----XX XXXXXXXX		
00051CH	ADCD021 [R] B, H, W 10----XX XXXXXXXX		ADCD031 [R] B, H, W 10----XX XXXXXXXX		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000520H to 00053CH	—				(Reserved)
000540H	RCR10 [W] B, H, W XXXXXXXX	RCR00 [W] B, H, W XXXXXXXX	UDCR10 [R] B, H, W 00000000	UDCR00 [R] B, H, W 00000000	Up/down counter 0
000544H	CCRH0 [R/W] B, H 00000000	CCRL0 [R/W, R] B, H -0001000	—	CSR0 [R/W, R] B 00000000	
000548H to 00057CH	—				(Reserved)
000580H	BT1TMR [R] B, H, W 00000000 00000000		BT1TMCR [R/W] B, H, W -0000000 00000000		Base timer 1
000584H	—	BT1STC [R/W] B 00000000	—		
000588H	BT1PCSR/BT1PRLL [R/W] H, W XXXXXXXX XXXXXXXX		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H, W XXXXXXXX XXXXXXXX		
00058CH to 000600H	—				(Reserved)
000604H	—		PCR8 [R/W] B -0000000	—	Pull-up resistor control register
000608H	PCRA [R/W] B, H -----00-	PCRB [R/W] B, H 0000----	PCRC [R/W] B 00000000	—	
00060CH	—		PCRG [R/W] B, H --000000	PCRH [R/W] B, H -----000	
000610H	PCRJ [R/W] B ----0000	—	PCRL [R/W] B -----000	—	
000614H	PCRP [R/W] B, H --000000	PCRQ [R/W] B, H --000000	—		
000618H to 000FFCH	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
001000H	DMASA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 006FFCH	—				(Reserved)
007000H	FLCR [R/W, R] B ----X-0-	—			Flash memory
007004H	FLWC [R/W] B --11-011	—			
007008H to 007010H	—				
007014H to 00701CH	—				(Reserved)
007020H	WREN [R/W] H 00000000 00000000		—		Wild register control block
007024H to 00702CH	—				(Reserved)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
007030H	WA00 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				Wild register control block
007034H	WD00 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007038H	WA01 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00703CH	WD01 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007040H	WA02 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007044H	WD02 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007048H	WA03 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00704CH	WD03 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007050H	WA04 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007054H	WD04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007058H	WA05 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00705CH	WD05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007060H	WA06 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007064H	WD06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007068H	WA07 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00706CH	WD07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007070H	WA08 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007074H	WD08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
007078H	WA09 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				Wild register control block
00707CH	WD09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007080H	WA10 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007084H	WD10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007088H	WA11 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00708CH	WD11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007090H	WA12 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
007094H	WD12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
007098H	WA13 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
00709CH	WD13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0070A0H	WA14 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
0070A4H	WD14 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0070A8H	WA15 [R/W] W -------- ----XXXX XXXXXXXX XXXXXX--				
0070ACH	WD15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0070B0H to 0FFFFCH	—				(Reserved)

* : The lower 16 bits (DTC15 to DTC0) of DMACA0 to DMACA4 cannot be accessed as bytes.

Notes :
- Data is undefined in reserved or (—) area.
- Do not execute read modify write (RMW) instruction on registers having a write-only bit.
- The initial values are varied depending on the product series. Please refer to the hardware manual of MB91490 series for more details.

■ INTERRUPT VECTOR

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
Reset	0	00	—	3FC$_H$	000FFFFC$_H$
Mode vector	1	01	—	3F8$_H$	000FFFF8$_H$
System reserved	2	02	—	3F4$_H$	000FFFF4$_H$
System reserved	3	03	—	3F0$_H$	000FFFF0$_H$
System reserved	4	04	—	3EC$_H$	000FFFEC$_H$
System reserved	5	05	—	3E8$_H$	000FFFE8$_H$
System reserved	6	06	—	3E4$_H$	000FFFE4$_H$
Coprocessor absent trap	7	07	—	3E0$_H$	000FFFE0$_H$
Coprocessor error trap	8	08	—	3DC$_H$	000FFFDC$_H$
INTE instruction	9	09	—	3D8$_H$	000FFFD8$_H$
System reserved	10	0A	—	3D4$_H$	000FFFD4$_H$
System reserved	11	0B	—	3D0$_H$	000FFFD0$_H$
Step trace trap	12	0C	—	3CC$_H$	000FFFCC$_H$
NMI request (tool)	13	0D	—	3C8$_H$	000FFFC8$_H$
Undefined instruction exception	14	0E	—	3C4$_H$	000FFFC4$_H$
NMI request	15	0F	—	3C0$_H$	000FFFC0$_H$
External interrupt 0	16	10	ICR00	3BC$_H$	000FFFBC$_H$
External interrupt 1	17	11	ICR01	3B8$_H$	000FFFB8$_H$
External interrupt 2	18	12	ICR02	3B4$_H$	000FFFB4$_H$
External interrupt 3	19	13	ICR03	3B0$_H$	000FFFB0$_H$
External interrupt 4	20	14	ICR04	3AC$_H$	000FFFAC$_H$
External interrupt 5	21	15	ICR05	3A8$_H$	000FFFA8$_H$
External interrupt 6	22	16	ICR06	3A4$_H$	000FFFA4$_H$
Low voltage detection interrupt	23	17	ICR07	3A0$_H$	000FFFA0$_H$
Reload timer 0	24	18	ICR08	39C$_H$	000FFF9C$_H$
Reload timer 1	25	19	ICR09	398$_H$	000FFF98$_H$
Base timer 0 (source 0/source 1)	26	1A	ICR10	394$_H$	000FFF94$_H$
Multi-function serial interface 0 (UART transmission completed/reception completed/I^{2}C status)	27	1B	ICR11	390$_H$	000FFF90$_H$
Multi-function serial interface 1 (UART transmission completed/reception completed/I^{2}C status)	28	1C	ICR12	38C$_H$	000FFF8C$_H$
Base timer 1 (source 0/source 1)	29	1D	ICR13	388$_H$	000FFF88$_H$

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
Up/down counter 0	30	1E	ICR14	384H	000FFF84H
DTTI0	31	1F	ICR15	380H	000FFF80H
DMAC0 (end/error)	32	20	ICR16	37CH	000FFF7CH
DMAC1 (end/error)	33	21	ICR17	378H	000FFF78H
DMAC2/3/4 (end/error)	34	22	ICR18	374H	000FFF74H
Multi-function serial interface 2 (UART transmission completed/reception completed/I²C status)	35	23	ICR19	370H	000FFF70H
System reserved	36	24	—	36CH	000FFF6CH
System reserved	37	25	—	368H	000FFF68H
System reserved	38	26	—	364H	000FFF64H
System reserved	39	27	—	360H	000FFF60H
PPG0/PPG1	40	28	ICR24	35CH	000FFF5CH
PPG2/PPG3	41	29	ICR25	358H	000FFF58H
PPG4/PPG5	42	2A	ICR26	354H	000FFF54H
PPG6/PPG7	43	2B	ICR27	350H	000FFF50H
Wave form generator 0 (underflow)	44	2C	ICR28	34CH	000FFF4CH
Wave form generator 1 (underflow)	45	2D	ICR29	348H	000FFF48H
Wave form generator 2 (underflow)	46	2E	ICR30	344H	000FFF44H
Timebase timer overflow	47	2F	ICR31	340H	000FFF40H
System reserved	48	30	—	33CH	000FFF3CH
Free-run timer 0 (compare clear)	49	31	ICR33	338H	000FFF38H
Free-run timer 0 (zero detection)	50	32	ICR34	334H	000FFF34H
Free-run timer 1 (compare clear)	51	33	ICR35	330H	000FFF30H
Free-run timer 1 (zero detection)	52	34	ICR36	32CH	000FFF2CH
Free-run timer 2 (compare clear)	53	35	ICR37	328H	000FFF28H
Free-run timer 2 (zero detection)	54	36	ICR38	324H	000FFF24H
8/10-bit A/D converter 2	55	37	ICR39	320H	000FFF20H
System reserved	56	38	—	31CH	000FFF1CH
8/10-bit A/D converter 1	57	39	ICR41	318H	000FFF18H
ICU0/ICU1 (capture)	58	3A	ICR42	314H	000FFF14H
ICU2/ICU3 (capture)	59	3B	ICR43	310H	000FFF10H
OCU0/OCU1 (match)	60	3C	ICR44	30CH	000FFF0CH

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	TBR default address
	Decimal	Hexa-decimal			
OCU2/OCU3 (match)	61	3D	ICR45	308H	000FFF08H
OCU4/OCU5 (match)	62	3E	ICR46	304H	000FFF04H
Interrupt delay source bit	63	3F	ICR47	300H	000FFF00H
System reserved (Used by REALOS)	64	40	—	2FCH	000FFEFCH
System reserved (Used by REALOS)	65	41	—	2F8H	000FFEF8H
System reserved	66	42	—	2F4H	000FFEF4H
System reserved	67	43	—	2F0H	000FFEF0H
System reserved	68	44	—	2ECH	000FFEECH
System reserved	69	45	—	2E8H	000FFEE8H
System reserved	70	46	—	2E4H	000FFEE4H
System reserved	71	47	—	2E0H	000FFEE0H
System reserved	72	48	—	2DCH	000FFEDCH
System reserved	73	49	—	2D8H	000FFED8H
System reserved	74	4A	—	2D4H	000FFED4H
System reserved	75	4B	—	2D0H	000FFED0H
System reserved	76	4C	—	2CCH	000FFECCH
System reserved	77	4D	—	2C8H	000FFEC8H
System reserved	78	4E	—	2C4H	000FFEC4H
System reserved	79	4F	—	2C0H	000FFEC0H
Used by INT instruction	80 to 255	50 to FF	—	2BCH to 000H	000FFEBCH to 000FFC00H

■ PIN STATUS IN EACH CPU STATE

Terms used as the status of pins mean as follows.

- Input enabled
  Means that the input function can be used.

- Input disabled
  Indicates that the input function cannot be used.

- Input fixed to “0”
  A state of a pin, in which "0" is transmitted to internal circuitry, with the external input shut off by the input gate adjacent to the pin.

- Output Hi-Z
  Means to place a pin in a high impedance state by disabling the pin driving transistor from driving.

- Preserving the previous state
  Means to output the state existing immediately prior to entering this mode.
  That is, to output according to an internal resource with an output when it is operating or to preserve an output when the output is provided, for example, as a port.

- Input enabled when external interrupt function selected and enabled
  Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

• List of pin status

Pin name	Function	During initialization		In sleep mode	In stop mode	
		INITX = "L"*1 or when Low voltage detection reset occurs	INITX = "H"*2 or when Low voltage detection reset is released		HIZ = 0	HIZ = 1
NMIX	NMIX	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
P80 to P83	INT0 to INT3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Input enabled	Input enabled	Output Hi-Z/ Input "0" fixed
P84	INT4/PPG4					
P85	INT5/PPG5					Input enabled when interrupt function selected and enabled
P86	INT6/PPG6					
PA1, PA2	ADTG1, ADTG2	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PB4 to PB7	AN1-0 to AN1-3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input "0" fixed	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/ Input "0" fixed
PC0 to PC7	AN2-0 to AN2-7					
PG0, PG3	SCK0, SCK1	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/Input "0" fixed
PG1, PG4	SIN0, SIN1					
PG2, PG5	SOT0, SOT1					
PH0	SCK2					
PH1	SIN2					
PH2	SOT2					
PJ0, PJ2	TIN0, TIN1	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/Input "0" fixed
PJ1, PJ3	TOUT0, TOUT1					
PL0	AIN0	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/Input "0" fixed
PL1	BIN0					
PL2	ZIN0					
PP0 to PP3	IC0 to IC3	Output Hi-Z/ Input disabled	Output Hi-Z/ Input enabled	Retention of the immediately prior state	Retention of the immediately prior state	Output Hi-Z/Input "0" fixed
PP4	CKI0					
PP5	DTTI0					
PQ0 to PQ5	RTO0 to RTO5					

*1 : INITX = "L" : Indicates the pin status with INITX remaining at the "L" level.

*2 : INITX = "H" : Indicates the pin status existing immediately after INITX transition from "L" to "H" level.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.5	V_{SS} + 6.0	V	
Analog power supply voltage*1,*2,*6	AVCC10	V_{SS} – 0.5	V_{SS} + 6.0	V	
Analog reference voltage*7	AVRH2	V_{SS} – 0.5	V_{SS} + 6.0	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Analog pin input voltage*1	V_{IA}	V_{SS} – 0.3	AV_{CC} + 0.3	V	
Output voltage*1	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current*3	I_{OL}	—	10	mA	
“L” level average output current*4	I_{OLAV}	—	4	mA	Except port Q0 to Q5
			12	mA	Port Q0 to Q5
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current*5	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current*3	I_{OH}	—	–10	mA	
“H” level average output current *4	I_{OHAV}	—	–4	mA	Except port Q0 to Q5
			–12	mA	Port Q0 to Q5
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current*5	ΣI_{OHAV}	—	–50	mA	
Power consumption	P_D	—	430	mW	
Storage temperature	T_{STG}	–55	+125	°C	

*1 : The parameter is based on V_{SS} = AVSS10 = 0 V.

*2 : Be careful not to exceed V_{CC} + 0.3 V, for example, when the power is turned on.
Be careful to set AVCC10 equal V_{CC}, for example, when the power is turned on.

*3 : The maximum output current is the peak value for a single pin.

*4 : The average output is the average current for a single pin over a period of 100 ms.

*5 : The total average output current is the average current for all pins over a period of 100 ms.

*6 : AVCC10 is the analog supply voltage for the 8/10-bit A/D converter.

*7 : AVRH2 is the analog reference voltage for the 8/10-bit A/D converter.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AVSS10 = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.7	5.5	V	
Analog power supply voltage	AVCC10	V_{SS} + 2.7	V_{SS} + 5.5	V	For all 8/10-bit A/D converters (common use)
Analog reference voltage	AVRH2	AVSS10	AVCC10	V	For all 8/10-bit A/D converters (common use)
Operating temperature	T_A	− 40	+ 85	°C	

Note : During power-on, it takes approximately 600 µs for the internal power supply to stabilize after the V_{CC} power supply has stabilized. Continue to assert the INITX pin during this period.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to +85 °C)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	CMOS hysteresis input pin	—	$V_{CC} \times 0.8$	—	V_{CC}	V	
"L" level input voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS}	—	$V_{CC} \times 0.2$	V	
"H" level output voltage	V_{OH1}	Except port Q0 to Q5	V_{CC} = 5.0 V, I_{OH} = 4 mA	V_{CC} − 0.5	—	—	V	
	V_{OH2}	Port Q0 to Q5	V_{CC} = 5.0 V, I_{OH} = 12 mA	V_{CC} − 0.5	—	—	V	*1
			V_{CC} = 3.0 V, I_{OH} = 4 mA	V_{CC} − 0.5	—	—	V	*2
"L" level output voltage	V_{OL1}	Except port Q0 to Q5	V_{CC} = 5.0 V, I_{OL} = 4 mA	—	—	V_{SS} + 0.4	V	
	V_{OL2}	Port Q0 to Q5	V_{CC} = 5.0 V, I_{OL} = 12 mA	—	—	V_{SS} + 0.4	V	*1
			V_{CC} = 3.0 V, I_{OL} = 4 mA	—	—	V_{SS} + 0.4	V	*2
Input leak current	I_{LI}	—	V_{CC} = 5.0 V, $V_{SS} < V_I < V_{CC}$	− 5	—	—	µA	
Pull-up resistance	R_{PULL}	INITX, pull-up pin	—	—	50	—	kΩ	
Power supply current	I_{CC}	VCC	V_{CC} = 5.0 V, f_C = 20 MHz, PLL × 4, CLKB = 80 MHz CLKP = 40 MHz Flash memory 3 wait (4cycle) access	—	60	70	mA	
			V_{CC} = 5.0 V, f_C = 10 MHz, PLL × 5, CLKB = 50 MHz CLKP = 25 MHz Flash memory 2 wait (3cycle) access	—	45	55	mA	
			V_{CC} = 5.0 V, f_C = 10 MHz, PLL × 4, CLKB = 40 MHz CLKP = 40 MHz Flash memory 2 wait (3cycle) access	—	40	50	mA	

(Continued)

(Continued)

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to +85 °C)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCS}	VCC	V_{CC} = 5.0 V, f_C = 20 MHz, PLL × 4, CLKB = 80 MHz CLKP = 40 MHz Flash memory 3 wait (4cycle) access	—	15	22	mA	In sleep mode
			V_{CC} = 5.0 V, f_C = 10 MHz, PLL × 5, CLKB = 50 MHz CLKP = 25 MHz Flash memory 2 wait (3cycle) access	—	9	15	mA	In sleep mode
			V_{CC} = 5.0 V, f_C = 10 MHz, PLL × 4, CLKB = 40 MHz CLKP = 40 MHz Flash memory 2 wait (3cycle) access	—	11	17	mA	In sleep mode
	I_{CCH}	VCC	V_{CC} = 5.0 V, T_A = + 25 °C	—	60	200	µA	In stop mode
Input capacitance	C_{IN}	Other than VCC, VSS, AVSS10, AVCC10, AVRH2	—	—	5	15	pF	

*1 : V_{CC} = 4.0 V to 5.5 V

*2 : V_{CC} = 2.7 V to 4.0 V

4. Flash Memory Write/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (8 Kbytes sectors)	V_{CC} = 5.0 V, T_A = +25 °C	—	0.5	2.0	s	Not including time for internal writing before deletion.
Word write time	V_{CC} = 5.0 V, T_A = +25 °C	—	6	100	µs	Not including system-level overhead time.
Chip erase time	V_{CC} = 5.0 V, T_A = +25 °C	—	1.8	29.5	s	Not including system-level overhead time.
Erase/write cycle	—	10000	—	—	cycle	
Flash memory data hold time	—	10	—	—	year	

5. AC Characteristics

(1) Clock Timing

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to +85 °C)

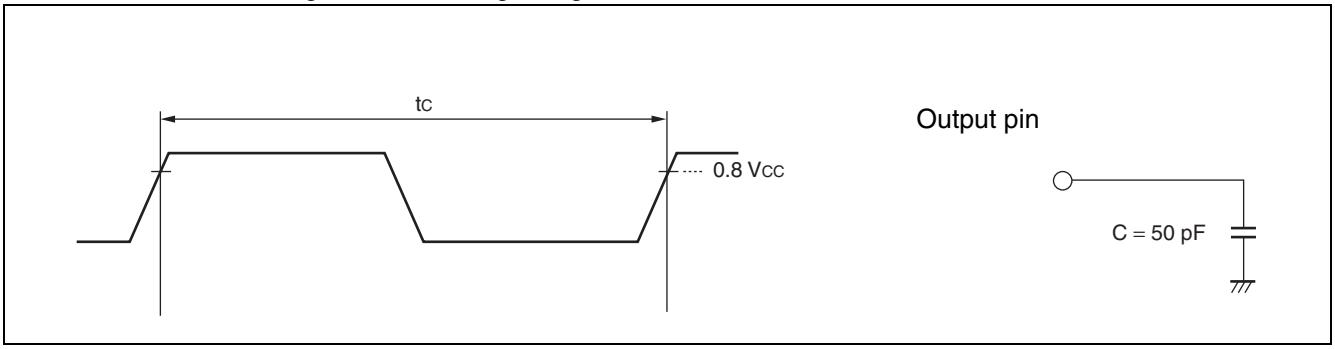
Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0 X1	—	10*2	—	20	MHz	When using the PLL within the self-oscillating range, set the multiplier so that the internal clock does not exceed the internal operating clock frequency.
Clock cycle time	t_C	X0 X1		50*2	—	100	ns	
Internal operating clock frequency	f_{CPB}	—	When 20 MHz is input as the X0 clock frequency and the oscillator circuit PLL system is set to × 4 multiplication	5*1	—	80	MHz	CPU
	f_{CPP}			5*1	—	40	MHz	Peripheral
Internal operating clock cycle time	t_{CPB}	—		12.5	—	200	ns	CPU
	t_{CPP}			25	—	200	ns	Peripheral

*1 : The values assume a gear cycle of 1/16.

*2 : When the PLL is used, the PLL multiplication rate varies depending on the frequency of the clock input to the X0 and X1 pins. Set the PLL multiplication rate so that the PLL output clock frequency is in the range between 40 MHz and 80 MHz.

PLL Multiplication Rate	1	2	3	4	5	6	7	8	Unit
PLL output clock frequency when X0 = 10 MHz	(Setting not allowed)			40	50	60	70	80	MHz
PLL output clock frequency when X0 = 20 MHz	(Setting not allowed)	40	60	80	(Setting not allowed)				

• Conditions for measuring the clock timing ratings



(2) PLL Oscillation stabilization time (LOCK UP TIME)

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
PLL Oscillation stabilization wait time (LOCK UP TIME)	t_{LOCK}*	—	—	600	—	µs

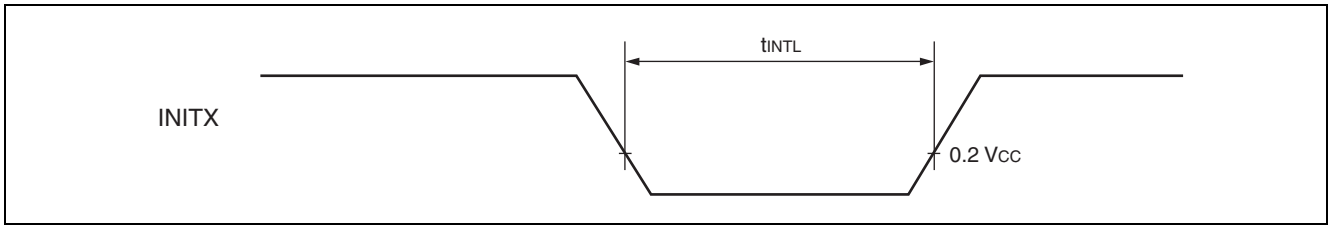
* : The length of time to wait for the PLL oscillations to stabilize.

(3) Reset Input Ratings

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	$t_{PON} + t_{STBL}$ + Oscillation time of oscillator + $tc \times 2^{13}$	—	ns
INITX input time (at STOP)				Oscillation time of oscillator + $tc \times 10$	—	ns
INITX input time (other than the above)				$tc \times 10$	—	ns

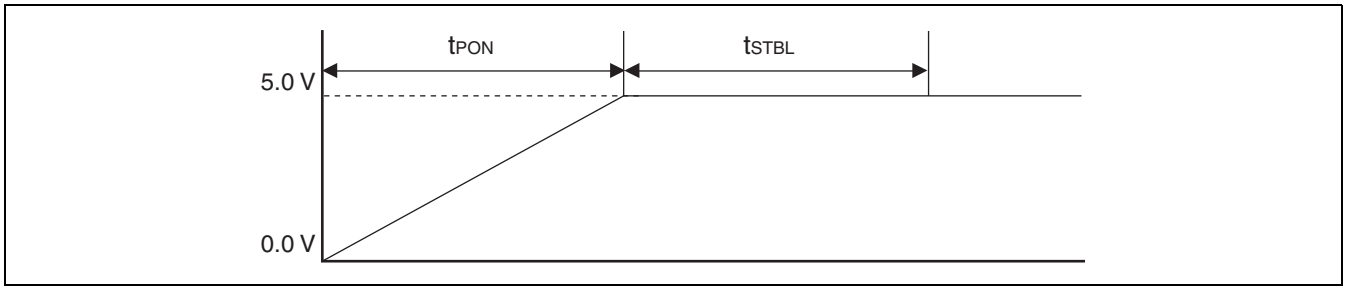
Notes : • For t_C (clock cycle time) , refer to “(1) Clock Timing”.
• For t_{PON} and t_{STBL}, refer to “ (4) Power on Rise Time /Power-on Stabilization Time Ratings”.



(4) Power on Rise Time /Power-on Stabilization Time Ratings

(V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Power on rise time	t_{PON}	VCC	—	600	—	µs
power-on stabilization time	t_{STBL}			600	—	µs



(5) UART Timing

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

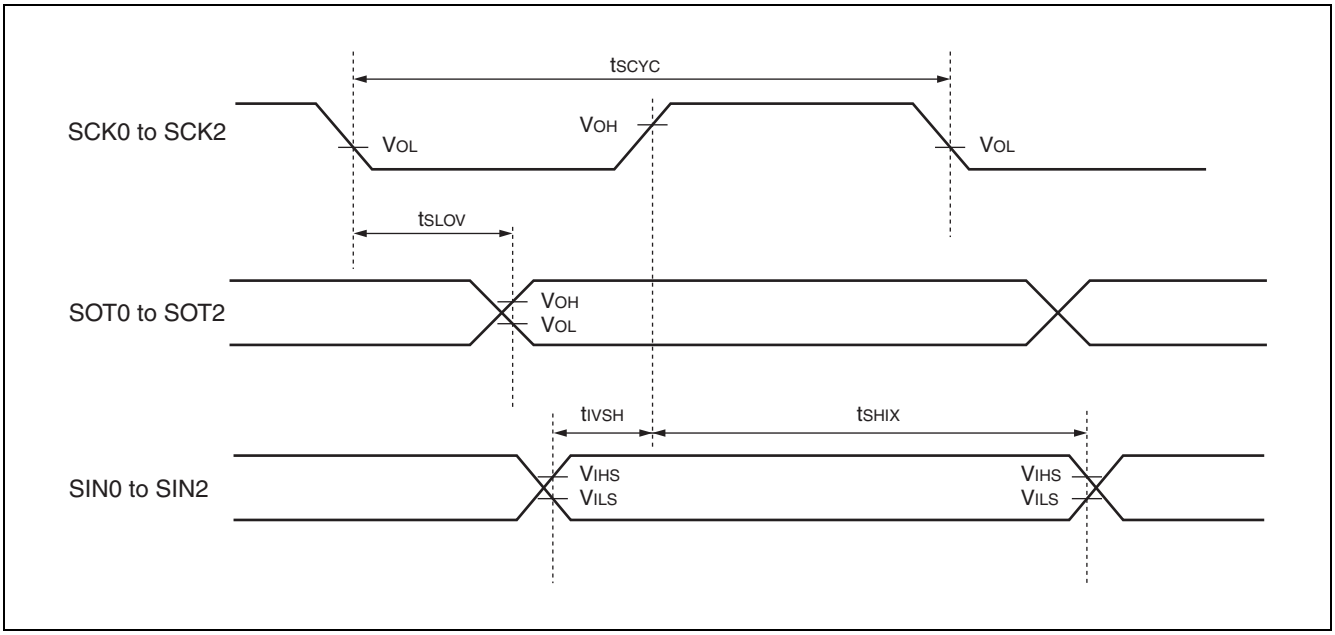
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal shift clock mode	$4t_{CYCP}$	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2 SOT0 to SOT2		− 20	+ 20	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2 SIN0 to SIN2		30	—	ns	*1
				35	—	ns	*2
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2 SIN0 to SIN2		0	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External shift clock mode	$2 \times t_{CYCP} - 10$	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		$t_{CYCP} + 10$	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0 to SCK2 SOT0 to SOT2		—	25	ns	*1
				—	35	ns	*2
Valid SIN → SCK ↑	t_{IVSH}	SCK0 to SCK2 SIN0 to SIN2		10	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK0 to SCK2 SIN0 to SIN2		20	—	ns	

*1 : V_{CC} = 4.0 V to 5.5 V

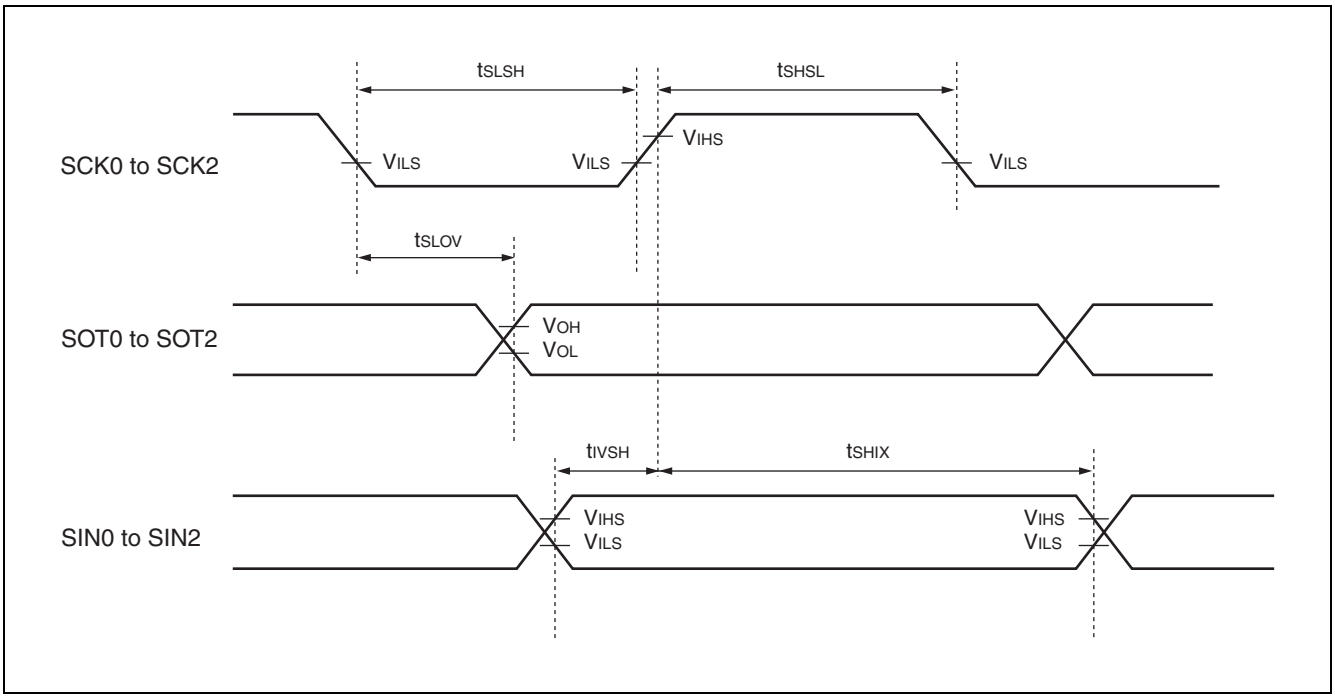
*2 : V_{CC} = 2.7 V to 4.0 V

Notes : • The above ratings are the AC characteristics for CLK synchronous mode.
• t_{CYCP} indicates the peripheral clock cycle time.

• Internal shift clock mode



• External shift clock mode



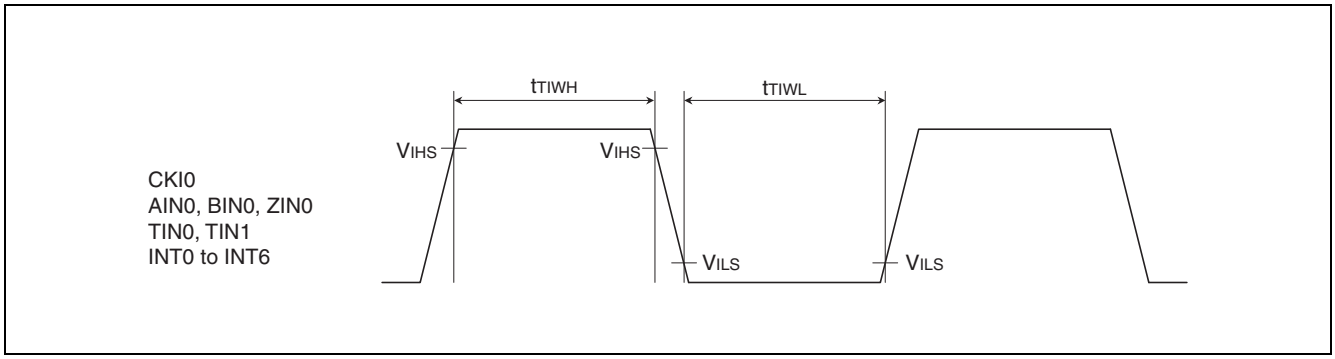
(6) Free-run Timer Clock, Up/Down Counter, Base Timer, and External Interrupt Input Timing

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Free-run timer input clock pulse width	t_{TIWH} t_{TIWL}	CKI0	—	4 × t_{CYCP}	—	ns
Up-down counter input pulse width		AIN0 BIN0 ZIN0		4 × t_{CYCP}	—	ns
Base timer input pulse width		TIN0, TIN1		4 × t_{CYCP}	—	ns
External interrupt input pulse width		INT0 to INT6		4 × t_{CYCP}	—	ns
				1.0*	—	µs

* : In stop mode

Note : t_{CYCP} indicates the peripheral clock cycle time.

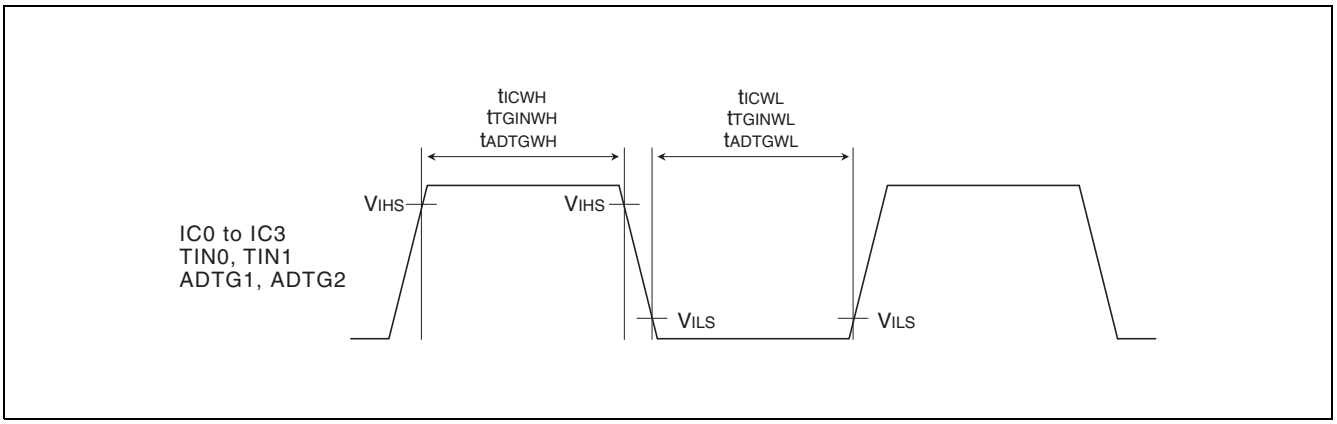


(7) Trigger Input Timing

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Input Capture trigger input	t_{ICWH} t_{ICWL}	IC0 to IC3	—	5 × t_{CYCP}	—	ns
Base timer trigger input	t_{TGINWH} t_{TGINWL}	TIN0, TIN1		4 × t_{CYCP}	—	ns
A/D activation trigger input	t_{ADTGWH} t_{ADTGWL}	ADTG1, ADTG2		5 × t_{CYCP}	—	ns

Note : t_{CYCP} indicates the peripheral clock cycle time.



(8) I²C Timing

a. Master Mode

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Standard Mode		Fast Mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SDAn, SCLn	R=1 kΩ, C=50 pF*4	0	100	0	400	kHz	
"L" width of the SCL clock	t_{LOW}			4.7	—	1.3	—	µs	
"H" width of the SCL clock	t_{HIGH}			4.0	—	0.6	—	µs	
Bus free time between STOP and START conditions	t_{BUS}			4.7	—	1.3	—	µs	
SCL↓→ SDA output delay time	t_{DLDAT}			—	$5 \times t_{CYCP}$*1	—	$5 \times t_{CYCP}$*1	ns	
Setup time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}			4.7	—	0.6	—	µs	
Hold time for a repeated START condition SDA↓→SCL↓	t_{HDSTA}			4.0	—	0.6	—	µs	The first clock pulse is generated after this.
Setup time for STOP condition SCL↑→SDA↑	t_{SUSTO}			4.0	—	0.6	—	µs	
SDA Data input hold time (vs. SCL↓)	t_{HDDAT}			$2 \times t_{CYCP}$*1	—	$2 \times t_{CYCP}$*1	—	µs	
SDA Data input setup time (vs. SCL↑)	t_{SUDAT}			250	—	100 *2	—	ns	

*1 : t_{CYCP} indicates the peripheral clock cycle time.

*2 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.
If a device does not extend the "L" period of the SCL signal, it is necessary to output the next piece of data to the SDA line 1250 ns (SDA and SCL rising Max time + t_{SUDAT}) before the SCL line is released.

*3 : For use at over 100 kHz, set the peripheral clock to at least 6 MHz.

*4 : R and C are the pull-up resistance and load capacitance of the SCL and SDA lines.

b. Slave Mode

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = AVSS10 = 0.0 V, T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Condition	Standard Mode		Fast Mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SDAn, SCLn	R=1 kΩ, C=50 pF*4	0	100	0	400	kHz	
"L" width of the SCL clock	t_{LOW}			4.7	—	1.3	—	µs	
"H" width of the SCL clock	t_{HIGH}			4.0	—	0.6	—	µs	
Bus free time between STOP and START conditions	t_{BUS}			4.7	—	1.3	—	µs	
SCL ↓ → SDA output delay time	t_{DLDAT}			—	5 × t_{CYCP} *1	—	5 × t_{CYCP} *1	ns	
Setup time for a repeated START condition SCL ↑ → SDA ↓	t_{SUSTA}			4.7	—	0.6	—	µs	
Hold time for a repeated START condition SDA ↓ → SCL ↓	t_{HDSTA}			4.0	—	0.6	—	µs	The first clock pulse is generated after this.
Setup time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}			4.0	—	0.6	—	µs	
SDA Data input hold time (vs. SCL ↓)	t_{HDDAT}			2 × t_{CYCP} *1	—	2 × t_{CYCP} *1	—	µs	
SDA Data input setup time (vs. SCL ↑)	t_{SUDAT}			250	—	100 *2	—	ns	

*1 : t_{CYCP} indicates the peripheral clock cycle time.

*2 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.
If a device does not extend the "L" period of the SCL signal, it is necessary to output the next piece of data to the SDA line 1250 ns (SDA and SCL rising Max time + t_{SUDAT}) before the SCL line is released.

*3 : For use at over 100 kHz, set the peripheral clock to at least 6 MHz.

*4 : R and C are pull-up resistance and load capacitance of the SCL and SDA lines.

6. Electrical Characteristics for the A/D Converter

(1) 8/10-bit A/D Converter

(V_{CC} = 4.0 V to 5.5 V, AVRH2 = 4.0 V to 5.5 V, V_{SS} = AVSS10 = 0 V, T_A = − 40 °C to + 85 °C)

Parameter	Sym-bol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	− 4	—	+ 4	LSB	When AVRH2 = 5.0 V
Linearity error	—	—	− 3.5	—	+ 3.5	LSB	
Differential linearity error	—	—	− 3	—	+ 3	LSB	
Zero transition voltage	V_{OT}	AN1-0 to AN1-3 AN2-0 to AN2-7	AVSS10−3.5	AVSS10+0.5	AVSS10+4.5	LSB	
Full-scale transition voltage	V_{FST}	AN1-0 to AN1-3 AN2-0 to AN2-7	AVRH2−5.5	AVRH2−1.5	AVRH2+2.5	LSB	
Conversion time*1	—	—	1.2	—	—	µs	
Analog port input current	I_{AIN}	AN1-0 to AN1-3 AN2-0 to AN2-7	—	—	10	µA	
Analog input voltage	V_{AIN}	AN1-0 to AN1-3 AN2-0 to AN2-7	AVSS10	—	AVRH2	V	
Reference voltage	—	AVRH2	AVSS10	—	AVCC10	V	
Power supply current (Analog + digital)	I_A	AVCC10	—	2	5	mA	For each 1 unit
	I_{AH}*2	AVCC10	—	—	5	µA	
Reference voltage supply current (between AVRH2 and AVSS)	I_R	AVRH2	—	1	2.5	mA	For each 1 unit, at AVRH2 = 5.0 V AVSS10 = 0 V
	I_{RH}*2	AVRH2	—	—	5	µA	For each 1 unit, at stop mode
Analog input capacitance	—	—	—	—	12.5	pF	
Interchannel disparity	—	AN1-0 to AN1-3 AN2-0 to AN2-7	—	—	4	LSB	

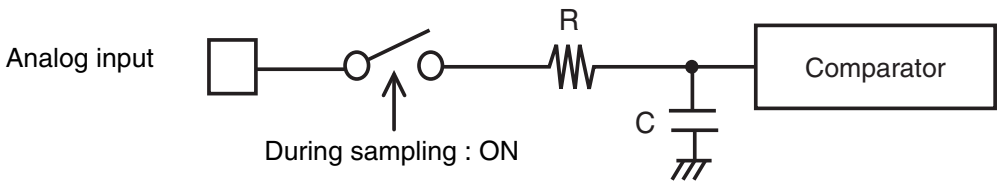
*1 : When V_{CC} = AVCC10 = 5.0 V and peripheral clock = 33 MHz

*2 : The current when the CPU is in stop mode and the A/D converter is not operating (at V_{CC} = AVCC10 = AVRH2 = 5.0 V) .

Notes : • The above figures do not guarantee the accuracy between each unit.
• Output impedance of the external circuit ≤ 2 kΩ.
• The result of 8/10 bit A/D conversion is not guaranteed at the voltage of V_{CC} = 2.7 V to 4.0 V.

- **External impedance and sampling time of analog inputs**
  - The A/D converter is fitted with a sample and hold circuit. If the external impedance is so high that there is not sufficient time for sampling, the internal sample and hold capacitor will not fully charge to the analog voltage, and the precision of the A/D conversion will be adversely affected. Therefore, in order to satisfy the A/D conversion precision specifications, either adjust the register values and operating frequency or reduce the external impedance so that the sampling time is greater than the minimum value as given by the relationship between external impedance and minimum sampling time. If you are still unable to hold enough sampling time, connect a capacitor of about 0.1 µF to the analog input pin.

• Analog input circuit schematic

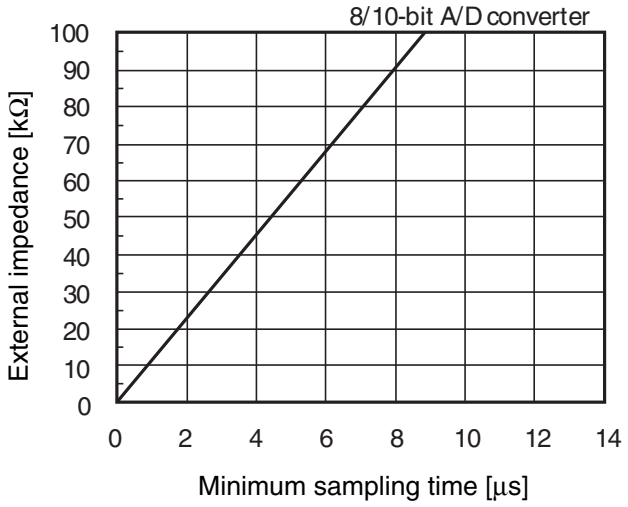


	R	C
8/10-bit A/D converter	4.6 kΩ	12.5 pF

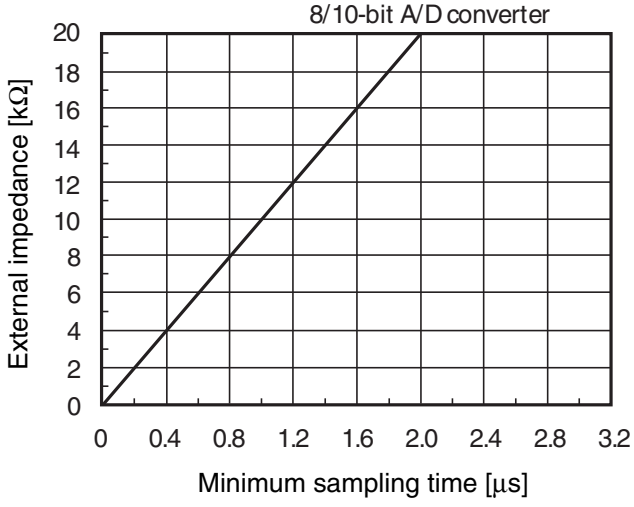
Note : The values are reference values.

• The relationship between the external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)



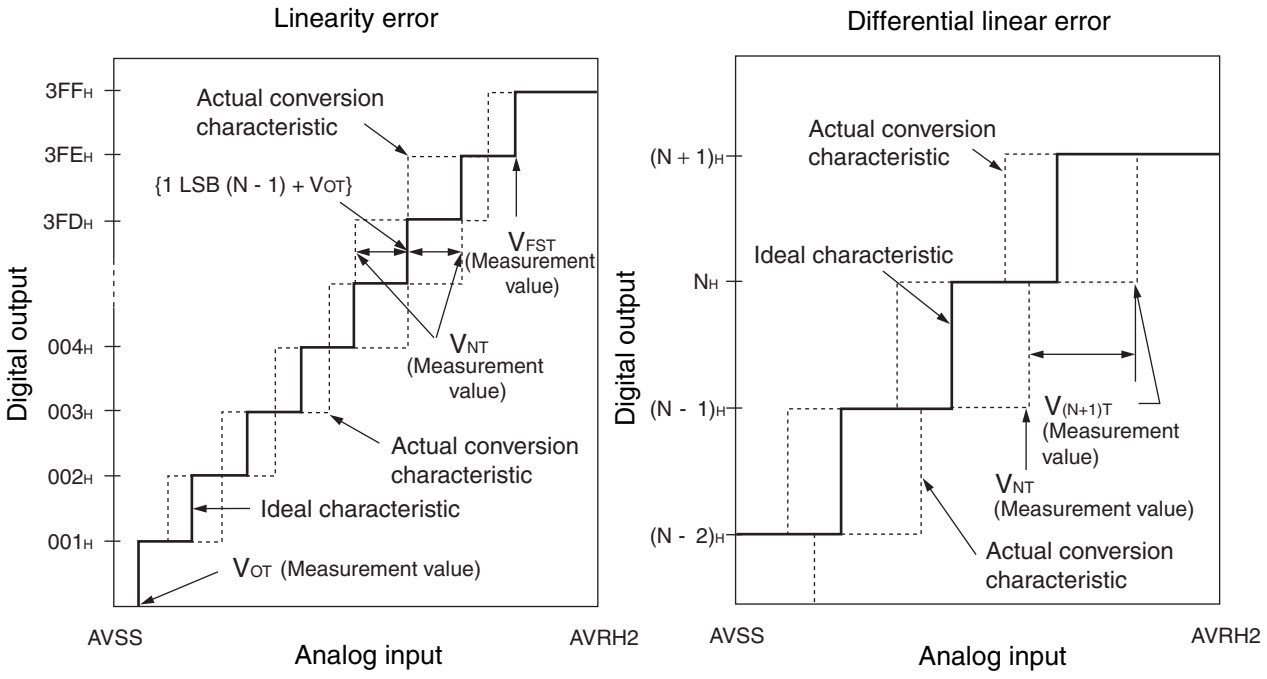
(External impedance = 0 kΩ to 20 kΩ)



- **About errors**
  - The relative error increases as the value of |AVRH2 − AVSS| decreases.

• **Definition of 8/10-bit A/D Converter Terms**

- Resolution : Analog variation that is recognized by the A/D converter.
- Linearity error : Deviation between the line connecting zero transition point (0000000000←→0000000001) and full-scale transition point (1111111110←→1111111111) and actual conversion characteristics.
- Differential linear error : Deviation from the ideal value of input voltage necessary to change the output code by ILSB.
- Total Error : This error is the difference between actual and ideal values, including the zero transition error/full-scale transition error/linearity error.



$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which digital output changes from $3FE_H$ to $3FF_H$.
V_{NT} : Voltage at which digital output changes from $(N - 1)_H$ to N_H.

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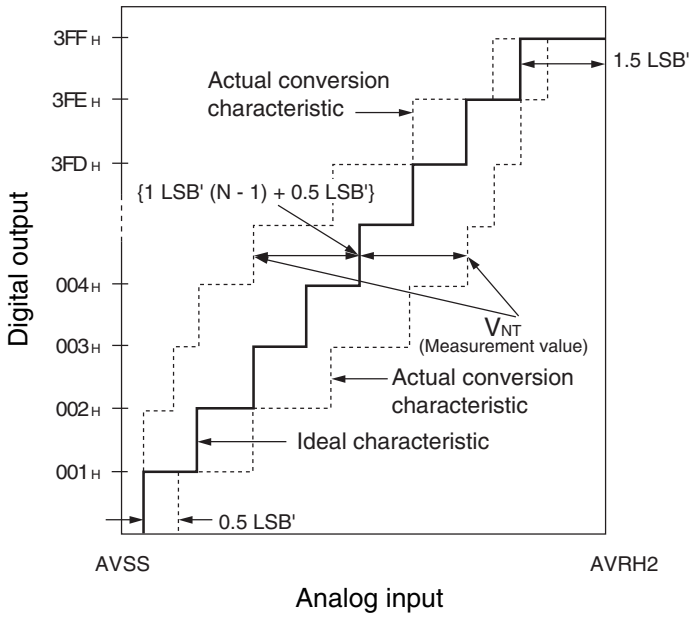
Total error



$$1\,\text{LSB'}\,(\text{ideal value}) = \frac{\text{AVRH2} - \text{AVSS}}{1024}\,[\text{V}]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\,\text{LSB'} \times (\text{N} - 1) + 0.5\,\text{LSB'}\}}{1\,\text{LSB'}}$$

N : A/D converter digital output value

V_{NT} : Voltage at which digital output changes from $(N + 1)_H$ to N_H.

V_{OT}' (ideal value) = AVSS + 0.5 LSB' [V]

V_{FST}' (ideal value) = AVRH2 – 1.5 LSB' [V]

7. Low Voltage Detection Interrupt / Reset Electrical Characteristics

a. Low Voltage Detection Interrupt

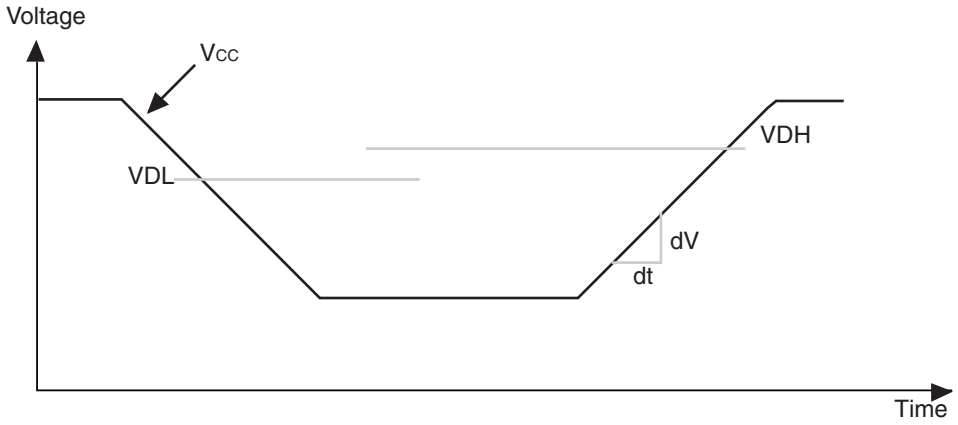
(T_A = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Detect voltage	VDL	VCC	3.40	3.70	4.00	V	When voltage drops
Release voltage	VDH	VCC	3.45	3.75	4.05	V	When voltage rises
Power supply voltage changing rate	| dV/dt |	VCC	—	—	0.004	V/µs	Value which detect voltage (VDL) and release voltage (VDH) are guaranteed within each spec.

b. Low Voltage Detection Reset

(T_A = − 40 °C to + 85 °C)

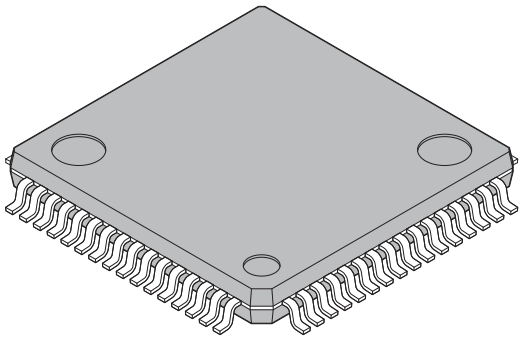
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Detect voltage	VDL	VCC	2.76	3.00	3.24	V	When voltage drops
Release voltage	VDH	VCC	2.81	3.05	3.29	V	When voltage rises
Power supply voltage changing rate	| dV/dt |	VCC	—	—	0.004	V/µs	Value which detect voltage (VDL) and release voltage (VDH) are guaranteed within each spec.



■ ORDERING INFORMATION

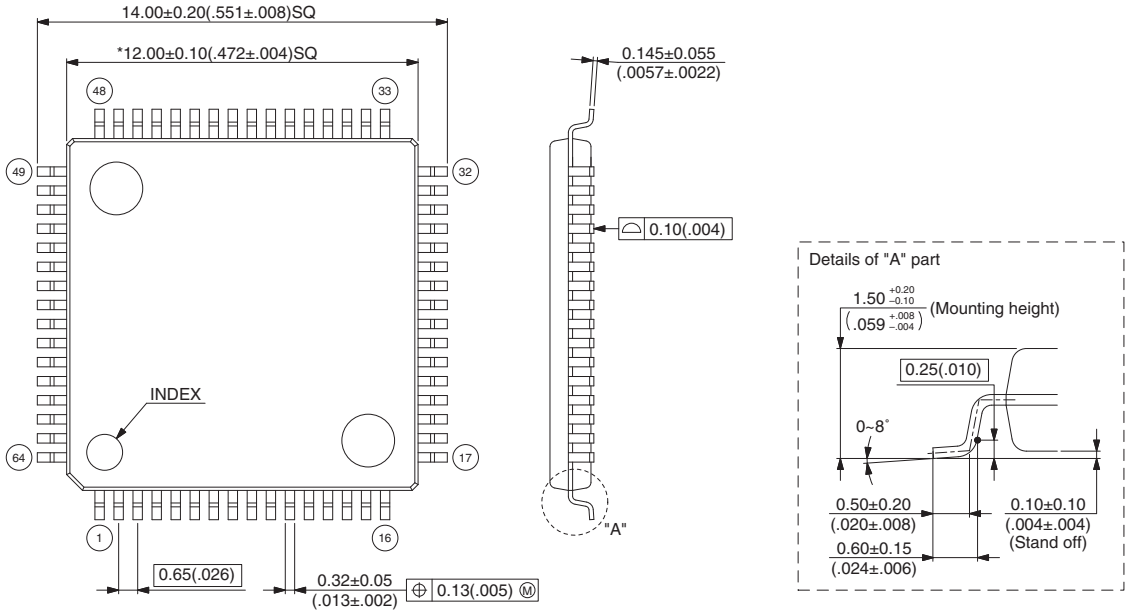
Part No.	Package
MB91F492PMC-GE1	64-pin plastic LQFP (FPT-64P-M23)
MB91F492PMC1-GE1	64-pin plastic LQFP (FPT-64P-M24)

■ PACKAGE DIMENSIONS

64-pin plastic LQFP		
 (FPT-64P-M23)	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

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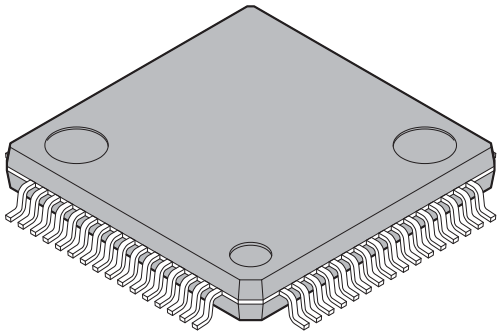
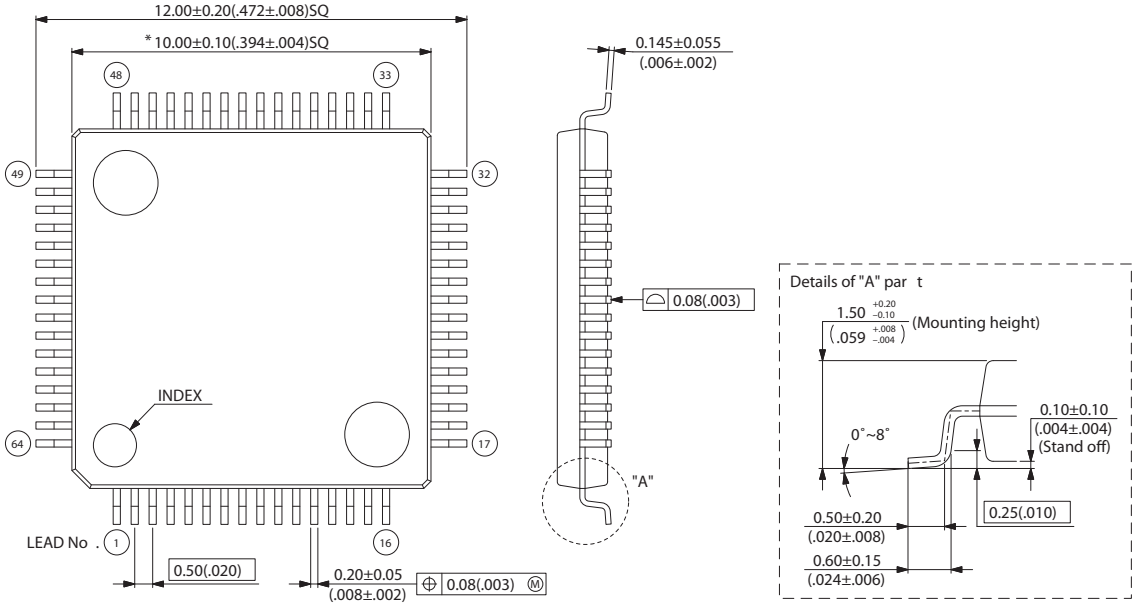
64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Pa ckage width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	We ight	0.32 g
(FPT -64P-M24)	Code (Ref erence)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT -64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensi ons in mm (in ches).
Note: The values in parentheses are reference values

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