

Single Output, Low Power Programmable Clock Generator

Features

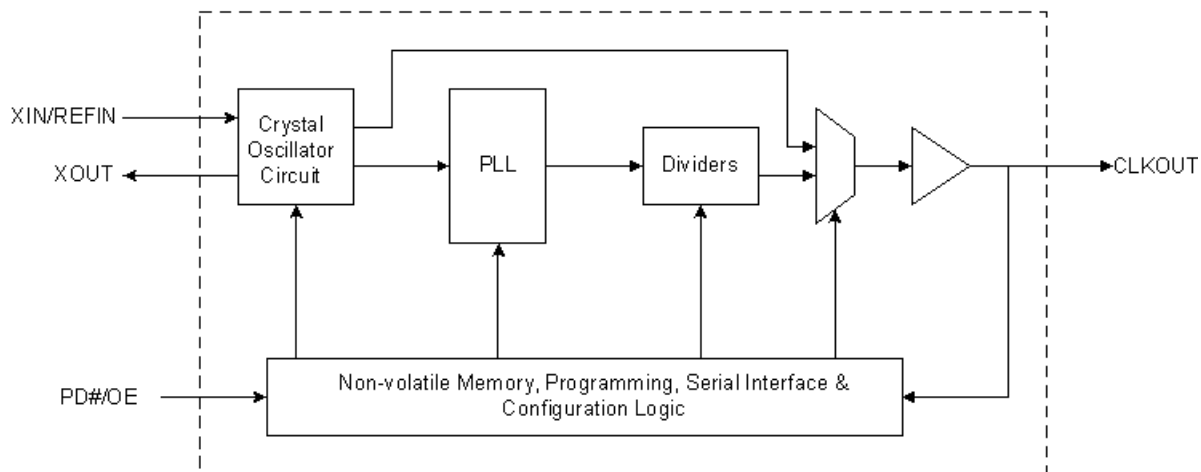
- Small Footprint, 8-pin QFN 1.7 mm × 1.7 mm × 0.6 mm package
- Low Power and Low Jitter Operation
- Multiple Operating Voltages:
 - CY22U1S: 2.5 V, 3.0 V, or 3.3 V
 - CY22U1L: 1.8 V
- Programmable Single Output Clock Generator Frequency Range:
 - 1 to 200 MHz
- Crystal or External Reference Clock Input Frequency Range:
 - Fundamental Tuned Crystal: 8 to 48 MHz
 - External Reference Clock: 1 to 166 MHz
- Programmable Capacitor Tuning Array
- Programmable PD# or OE Control Pin
- Programmable Asynchronous or Synchronous OE and PD# Modes

Benefits

- Services digital televisions and displays, set top boxes, multifunction printers, and a variety of consumer electronics applications.
- Saves PCB space due to small form factor.
- Enables quick turnaround and flexibility and adaptability to design changes through programmability.
- Enables synthesis of highly accurate and stable output clock frequencies with zero or low ppm error.
- Enables fine tuning of output clock frequency by adjusting the crystal load C_{Load} using programmable internal capacitors.
- Lowers clock solution cost by pairing a high frequency PLL programmability with a low cost, low frequency crystal.
- Enables low power during the power down or output disable function.
- Provides flexibility for system applications through selectable asynchronous or synchronous output enable and disable.

For a complete list of related documentation, click [here](#).

Logic Block Diagram

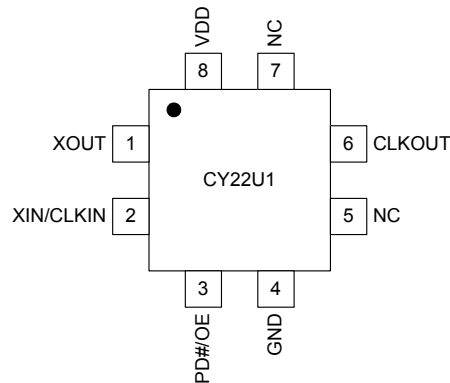


Contents

| | | | |
|--|----------|--|-----------|
| Pinouts | 3 | Switching Waveforms | 8 |
| Pin Definitions | 3 | Ordering Information | 10 |
| Functional Description | 3 | Possible Configurations | 10 |
| Configurable PLL | 3 | Ordering Code Definitions | 10 |
| Input Reference Clock Option | 3 | Package Drawing and Dimensions | 12 |
| Multiple VDD Power Supply Option | 4 | Acronyms | 13 |
| Power Management Feature | 4 | Document Conventions | 13 |
| Crystal Oscillator Tuning Circuit | 4 | Units of Measure | 13 |
| Programmable Features | 5 | Document History Page | 14 |
| Programming Support | 5 | Sales, Solutions, and Legal Information | 15 |
| Absolute Maximum Ratings | 5 | Worldwide Sales and Design Support | 15 |
| Recommended Operating Conditions | 5 | Products | 15 |
| DC Electrical Specifications | 6 | PSoC Solutions | 15 |
| AC Electrical Specifications | 7 | | |
| Recommended Crystal Specifications | | | |
| for SMD Package | 7 | | |

Pinouts

Figure 1. Pin Diagram – CY22U1 8-pin 1.7 mm × 1.7 mm QFN



Pin Definitions

CY22U1 8-pin 1.7 mm × 1.7 mm QFN

| Pin Number | Name | IO | Description |
|------------|-----------|--------|---|
| 1 | XOUT | Output | Crystal output. Float for external clock input. |
| 2 | XIN/CLKIN | Input | Crystal or external clock input. |
| 3 | PD#/OE | Input | Multifunction pin. Active low power down or active high output enable pin. Has weak internal pull up. |
| 4 | GND | Power | Power supply ground. |
| 5 | NC | – | No connect. Pin has no internal connection. |
| 6 | CLKOUT | Output | Programmable clock output. Output voltage depends on VDD. Has weak internal pull down. |
| 7 | NC | – | No connect. Pin has no internal connection. |
| 8 | VDD | Power | Programmable power supply: CY22U1S: 2.5 V, 3.0 V, 3.3 V (standard voltage) CY22U1L: 1.8 V (low voltage) |

Functional Description

The UniClock CY22U1 is a programmable, high accuracy, PLL-based clock generator device designed to replace crystals and crystal oscillators and save on cost and board space, while increasing reliability. The low jitter and accurate outputs makes this device suitable for use in digital televisions and displays, set top boxes, multifunction printers, and a variety of consumer electronics applications.

The device has several programmable options listed in the section [Programmable Features on page 5](#). The entire configuration is one time programmable.

Configurable PLL

The device uses a programmable PLL to generate output frequencies from 1 to 200 MHz. The high resolution of the PLL and flexible output dividers provide this flexibility.

Input Reference Clock Option

There is an option of a crystal or clock signal for the input reference clock. The frequency range for crystal (XIN) is 8 MHz to 48 MHz, while the range for an external reference clock (CLKIN) is 1 MHz to 166 MHz. A PLL bypass mode enables this device to be used as a crystal oscillator.

Multiple VDD Power Supply Option

The device has programmable power supply options. The operating supply voltages are 2.5 V, 3.0 V, or 3.3 V for CY22U1S and 1.8 V for CY22U1L.

Power Management Feature

The UniClock CY22U1 offers PD# (active LOW) and OE (active HIGH) functions. When the power down mode is selected (PD# = 0), the oscillator and PLL are placed in a low supply current standby mode and the output is tristated and weakly pulled LOW. The oscillator and PLL circuits must relock when the part exits the power down mode. If the output is disabled (OE = 0), the output is tristated and weakly pulled LOW. In this mode, the oscillator and PLL circuits continue to operate, which enables a rapid return to normal operation when the output is enabled.

In addition, the PD# or OE mode can be programmed to occur asynchronously or synchronously with respect to the output signal. When the asynchronous setting is used, entering power down or disabling the output occurs immediately (enabling logic delays), regardless of the position in the clock cycle. Similarly, exiting power down or enabling the output occurs immediately with no guarantee of full output clock pulses. However, when the synchronous setting is used, the part waits for a falling edge at the output before entering power down or disabling the output. This prevents output glitches. The first output pulse is guaranteed to be a full clock pulse when enabling outputs with a synchronous OE pin. The first output pulse is not guaranteed to

be a full clock when exiting power down in synchronous or asynchronous mode.

Output Frequency Tuning

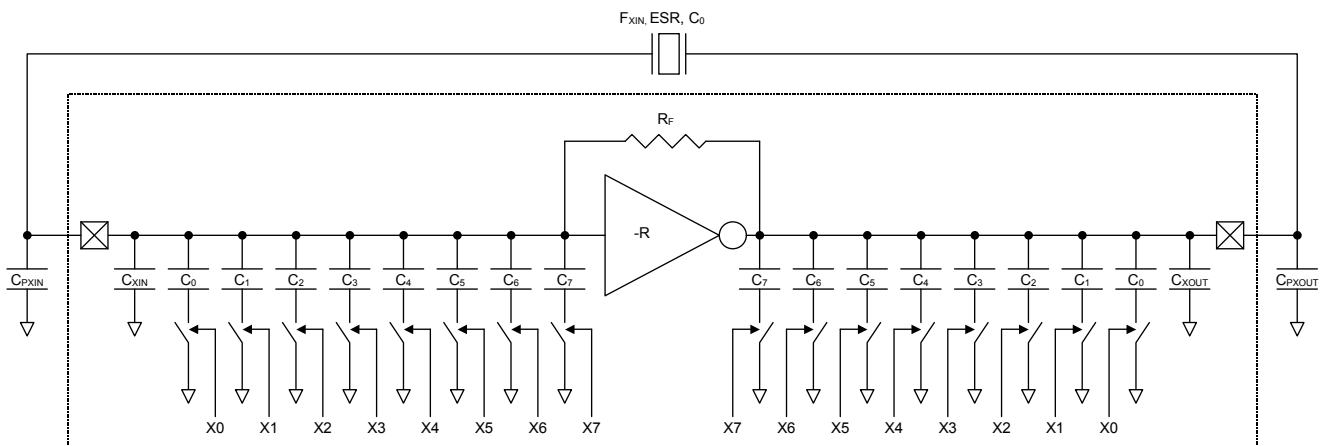
The UniClock CY22U1 contains an on-chip oscillator with a built in programmable capacitor array for fine tuning of the output frequency. The capacitive load seen by the crystal is adjusted by programming the memory bits. This feature can compensate for crystal variations or provide a more accurate synthesized frequency. Figure 2 shows the crystal oscillator tuning circuit block diagram.

Crystal Oscillator Tuning Circuit

Table 1. Crystal Oscillator Tuning Capacitor Values

| Cap | Value ^[1] | Unit |
|----------------|----------------------|------|
| C ₇ | 5.000 | pF |
| C ₆ | 2.500 | pF |
| C ₅ | 1.250 | pF |
| C ₄ | 0.625 | pF |
| C ₃ | 0.313 | pF |
| C ₂ | 0.156 | pF |
| C ₁ | 0.078 | pF |
| C ₀ | 0.039 | pF |

Figure 2. Crystal Oscillator Tuning Block Diagram



Note

1. The capacitor values are nominal.

Programmable Features

The following list of features can be custom configured:

- PLL frequency and output divider value
- Oscillator tuning (crystal load) capacitance value
- Direct oscillator output (PLL bypass)
- High or low power supply voltage operation
- Power management mode (OE or PD#)
- Power management timing (synchronous or asynchronous)

Programming Support

The device is available in factory and field programmable versions. The CyClockMaker Programming kit (CY3675-CLKMAKER1) along with CyClockWizard configuration software is used for field programming the device. For specific programming needs, contact your local Cypress field application engineer (FAE) or sales representative.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 2. Absolute Maximum Ratings

| Parameter ^[2] | Description | Condition | Min | Max | Unit |
|--------------------------|---|-----------------------------|----------------|-----------------------|-------|
| V _{DD} | Supply voltage, 2.5 V/3.0 V/3.3 V range | | -0.5 | 4.4 | V |
| | Supply voltage, 1.8 V range | | -0.5 | 2.8 | V |
| V _{IN} | Input voltage | Relative to V _{SS} | -0.5 | V _{DD} + 0.5 | V |
| T _S | Temperature, storage | Non functional | -55 | +125 | °C |
| T _J | Temperature, junction | Non functional | -40 | +125 | °C |
| ESD _{HBM} | ESD protection (human body model) | JEDEC EIA/JESD22-A114-E | 2000 | - | Volts |
| D _{RET} | Data retention at T _J = 125 °C | | 10 | - | Yr. |
| PR _{CYCLE} | Maximum programming cycle | | 1 | | |
| UL-94 | Flammability rating | | V-0 at 1/8 in. | | |
| MSL | Moisture sensitivity level | | 3 | | |

Recommended Operating Conditions

| Parameter ^[2] | Description | Min | Typ | Max | Unit |
|--------------------------|---|------|-----|-----|------|
| V _{DD} | Supply voltage, 1.8 V operating range for CY22U1L | 1.6 | - | 2.0 | V |
| | Supply voltage, 2.5 V operating range for CY22U1S | 2.2 | - | 2.8 | V |
| | Supply voltage, 3.0 V operating range for CY22U1S | 2.7 | - | 3.3 | V |
| | Supply voltage, 3.3 V operating range for CY22U1S | 3.0 | - | 3.6 | V |
| T _{AC} | Commercial ambient temperature | 0 | - | 70 | °C |
| T _{AI} | Industrial ambient temperature | -40 | - | 85 | °C |
| T _{PU} | Power up time for V _{DD} to reach minimum specified voltage (power ramp must be monotonic) | 0.05 | - | 500 | ms |
| T _{PD} | Minimum pulse width of PD#/OE input | 100 | - | - | ns |
| C _{OUT} | Output load capacitance | - | - | 15 | pF |

Note

2. Stresses beyond those listed under Table 2 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rated Conditions for extended periods may affect device reliability or cause permanent device damage.

DC Electrical Specifications

| Parameter ^[3] | Description | Test Conditions | Min | Typ | Max | Unit |
|--------------------------|----------------------------------|---|-----------------------|-----|--------------------------------------|------|
| V _{IL1} | Input low voltage of PD#/OE | | – | – | 0.2 × V _{DD} | V |
| V _{IH1} | Input high voltage of PD#/OE | | 0.8 × V _{DD} | – | – | V |
| V _{IL2} | Input low voltage of REFIN | CY22U1S | -0.2 | – | 0.4 | V |
| | | CY22U1L | -0.2 | – | 0.4 | V |
| V _{IH2} | Input high voltage of REFIN | CY22U1S | 1.2 | – | 2.1 | V |
| | | CY22U1L | 1.2 | – | V _{DD} + 0.3 ^[4] | V |
| V _{OL1} | Output low voltage | I _{OL} = 8 mA, V _{DD} = 3.0/3.3 V | – | – | 0.4 | V |
| V _{OH1} | Output high voltage | I _{OH} = 8 mA, V _{DD} = 3.0/3.3 V | V _{DD} – 0.4 | – | – | V |
| V _{OL2} | Output low voltage | I _{OL} = 4 mA, V _{DD} = 1.8/2.5 V | – | – | 0.1 × V _{DD} | V |
| V _{OH2} | Output high voltage | I _{OH} = 4 mA, V _{DD} = 1.8/2.5 V | 0.9 × V _{DD} | – | – | V |
| I _{IL} | Input low current | Input = V _{SS} | – | <1 | 10 | μA |
| I _{IH} | Input high current | Input = V _{DD} | – | <1 | 10 | μA |
| I _{OZL} | Output leakage current | Output = V _{SS} , T _j = 85 °C | – | <1 | 5 | μA |
| I _{OZH} | Output leakage current | Output = V _{DD} | – | – | 50 | μA |
| I _{DD} | Power supply current for CY22U1L | F _{OUT} = 50 MHz, 15 pF load | – | – | 7.5 | mA |
| | | F _{OUT} = 200 MHz, 15 pF load | – | – | 15 | mA |
| | Power supply current for CY22U1S | F _{OUT} = 50 MHz, 15 pF load | – | – | 10 | mA |
| | | F _{OUT} = 200 MHz, 15 pF load | – | – | 25 | mA |
| I _{PD} | Power down current | T _j = 85 °C | – | 25 | 50 | μA |
| R _{UP} | Input pull up resistors | PD#/OE = low | 1 | – | 6 | MΩ |
| | | PD#/OE = high | 100 | – | 250 | kΩ |
| R _{DN} | Output pull down resistors | | 500 | – | 1500 | kΩ |
| C _{IN} | Input capacitance of PD#/OE pin | | – | – | 7 | pF |

Notes

3. Parameters are guaranteed by design and characterization. Not 100% tested in production.
4. V_{IH2} absolute maximum value is 2.1V. For V_{DD} = 1.6 V to 1.8 V, the maximum V_{IH2} is V_{DD} + 0.3 V.

AC Electrical Specifications

| Parameter ^[5] | Description | Test Conditions | Min | Typ | Max | Unit |
|---------------------------|---|--|-------------|----------------|-----------------|--|
| F _{IN} (Crystal) | Crystal frequency range (XIN) | | 8 | – | 48 | MHz |
| F _{IN} (Clock) | Clock frequency range (REFIN) | | 1 | – | 166 | MHz |
| F _{CLK} | Output frequency | | 1 | – | 200 | MHz |
| T _R | Output rise time | Measured from 20% to 80% V _{DD} , C _{OUT} = 15 pF | – | – | 1.5 | ns |
| T _F | Output fall time | Measured from 80% to 20% V _{DD} , C _{OUT} = 15 pF | – | – | 1.5 | ns |
| DC | Output clock duty cycle | Using PLL as a source | 45 | 50 | 55 | % |
| T _{CCJ} | Cycle-to-cycle jitter of CLKOUT using PLL | F _{OUT} ≥ 100 MHz 100 MHz ≥ F _{OUT} ≥ 50 MHz F _{OUT} < 50 MHz | – – – | 75 150 – | 125 200 1 | ps ps %T _{OUT} ^[6] |
| T _P | Period jitter of CLKOUT using PLL | F _{OUT} ≥ 100 MHz 100 MHz ≥ F _{OUT} ≥ 50 MHz F _{OUT} < 50 MHz | – – – | 75 150 – | 125 200 1 | ps ps %T _{OUT} ^[6] |
| T _{PO,CLK} | Power on time for output clock | | – | – | 5 | ms |
| T _{PU,CLK} | Power up time from power down for output clock | | – | – | 5 | ms |
| T _{PD,ASYNC} | Time from falling edge of PD# to stopped outputs, asynchronous mode | | – | – | 100 | ns |
| T _{PD,SYNC} | Time from falling edge of PD# to stopped outputs, synchronous mode | | – | – | 1.5T + 100 | ns |
| T _{OD,ASYNC} | Time from falling edge of OE to stopped outputs, asynchronous mode | | – | – | 100 | ns |
| T _{OD,SYNC} | Time from falling edge of OE to stopped outputs, synchronous mode | | – | – | 1.5T + 100 | ns |
| T _{OE,ASYNC} | Time from rising edge of OE to running outputs, asynchronous mode | | – | – | 100 | ns |

Recommended Crystal Specifications for SMD Package

| Parameter | Description | Range 1 | Range 2 | Range 3 | Unit |
|------------------|-----------------------------------|---------|---------|---------|------|
| F _{MIN} | Minimum frequency | 8 | 14 | 28 | MHz |
| F _{MAX} | Maximum frequency | 14 | 28 | 48 | MHz |
| R ₁ | Maximum motional resistance (ESR) | 135 | 50 | 30 | Ω |
| C ₀ | Nominal shunt capacitance | 4 | 4 | 2 | pF |
| C _L | Nominal load capacitance | 18 | 14 | 12 | pF |
| D _L | Maximum crystal drive level | 300 | 300 | 300 | μW |

Notes

5. Parameters are guaranteed by design and characterization. Not 100% tested in production.
 6. %T_{OUT} is the percentage of the output clock period.

Switching Waveforms

Figure 3. CLKOUT Rise and Fall Time

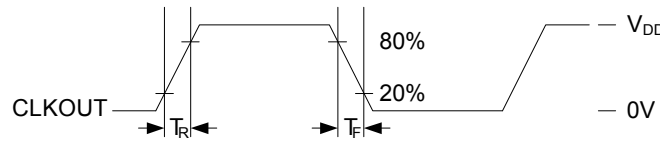


Figure 4. Duty Cycle Timing (DC)

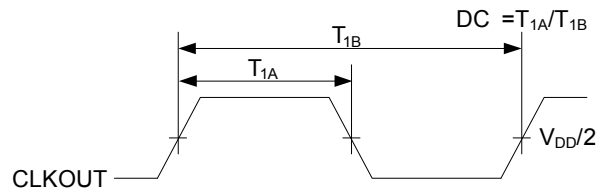


Figure 5. Period Jitter

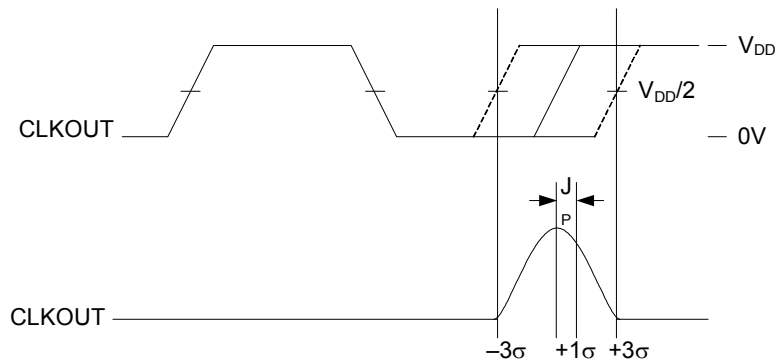


Figure 6. Cycle to Cycle Jitter

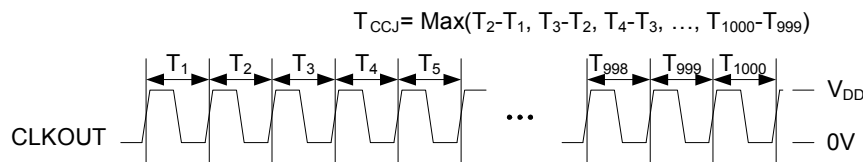
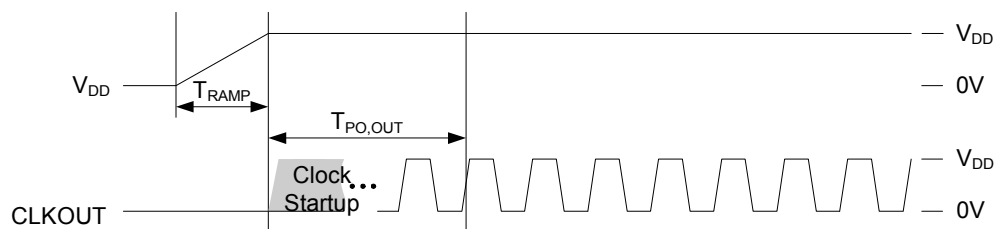


Figure 7. Power On Timing



Switching Waveforms (continued)

Figure 8. Power Down Timing (Synchronous and Asynchronous Modes) and Power Up Timing

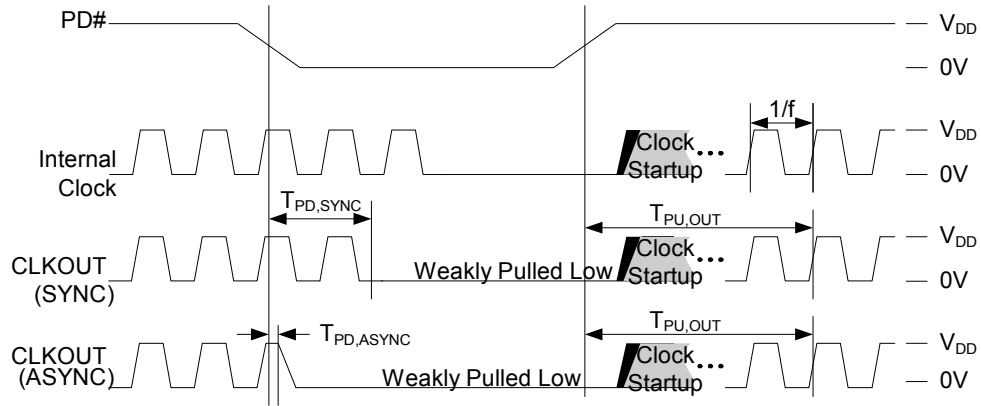
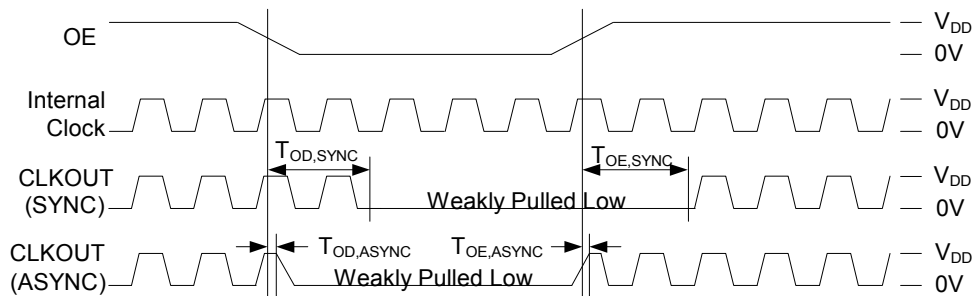


Figure 9. CLKOUT Enable (Synchronous and Asynchronous Modes) and CLKOUT Disable Timing



Ordering Information

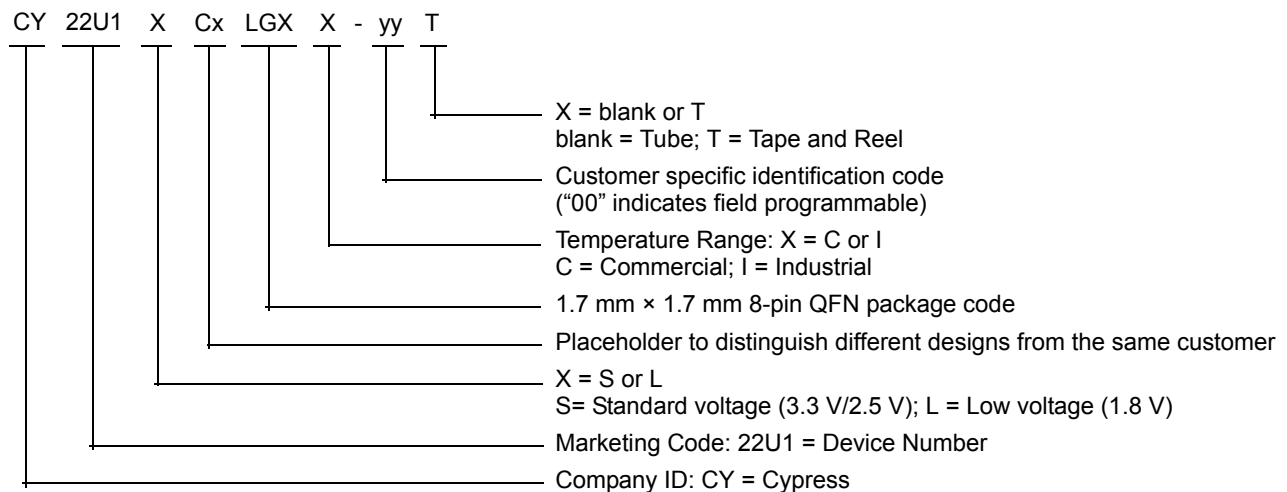
| Part Number | Type | V _{DD} (V) | Production Flow |
|-------------------|------|---------------------|-----------------|
| Programmer | | | |
| CY3675-CLKMAKER1 | | Programming Kit | |

Possible Configurations

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or Sales Representative for more information.

| Part Number ^[7, 8] | Type | V _{DD} (V) | Production Flow |
|-------------------------------|-----------|--|------------------------------|
| Pb-free | | | |
| CY22U1SCxLGXI-yy | 8-pin QFN | Supply voltage: 2.5 V, 3.0 V, or 3.3 V | Industrial, -40 °C to +85 °C |
| CY22U1LCxLGXI-yy | 8-pin QFN | Supply voltage: 1.8 V | Industrial, -40 °C to +85 °C |

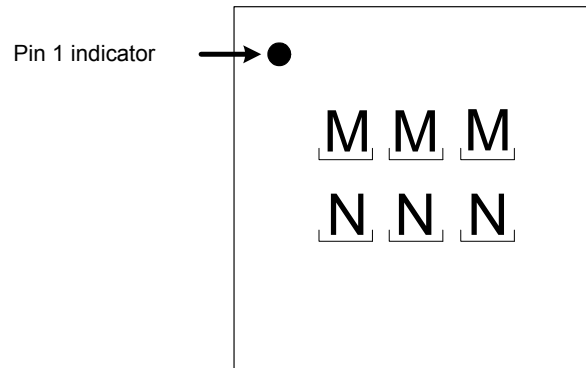
Ordering Code Definitions



Notes

7. x indicates a part marking placeholder to distinguish different configurations for the same customer, beginning alphabetically from "A".
8. yy indicates "Factory Programmable" and are factory programmed configurations. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Figure 10. Actual Marking

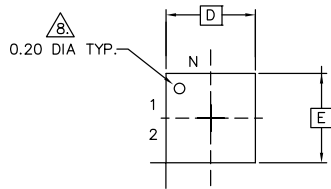


(MMM) = 7th, 8th and 9th characters of marketing part number

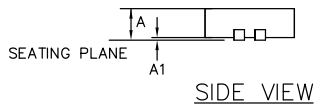
(NNN) = Last 3 digits of assembly lot number

Package Drawing and Dimensions

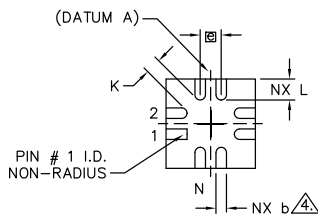
Figure 11. 8-pin QFN (1.7 mm × 1.7 mm × 0.6 mm) LG08A Package Outline, 001-49591



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M - 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, ϕ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.

| SYMBOL | COMMON DIMENSIONS | | | No. of Terminals |
|--------|-------------------|------|------|------------------|
| | MIN. | NOM. | MAX. | |
| A | 0.50 | 0.55 | 0.60 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| ϕ | 0 | | 12 | 2 |
| K | 0.20 MIN. | | | |
| D | 1.7 BSC | | | |
| E | 1.7 BSC | | | |
| ϕ | 0.40 BSC | | | |
| N | 8 | | | 3 |
| ND | 2 | | | 5 |
| NE | 2 | | | 5 |
| L | 0.35 | 0.40 | 0.45 | |
| b | 0.15 | 0.20 | 0.25 | 8 |

REFERENCE JEDEC#: MO-220

PACKAGE WEIGHT: Refer to PMDD Spec.

001-49591 *B

Acronyms

| Acronym | Description |
|---------|--|
| EIA | electronic industries alliance |
| ESD | electrostatic discharge |
| FAE | field application engineer |
| JEDEC | joint electron devices engineering council |
| MSL | moisture sensitivity level |
| OE | output enable |
| PCB | printed circuit board |
| PD | power down |
| PLL | phase-locked loop |
| QFN | quad flat no-lead |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-------------------|
| °C | degree Celsius |
| kΩ | kilohm |
| MHZ | megahertz |
| MΩ | megaohm |
| μA | microampere |
| μW | microwatt |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| V | volt |

Document History Page

| Document Title: UniClock CY22U1, Single Output, Low Power Programmable Clock Generator | | | | |
|--|---------|-----------------|-----------------|---|
| Document Number: 001-50320 | | | | |
| Rev | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 2612925 | CXQ / AESA | 11/26/2008 | New data sheet. |
| *A | 2636981 | CXQ / PYRS | 01/15/09 | Removed sub-section "Programmable Output Drive Strength" under the main section Functional Description . Updated sub-section Input Reference Clock Option under the main section Functional Description (Changed input range minimum value from 8 MHz to 1 MHz, changed input range maximum value from 200 MHz to 166 MHz). Updated Programming Support (Replaced "CY3672 Programming kit along with CyberClocksOnline" reference with "CyClockMaker Programming kit along with CyClockDesigner" reference). Updated DC Electrical Specifications (Changed minimum and maximum values of V_{IH2} and V_{IL2} parameters, added typical value of I_{PD} parameter (25 μ A)). Updated AC Electrical Specifications (Added T_p parameter and its details). Updated Ordering Information (updated part numbers) and added marking format information. Updated Package Drawing and Dimensions to spec 001-49591. |
| *B | 2673516 | CXQ / PYRS | 03/13/09 | Changed status of data sheet from Advanced to Preliminary. Updated Features (Deleted "1.8 V" when referring to external reference). Updated DC Electrical Specifications (Updated Test Conditions of V_{IL2} and V_{IH2} parameters (fixed error in device name), changed maximum value of V_{IH2} parameter for CY22M1L, added note 4 and referred the same note in maximum value of V_{IH2} parameter, replaced TBD with values for maximum values of I_{DD} parameter). |
| *C | 2748211 | TSAI | 08/10/09 | Posting to external web. |
| *D | 3450335 | PURU | 11/29/2011 | Changed status of data sheet from Preliminary to Final. Updated hyper links in Programming Support . Updated Ordering Information (Removed Obsolete parts, added existing parts, added Programmer and socket in table, divided Ordering information into Possible Configurations table) and added Ordering Code Definitions . Updated Package Drawing and Dimensions . Added Acronyms and Units of Measure . Updated in new template. |
| *E | 3847630 | PURU | 12/20/2012 | Updated Ordering Information (Updated part numbers, also removed details of pruned parts in Possible Configurations). Updated Package Drawing and Dimensions : spec 001-49591 – Changed revision from *A to *B. |
| *F | 4580588 | TAVA | 12/05/2014 | Added related documentation hyperlink in page 1. Removed obsolete parts. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|--------------------------|--|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2008-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.